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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	91
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12dt256mpve

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V03.00	24 March 2003			Initial version for Maskset L91N , based on MC9S12DP256B V02.11.
V03.01	30 June 2003			• added new HCS12 core documentation • added cumulative program/erase cycle limitation to Table A-12 for EEPROM • updated Table 0-2 Document References
V03.02	24 July 2003			• removed cumulative program/erase cycle limitation from Table A-12 for EEPROM • added LRAE generic load and execute info to section 15
V03.03	26 July 2003			• Added MC9S12DT256 in QFP 80 to Table 0-1
V03.04	15 March 2004			• Added Masksets 0L01Y and 4L91N
V03.05	4 April 2005			• Changed NVM data retention specification **Table A-12**
V03.06	12 Oct 2005			• Corrected Flash Burst Programming Time **Table A-11**, • NVM Reliability Spec **Table A-12** ,**Figure A-2**
V03.07	02 Jan 2006			• Corrected Flash Burst Programming Time **Table A-11**,

Section 3 System Clock Description

Section 4 Modes of Operation

Section 5 Resets and Interrupts

Section 6 HCS12 Core Block Description

List of Tables

The Device Guide provides information about the MC9S12DT256 device made up of standard HCS12 blocks and the HCS12 processor core.

This document is part of the customer documentation. A complete set of device manuals also includes the HCS12 Core User Guide and all the individual Block Guides of the implemented modules. In a effort to reduce redundancy all module specific information is located only in the respective Block Guide. If applicable, special implementation details of the module are given in the block description sections of this document.

See **Table 0-2** for names and versions of the referenced documents throughout the Device User Guide.

Table 0-2 Document References

User Guide	Version	Document Order Number
CPU12 Reference Manual	V04	CPU12RM/AD
HCS12 Multiplexed External Bus Interface (MEBI) Block Guide	V03	S12MEBIV3/D
HCS12 Module Mapping Control (MMC) Block Guide	V04	S12MMCV4/D
HCS12 Interrupt (INT) Block Guide	V01	S12INTV1/D
HCS12 Background Debug (BDM) Block Guide	V04	S12BDMV4/D
HCS12 Breakpoint (BKP) Block Guide	V01	S12BKPV1/D
Clock and Reset Generator (CRG) Block User Guide	V04	S12CRGV4/D
Enhanced Capture Timer (ECT_16B8C) Block User Guide	V01	S12ECT16B8CV1/D
Analog to Digital Converter 10 Bit 8 Channels (ATD_10B8C) Block User Guide	V02	S12ATD10B8CV2/D
Inter IC Bus (IIC) Block User Guide	V02	S12IICV2/D
Asynchronous Serial Interface (SCI) Block User Guide	V02	S12SCIV2/D
Serial Peripheral Interface (SPI) Block User Guide	V03	S12SPIV3/D
Pulse Width Modulator 8 Bit 8 Channel (PWM_8B8C) Block User Guide	V01	S12PWM8B8CV1/D
256 K Byte Flash (FTS256K) Block User Guide	V03	S12FTS256KV3/D
4K Byte EEPROM (EETS4K) Block User Guide	V02	S12EETS4KV2/D
Byte Level Data Link Controller -J1850 (BDLC) Block User Guide	V01	S12BDLCV1/D
Motorola Scalable CAN (MSCAN) Block User Guide	V02	S12MSCANV2/D
Voltage Regulator (VREG) Block User Guide	V01	S12VREGV1/D
Port Integration Module (PIM_9DP256) Block User Guide	V03	S12PIM9DP256V3/D
Oscillator (OSC) Block Guide	V02	S12OSCV2/D

Table 0-3 shows the Specification Change Summary for Maskset L91N.

Table 0-3 Specification Change Summary for Maskset L91N

Block	Spec Change
MCU_9DT256	removed CAN2 and CAN3
HCS12 V1.5	The Background Debug Module includes an Acknowledge Protocol (two additional hardware commands ACK_ENABLE/ACK_DISABLE)
HCS12 V1.5	The state of PK7/ROMCTL is latched into ROMON Bit during RESET into Emulation Mode or Normal Expanded Mode
CRG	Maskset includes an additional Pierce Oscillator

Table 1-1 Device Memory Map

Address	Module	Size (Bytes)
$1000 - $3FFF	RAM array	12288
$4000 - $7FFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at start	16384
$8000 - $BFFF	Flash EEPROM Page Window	16384
$C000 - $FFFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at end and 256 bytes of Vector Space at $FF80 - $FFFF	16384

$001E - $001E MEBI map 2 of 3 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001E	INTCR	Read:	IRQE	IRQEN	0	0	0	0	0	0
		Write:								

$001F - $001F INT map 2 of 2 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001F	HPRIO	Read:	PSEL7	PSEL6	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0
		Write:								

$0020 - $0027 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0020	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0021	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0022	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0023	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0024	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0025	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0026	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0027	Reserved	Read	0	0	0	0	0	0	0	0
		Write:								

$0028 - $002F BKP (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0028	BKPCT0	Read:	BKEN	BKFULL	BKBDM	BKTAG	0	0	0	0
		Write:								
$0029	BKPCT1	Read:	BK0MBH	BK0MBL	BK1MBH	BK1MBL	BK0RWE	BK0RW	BK1RWE	BK1RW
		Write:								
$002A	BKP0X	Read:	0	0	BK0V5	BK0V4	BK0V3	BK0V2	BK0V1	BK0V0
		Write:								
$002B	BKP0H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$002C	BKP0L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0040 - $007F ECT (Enhanced Capture Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0053	TC1 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0054	TC2 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0055	TC2 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0056	TC3 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0057	TC3 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0058	TC4 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0059	TC4 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$005A	TC5 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$005B	TC5 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$005C	TC6 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$005D	TC6 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$005E	TC7 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$005F	TC7 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0060	PACTL	Read: Write:	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
$0061	PAFLG	Read: Write:	0	0	0	0	0	0	PAOVF	PAIF
$0062	PACN3 (hi)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0063	PACN2 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0064	PACN1 (hi)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0065	PACN0 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0066	MCCTL	Read: Write:	MCZI	MODMC	RDMCL	0 ICLAT	0 FLMC	MCEN	MCPR1	MCPR0
$0067	MCFLG	Read: Write:	MCZF	0	0	0	POLF3	POLF2	POLF1	POLF0
$0068	ICPAR	Read: Write:	0	0	0	0	PA3EN	PA2EN	PA1EN	PA0EN
$0069	DLYCT	Read: Write:	0	0	0	0	0	0	DLY1	DLY0
$006A	ICOVW	Read: Write:	NOVW7	NOVW6	NOVW5	NOVW4	NOVW3	NOVW2	NOVW1	NOVW0
$006B	ICSYS	Read: Write:	SH37	SH26	SH15	SH04	TFMOD	PACMX	BUFEN	LATQ

$0040 - $007F ECT (Enhanced Capture Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$006C	Reserved	Read:								
		Write:								
$006D	TIMTST Test Only	Read:	0	0	0	0	0	0	TCBYP	0
		Write:								
$006E	Reserved	Read:								
		Write:								
$006F	Reserved	Read:								
		Write:								
$0070	PBCTL	Read:	0	PBEN	0	0	0	0	PBOVI	0
		Write:								
$0071	PBFLG	Read:	0	0	0	0	0	0	PBOVF	0
		Write:								
$0072	PA3H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0073	PA2H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0074	PA1H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0075	PA0H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0076	MCCNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0077	MCCNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0078	TC0H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0079	TC0H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$007A	TC1H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$007B	TC1H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$007C	TC2H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$007D	TC2H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$007E	TC3H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$007F	TC3H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0080 - $009F ATD0 (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0080	ATD0CTL0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0081	ATD0CTL1	Read:	0	0	0	0	0	0	0	0
		Write:								

Pin Name Funct. 1	Pin Name Funct. 2	Pin Name Funct. 3	Pin Name Funct. 4	Pin Name Funct. 5	Power Supply	Internal Pull Resistor		Description
						CTRL	Reset State	
EXTAL	—	—	—	—	VDDPLL	NA	NA	Oscillator Pins
XTAL	—	—	—	—	VDDPLL	NA	NA	
$\overline{\text{RESET}}$	—	—	—	—	VDDR	None	None	External Reset
TEST	—	—	—	—	N.A.	NA	NA	Test Input
VREGEN	—	—	—	—	VDDX	NA	NA	Voltage Regulator Enable Input
XFC	—	—	—	—	VDDPLL	NA	NA	PLL Loop Filter
BKGD	$\overline{\text{TAGHI}}$	MODC	—	—	VDDR	Always Up	Up	Background Debug, Tag High, Mode Input
PAD[15]	**AN1[7]**	**ETRIG1**	**—**	**—**	**VDDA**	**None**	**None**	**Port AD Input, Analog Input AN7 of ATD1, External Trigger Input of ATD1**
PAD[14:8]	**AN1[6:0]**	**—**	**—**	**—**	**VDDA**	**None**	**None**	**Port AD Inputs, Analog Inputs AN[6:0] of ATD1**
PAD[7]	AN0[7]	ETRIG0	—	—	VDDA	None	None	Port AD Input, Analog Input AN7 of ATD0, External Trigger Input of ATD0
PAD[6:0]	AN0[6:0]	—	—	—	VDDA	None	None	Port AD Inputs, Analog Inputs AN[6:0] of ATD0
PA[7:0]	ADDR[15:8]/ DATA[15:8]	—	—	—	VDDR	PUCR	Disabled	Port A I/O, Multiplexed Address/Data
PB[7:0]	ADDR[7:0]/ DATA[7:0]	—	—	—	VDDR	PUCR	Disabled	Port B I/O, Multiplexed Address/Data
PE7	NOACC	$\overline{\text{XCLKS}}$	—	—	VDDR	PUCR	Up	Port E I/O, Access, Clock Select
PE6	IPIPE1	MODB	—	—	VDDR	While $\overline{\text{RESET}}$ pin is low: Down		Port E I/O, Pipe Status, Mode Input
PE5	IPIPE0	MODA	—	—	VDDR	While RESET pin is low: Down		Port E I/O, Pipe Status, Mode Input
PE4	ECLK	—	—	—	VDDR	PUCR	Up	Port E I/O, Bus Clock Output
PE3	$\overline{\text{LSTRB}}$	$\overline{\text{TAGLO}}$	—	—	VDDR	PUCR	Up	Port E I/O, Byte Strobe, Tag Low
PE2	R/$\overline{\text{W}}$	—	—	—	VDDR	PUCR	Up	Port E I/O, R/$\overline{\text{W}}$ in expanded modes
PE1	$\overline{\text{IRQ}}$	—	—	—	VDDR	PUCR	Up	Port E Input, Maskable Interrupt
PE0	$\overline{\text{XIRQ}}$	—	—	—	VDDR	PUCR	Up	Port E Input, Non Maskable Interrupt
PH7	**KWH7**	**$\overline{\text{SS2}}$**	**—**	**—**	**VDDR**	**PERH/ PPSH**	**Disabled**	**Port H I/O, Interrupt, $\overline{\text{SS}}$ of SPI2**
PH6	**KWH6**	**SCK2**	**—**	**—**	**VDDR**	**PERH/ PPSH**	**Disabled**	**Port H I/O, Interrupt, SCK of SPI2**
PH5	**KWH5**	**MOSI2**	**—**	**—**	**VDDR**	**PERH/ PPSH**	**Disabled**	**Port H I/O, Interrupt, MOSI of SPI2**

Mnemonic	Pin Number 112-pin QFP	Nominal Voltage	Description
V_{DDPLL}	43	2.5 V	Provides operating voltage and ground for the Phased-Locked Loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator.
V_{SSPLL}	45	0 V	
VREGEN	97	5V	Internal Voltage Regulator enable/disable

2.4.7 VREGEN — On Chip Voltage Regulator Enable

Enables the internal 5V to 2.5V voltage regulator. If this pin is tied low, VDD1,2 and VDDPLL must be supplied externally.

specifies results in an error of less than 1/2 LSB (2.5mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance is allowed.

A.2.2.2 Source Capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage ≤ 1LSB, then the external filter capacitor, $C_f \geq 1024 * (C_{INS} - C_{INN})$.

A.2.2.3 Current Injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of $3FF ($FF in 8-bit mode) for analog inputs greater than V_{RH} and $000 for values less than V_{RL} unless the current is higher than specified as disruptive condition.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.
   The additional input voltage error on the converted channel can be calculated as $V_{ERR} = K * R_S * I_{INJ}$, with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Table A-9 ATD Electrical Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	C	Max input Source Resistance	R_S	-	-	1	KΩ
2	T	Total Input Capacitance Non Sampling Sampling	 C_{INN} C_{INS}			 10 22	pF
3	C	Disruptive Analog Input Current	I_{NA}	-2.5		2.5	mA
4	C	Coupling Ratio positive current injection	K_p			10^{-4}	A/A
5	C	Coupling Ratio negative current injection	K_n			10^{-2}	A/A

A.3.1.3 Sector Erase

Erasing a 512 byte Flash sector or a 4 byte EEPROM sector takes:

$$t_{era} \approx 4000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.3.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.3.1.5 Blank Check

The time it takes to perform a blank check on the Flash or EEPROM is dependant on the **location** of the first non-blank word starting at relative address zero. It takes one bus cycle per word to verify plus a setup of the command.

$$t_{check} \approx location \cdot t_{cyc} + 10 \cdot t_{cyc}$$

Table A-11 NVM Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	External Oscillator Clock (MC9S12DT256C< V, M)	f_{NVMOSC}	0.5		50 [1]	MHz
2	D	Bus frequency for Programming or Erase Operations	f_{NVMBUS}	1			MHz
3	D	Operating Frequency	f_{NVMOP}	150		200	kHz
4	P	Single Word Programming Time	t_{swpgm}	46 [2]		74.5 [3]	µs
5	D	Flash Burst Programming consecutive word [4]	t_{bwpgm}	20.4 [2]		31 [3]	µs
6	D	Flash Burst Programming Time for 32 Words [4]	t_{brpgm}	678.4 [2]		1035.5 [3]	µs
7	P	Sector Erase Time	t_{era}	20 [5]		26.7 [3]	ms
8	P	Mass Erase Time	t_{mass}	100 [5]		133 [3]	ms
9	D	Blank Check Time Flash per block	t_{check}	11 [6]		32778 [7]	t_{cyc}
10	D	Blank Check Time EEPROM per block	t_{check}	11 [6]		2058 [7]	t_{cyc}

NOTES:
1. Restrictions for oscillator in crystal mode apply!
2. Minimum Programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus}.

3. Maximum Erase and Programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f_{bus}. Refer to formulae in Sections **A.3.1.1 - A.3.1.4** for guidance.
4. Burst Programming operations are not applicable to EEPROM
5. Minimum Erase times are achieved under maximum NVM operating frequency f_{NVMOP}.
6. Minimum time, if first word in the array is not blank
7. Maximum time to complete check on an erased block

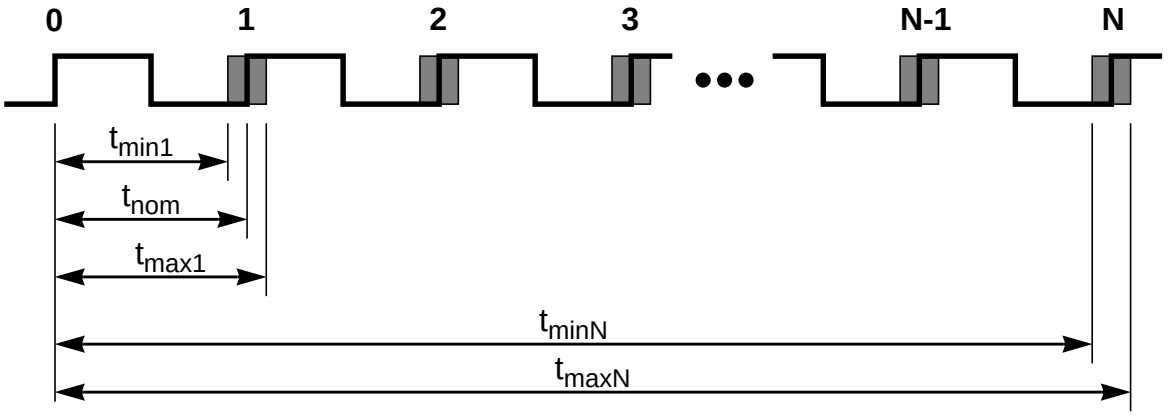


Figure A-4 Jitter Definitions

The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

For N < 100, the following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N}} + j_2$$

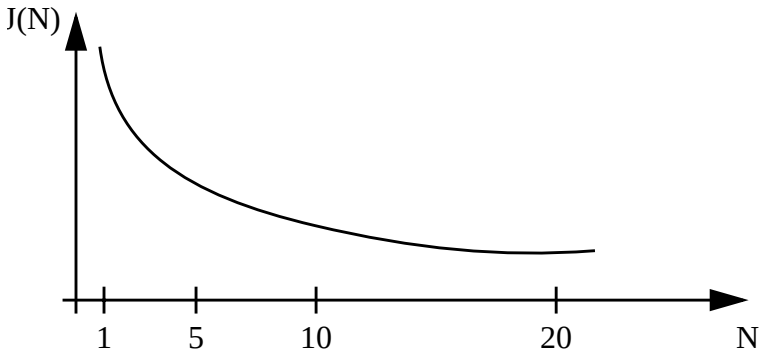


Figure A-5 Maximum bus clock jitter approximation

A.6 MSCAN

Table A-17 MSCAN Wake-up Pulse Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	MSCAN Wake-up dominant pulse filtered	t_{WUP}			2	µs
2	P	MSCAN Wake-up dominant pulse pass	t_{WUP}	5			µs

A.7 SPI

This section provides electrical parametrics and ratings for the SPI.

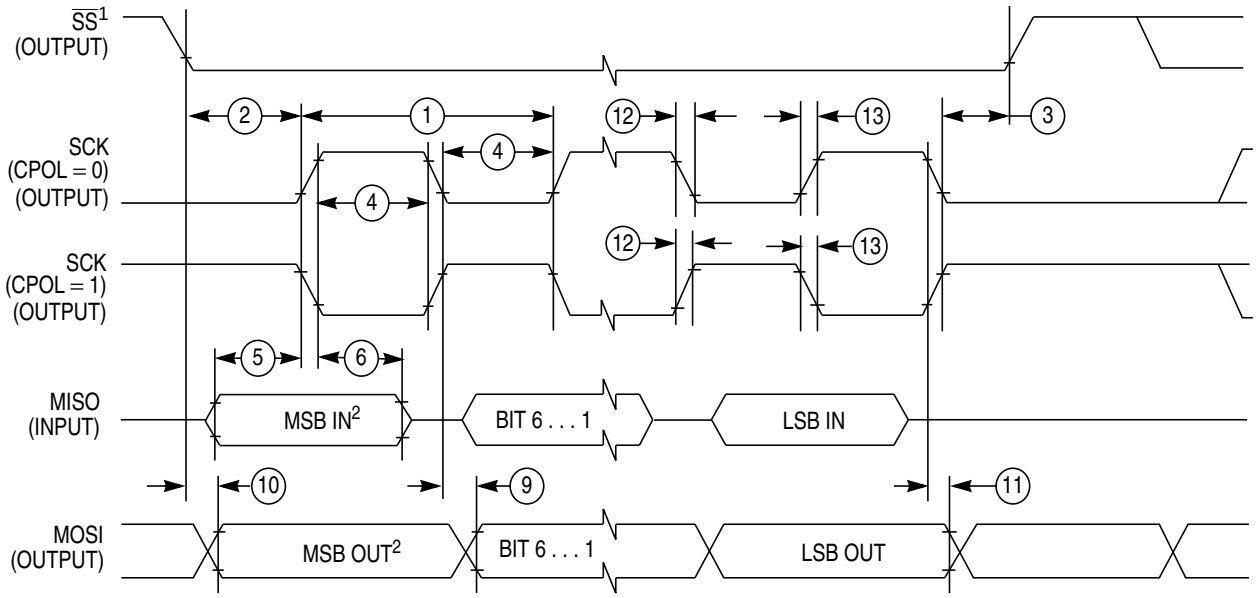
In **Table A-18** the measurement conditions are listed.

Table A-18 Measurement Conditions

Description	Value	Unit
Drive mode	full drive mode	—
Load capacitance C_{LOAD}, on all outputs	50	pF
Thresholds for delay measurement points	(20% / 80%) VDDX	V

A.7.1 Master Mode

In **Figure A-6** the timing diagram for master mode with transmission format CPHA=0 is depicted.



1.if configured as an output.

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-6 SPI Master Timing (CPHA=0)

In **Figure A-7** the timing diagram for master mode with transmission format CPHA=1 is depicted.

A.7.2 Slave Mode

In **Figure A-8** the timing diagram for slave mode with transmission format CPHA=0 is depicted.

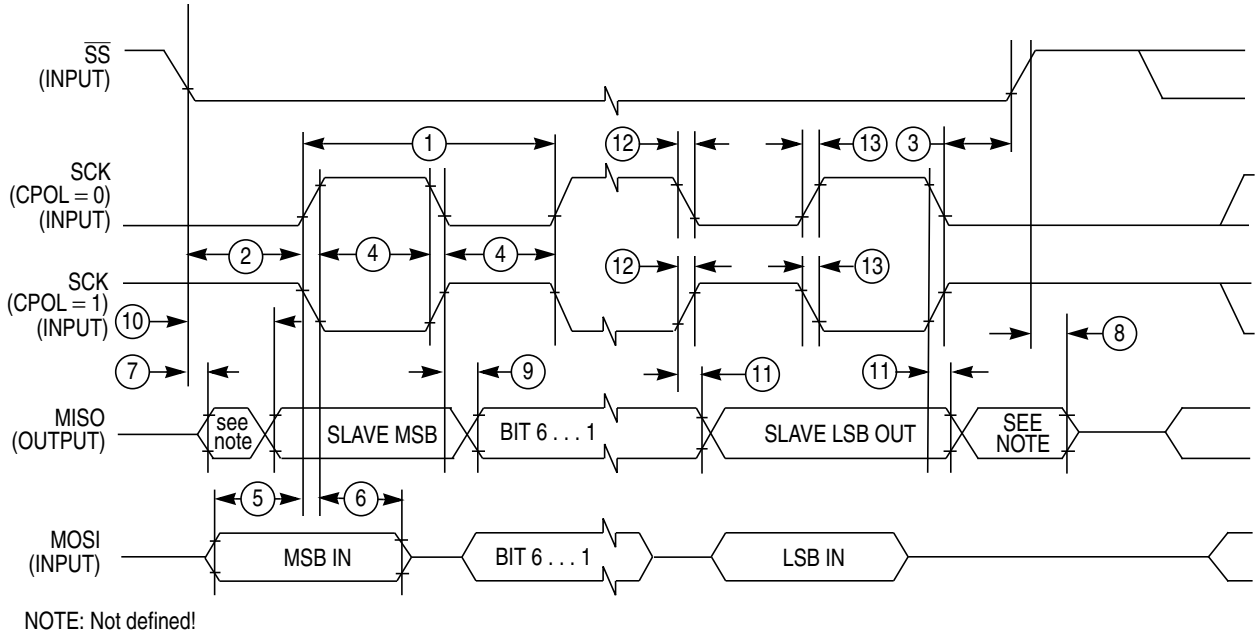


Figure A-8 SPI Slave Timing (CPHA=0)

In **Figure A-9** the timing diagram for slave mode with transmission format CPHA=1 is depicted.

Table A-21 Expanded Bus Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted, C_{LOAD} = 50pF							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Frequency of operation (E-clock)	f_o	0		25.0	MHz
2	P	Cycle time	t_{cyc}	40			ns
3	D	Pulse width, E low	PW_{EL}	19			ns
4	D	Pulse width, E high[1]	PW_{EH}	19			ns
5	D	Address delay time	t_{AD}			8	ns
6	D	Address valid time to E rise (PW_{EL}–t_{AD})	t_{AV}	11			ns
7	D	Muxed address hold time	t_{MAH}	2			ns
8	D	Address hold to data valid	t_{AHDS}	7			ns
9	D	Data hold to address	t_{DHA}	2			ns
10	D	Read data setup time	t_{DSR}	13			ns
11	D	Read data hold time	t_{DHR}	0			ns
12	D	Write data delay time	t_{DDW}			7	ns
13	D	Write data hold time	t_{DHW}	2			ns
14	D	Write data setup time[1] (PW_{EH}–t_{DDW})	t_{DSW}	12			ns
15	D	Address access time[1] (t_{cyc}–t_{AD}–t_{DSR})	t_{ACCA}	19			ns
16	D	E high access time[1] (PW_{EH}–t_{DSR})	t_{ACCE}	6			ns
17	D	Non-multiplexed address delay time	t_{NAD}			6	ns
18	D	Non-muxed address valid to E rise (PW_{EL}–t_{NAD})	t_{NAV}	15			ns
19	D	Non-multiplexed address hold time	t_{NAH}	2			ns
20	D	Chip select delay time	t_{CSD}			16	ns
21	D	Chip select access time[1] (t_{cyc}–t_{CSD}–t_{DSR})	t_{ACCS}	11			ns
22	D	Chip select hold time	t_{CSH}	2			ns
23	D	Chip select negated time	t_{CSN}	8			ns
24	D	Read/write delay time	t_{RWD}			7	ns
25	D	Read/write valid time to E rise (PW_{EL}–t_{RWD})	t_{RWV}	14			ns
26	D	Read/write hold time	t_{RWH}	2			ns
27	D	Low strobe delay time	t_{LSD}			7	ns
28	D	Low strobe valid time to E rise (PW_{EL}–t_{LSD})	t_{LSV}	14			ns
29	D	Low strobe hold time	t_{LSH}	2			ns
30	D	NOACC strobe delay time	t_{NOD}			7	ns
31	D	NOACC valid time to E rise (PW_{EL}–t_{NOD})	t_{NOV}	14			ns

FINAL PAGE OF
132
PAGES