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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SPI
Peripherals	LCD, POR, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	EPROM, UV
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705l5fue

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Section 2. Memory Map

2.1 Contents

Section 3. Central Processor Unit (CPU)

3.1 Contents

3.2 Introduction

This section describes the central processor unit (CPU).

4.3 Interrupts

There are six hardware interrupt sources in the MC68HC05L5:

- $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$
- Key wakeup interrupt ($\overline{\text{KWI}}$)
- Timer 1 (TOI, ICI, and OC1I)
- Timer 2 (TI2I and OC2I)
- Serial transfer complete interrupt (SSPI)
- Timebase interrupt (TBI)

4.3.1 $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$

Two external interrupt request inputs, $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$, share the same vector address at $3FFA and $3FFB.

Bits IRQ1S and IRQ2S in interrupt control register (INTCR) control whether $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$, respectively, respond only to the falling edge or falling edge and low level to trigger an interrupt. The $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$ are enabled by IRQ1E and IRQ2E bits and IRQ1F and IRQ2F bits are provided as an indicator in the interrupt status register (INTSR). Since the IRQ1(2)F can be set by either the pins or the data latches of PC7(6), be sure to clear the flags by software before setting the IRQ1(2)E bit.

The $\overline{\text{IRQ1}}$ and the $\overline{\text{IRQ2}}$ pins are shared with port C bit 7 and bit 6, respectively, and IRQ*x* pin states can be determined by reading port C pins. The BIL and BIH instructions apply only to the $\overline{\text{IRQ1}}$ input.

4.3.2 Key Wakeup Interrupt ($\overline{\text{KWI}}$)

Eight key wakeup inputs ($\overline{\text{KWI0}}$–$\overline{\text{KWI7}}$) share pins with port B. Each key wakeup input is enabled by the corresponding bit in the KWIEN register which resides in the option map, and $\overline{\text{KWI}}$ is enabled by the KWIE bit in the INTCR. When a falling edge is detected at one of the enabled key wakeup inputs, the KWIF bit in the INTSR is set and $\overline{\text{KWI}}$ is generated if KWIE = 1. Each input has a latch which responds only to the falling edge at the pin, and all input latches are cleared at the same time by clearing the KWIF bit. See **Figure 4-6**.

4.3.3 IRQ (KWI) Software Consideration

IRQ and KWI interrupts have a timing delay in a case described in **Figure 4-2**. This section shows programming for proper interrupts with IRQ or KWI.

Figure 4-1 shows an example of timer 1 interrupt. In this case, the interrupt by TOF occurs as soon as the TOIE (timer 1 overflow interrupt enable) bit is set.

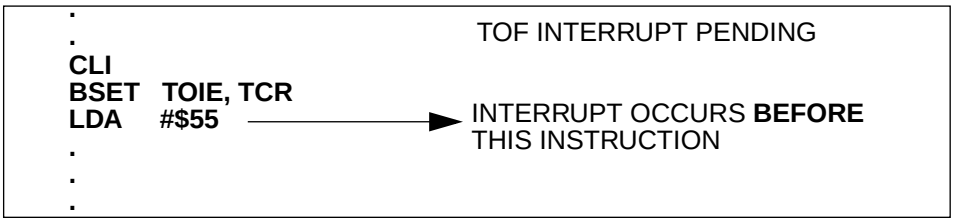


Figure 4-1. Timer 1 Interrupt

Figure 4-2 shows an example of $\overline{\text{IRQ1}}$ interrupt. In this case, the interrupt occurs **after** execution the instruction following the instruction which sets IRQ1E bit. The similar action occurs against $\overline{\text{IRQ2}}$ and $\overline{\text{KWI}}$ interrupts.

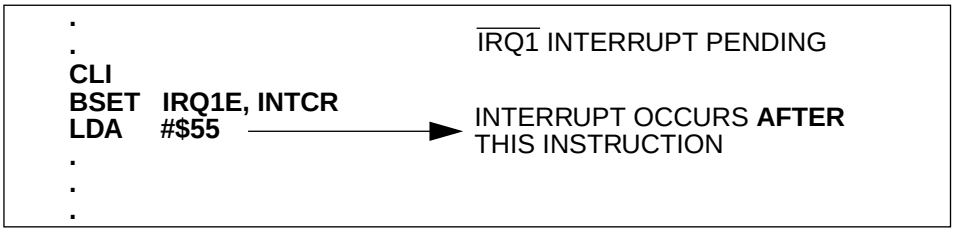


Figure 4-2. IRQ Timing Delay

This problem can be solved by using a software patch like **Figure 4-3**. A similar procedure could be used for $\overline{\text{IRQ2}}$ or $\overline{\text{KWI}}$.

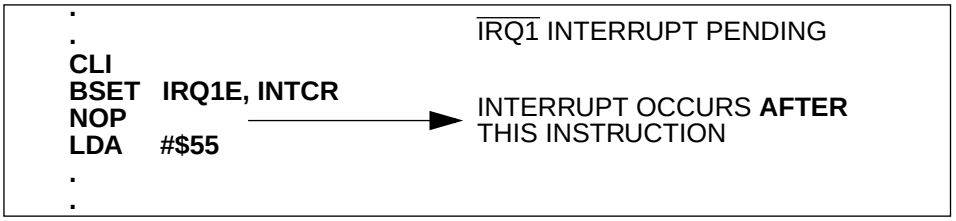


Figure 4-3. Software Patch for $\overline{\text{IRQ1}}$

IRQ1E — IRQ1 Interrupt Enable

The IRQ1E bit enables IRQ1 interrupt when IRQ1F is set. This bit is cleared on reset.

0 = IRQ1 interrupt disabled
1 = IRQ1 interrupt enabled

IRQ2E — IRQ2 Interrupt Enable

The IRQ2E bit enables IRQ2 interrupt when IRQ2F is set. This bit is cleared on reset.

0 = IRQ2 interrupt disabled
1 = IRQ2 interrupt enabled

Bit 5 — Reserved

This bit is not used and is always read as logic 0.

KWIE — Key Wakeup Interrupt (KWI) Enable

The KWIE bit enables key wakeup interrupt when KWIF is set. This bit is cleared on reset.

0 = KWI disabled
1 = KWI enabled

IRQ1S — IRQ1 Select Edge Sensitive Only

0 = IRQ1 configured for low level and negative edge sensitive
1 = IRQ1 configured to respond only to negative edges

IRQ2S — IRQ2 Select Edge Sensitive Only

0 = IRQ2 configured for low level and negative edge sensitive
1 = IRQ2 configured to respond only to negative edges

Bits 1 and 0 — Reserved

These bits are not used and always read as logic 0.

Section 5. Low-Power Modes

5.1 Contents

5.2 Introduction

The MCU has two power-saving modes, stop and wait. Flowcharts of these modes are shown in **Figure 5-2**.

5.3 Stop Mode

The STOP instruction places the MCU in its lowest-power mode. In stop mode, the internal main oscillator OSC is turned off, halting all internal processing, including timer operations (timer 1, timer 2, and computer operating properly (COP) watchdog timer. Suboscillator XOSC does not stop oscillating. Therefore, if XOSC is used as the clock source for the COP watchdog timer, COP is still functional in stop mode. See **Section 7. Oscillators/Clock Distributions.**

During stop mode, the timer prescaler is cleared. The I bit in the condition code register (CCR) is cleared to enable external interrupts. All other registers and memory remain unaltered. All input/output lines remain unchanged. The processor can be brought out of stop mode only by $\overline{\text{RESET}}$ or an interrupt from $\overline{\text{IRQ1}}$, $\overline{\text{IRQ2}}$, $\overline{\text{KWI}}$, SSPI (slave mode only), or TBI. See **Section 7. Oscillators/Clock Distributions.**

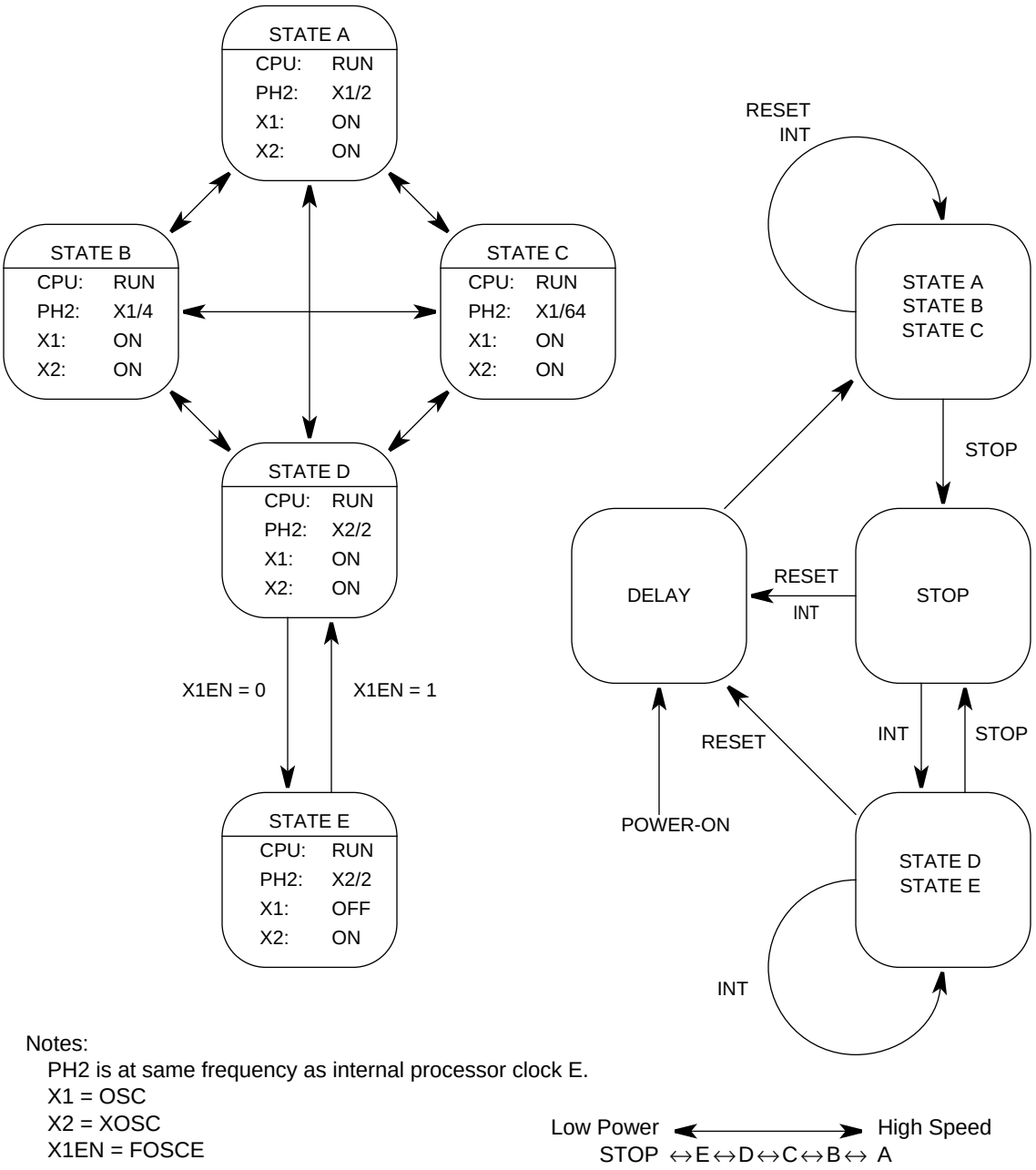


Figure 5-1. Clock State and STOP Recovery/Power-On Reset Delay Diagrams

6.2 Introduction

The MCU has five parallel ports:

- Port A has eight input/output (I/O) pins.
- Port B has eight input-only pins.
- Port C has six I/O pins and tow input-only pins.
- Port D has seven output-only pins.
- Port E has eight output-only pins.

Most of these 39 I/O pins serve multiple purposes, depending on the configuration of the MCU system. The configuration is in turn controlled by hardware mode selection as well as internal control registers.

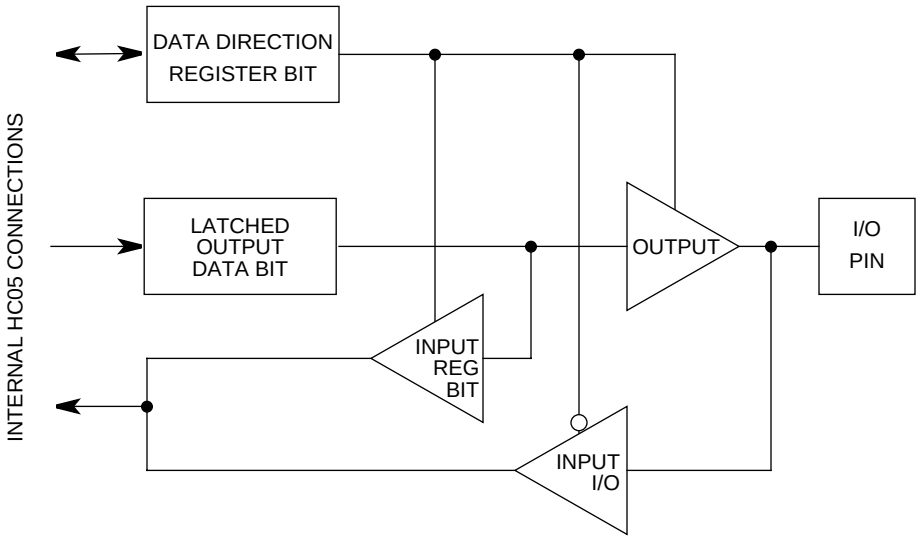


Figure 6-1. Port I/O Circuitry for One Bit

6.3.1 Port A Data Register

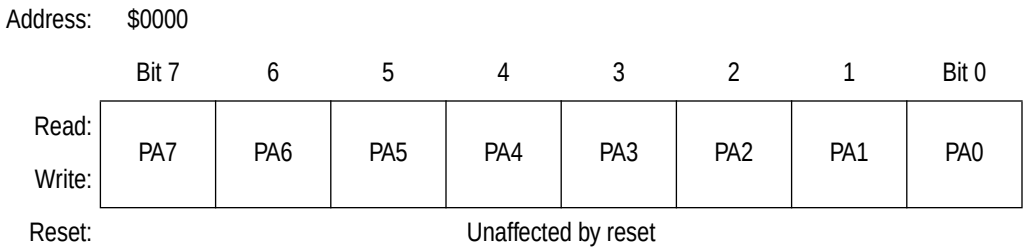


Figure 6-2. Port A Data Register (PORTA)

Read

Anytime; returns pin level if DDR set to input; returns output data latch if DDR set to output

Write

Anytime; data stored in an internal latch; drives pin only if DDR set for output

Reset

Becomes high-impedance inputs

6.3.2 Port A Data Direction Register

Address: Option Map — $0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
Reset:	0	0	0	0	0	0	0	0

Figure 6-3. Port A Data Direction Register (DDRA)

Read

Anytime when OPTM = 1

Write

Anytime when OPTM = 1

Reset

Cleared to $00; all general-purpose I/O configured for input

DDRA*x* — Port A Data Direction Register Bit *x*

0 = Configure I/O pin PA*x* to input

1 = Configure I/O pin PA*x* to output

6.5.1 Port C Data Register

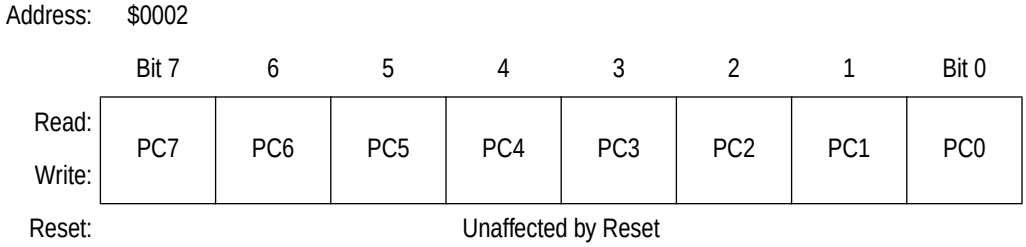


Figure 6-5. Port C Data Register (PORTC)

Read

Anytime; returns pin level if DDR set to input; returns output data latch if DDR set to output, PC7 and PC6 are input-only pins

Write

Anytime; data stored in an internal latch; drives pin only if DDR set for output; writes do not change pin state; when pin configured for SDO, SCK, and EVO peripheral output, bits 7 and 6 are read-only bits and write has no effect

Reset

Becomes high-impedance input

The 7-bit divider and POR counter are initialized to $0078 by two conditions:

- Power-on detection
- When FOSCE bit is cleared

7.4 System Clock Control

The system clock is provided for all internal modules except timebase. Both OSC and XOSC are available as the system clock source. The divide ratio is selected by the SYS1 and SYS0 bits in the MISC register. (See **Table 7-1**.)

By default, OSC divided by 64 is selected on reset.

NOTE: *Do not switch the system clock to XOSC (SYS1 and SYS0 = 11) when XOSC clock is not available. The XOSC clock is available when STUP flag is set.*

Do not switch the system clock to OSC (SYS1 and SYS0 = 00, 01, or 10) when OSC clock is not available. The OSC clock is available when FTUP flag is set.

Table 7-1. System Bus Clock Frequency Selection

SYS1	SYS0	Divide Ratio	CPU Bus Frequency (Hz)		
			OSC = 4.0 M	OSC = 4.1943 M	XOSC = 32.768 k
0	0	OSC ÷ 2	2.0 M	2.0972 M	—
0	1	OSC ÷ 4	1.0 M	1.0486 M	—
1	0	OSC ÷ 64	62.5 k	65.536 k	—
1	1	XOSC ÷ 2	—	—	16.384 k

7.6.4 COP

The computer operating properly (COP) watchdog timer is controlled by the COPE and COPC bits in the TBCR2 register.

The COP uses the same clock as TBI that is selected by the TBR1 and TBR0 bits. The TBI is divided by four and overflow of this divider generates COP timeout reset if the COP enable (COPE) bit is set. The COP timeout reset has the same vector address as POR and external $\overline{\text{RESET}}$. To prevent the COP timeout, the COP divider is cleared by writing a logic 1 to the COP clear (COPC) bit.

When the timebase divider is driven by the OSC clock, clock for the divider is suspended during stop mode or when FOSCE is a logic 0. This may cause COP period stretching or no COP timeout reset when processing errors occur. To avoid these problems, it is recommended that the XOSC clock be used for the COP functions.

When the timebase (COP) divider is driven by the XOSC clock, the divider does not stop counting and the COPC bit must be triggered to prevent the COP timeout.

Table 7-4. COP Timeout Period

TBCR2		COP Period (ms)					
TBR1	TBR0	OSC = 4.0 MHz		OSC = 4.1943 MHz		XOSC = 32.768 kHz	
		Min	Max	Min	Max	Min	Max
0	0	12.3	16.4	11.7	15.6	11.7	15.6
0	1	393	524	375	500	375	500
1	0	786	1048	750	1000	750	1000
1	1	1573	2097	1500	2000	1500	2000

11.4.1 Register/Memory Instructions

These instructions operate on CPU registers and memory locations. Most of them use two operands. One operand is in either the accumulator or the index register. The CPU finds the other operand in memory.

Table 11-1. Register/Memory Instructions

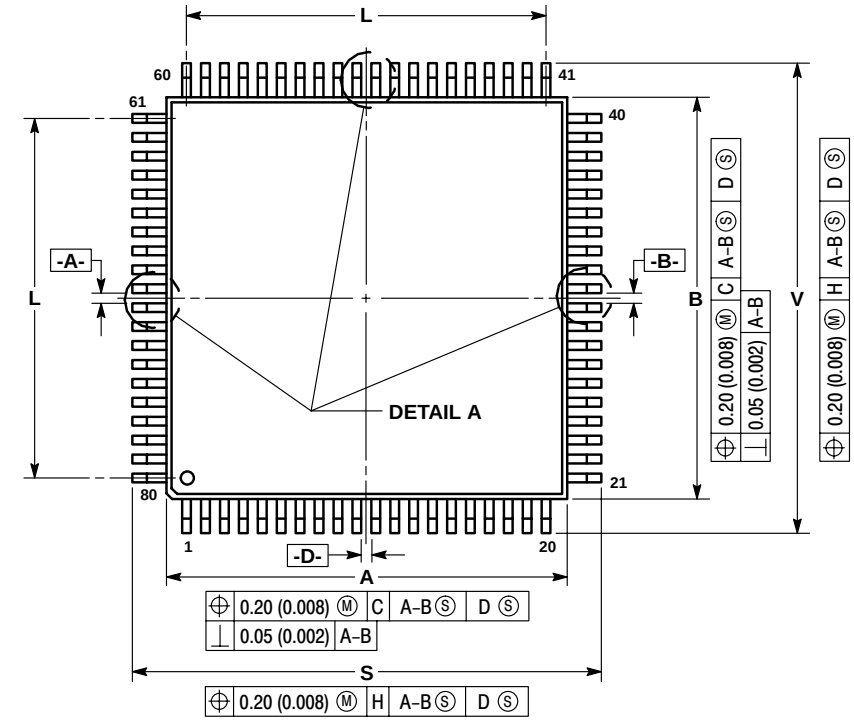
Instruction	Mnemonic
Add Memory Byte and Carry Bit to Accumulator	ADC
Add Memory Byte to Accumulator	ADD
AND Memory Byte with Accumulator	AND
Bit Test Accumulator	BIT
Compare Accumulator	CMP
Compare Index Register with Memory Byte	CPX
EXCLUSIVE OR Accumulator with Memory Byte	EOR
Load Accumulator with Memory Byte	LDA
Load Index Register with Memory Byte	LDX
Multiply	MUL
OR Accumulator with Memory Byte	ORA
Subtract Memory Byte and Carry Bit from Accumulator	SBC
Store Accumulator in Memory	STA
Store Index Register in Memory	STX
Subtract Memory Byte from Accumulator	SUB

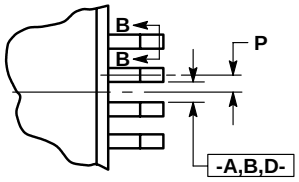
12.10 Control Timing

Characteristic[1]	Symbol	Min	Max	Unit
Frequency of oscillation (OSC) Crystal External clock	f_{osc}	 — dc	 4.2 4.2	MHz
Internal operating frequency[2], crystal or external clock (f_{OSC}/2) V_{DD} = 4.5 V to 5.5 V V_{DD} = 2.2 V to 5.5 V	f_{op}	 — —	 2.1 1.0	MHz
Cycle time (fast OSC selected) V_{DD} = 4.5 V to 5.5 V V_{DD} = 2.2 V to 5.5 V	t_{cyc}	 480 1.0	 — —	 ns µs
$\overline{\text{RESET}}$ pulse width when bus clock active	t_{RL}	1.5	—	t_{cyc}
Timer Resolution Input capture (TCAP) pulse width	 t_{RESL} t_{TH}, t_{TL}	 4.0 284	 — —	 t_{cyc} ns
Interrupt pulse width low (edge-triggered)	t_{ILIH}	284	—	ns
Interrupt pulse period[3]	t_{ILIL}	note 3	—	t_{cyc}
OSC1 pulse width (external clock input)	t_{OH}, t_{OL}	110	—	ns

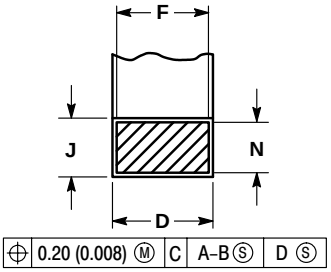
1. +2.2 ≤ V_{DD} ≤ +5.5 Vdc, V_{SS} = 0 Vdc, $T_L \le T_A \le T_H$, unless otherwise noted.
2. The system clock divider configuration (SYS1–SYS0 bits) should be selected such that the internal operating frequency (f_{OP}) does not exceed value specified in f_{OP} for a given f_{OSC}.
3. The minimum period, t_{ILIL}, should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}.

13.3 Quad Flat Pack (QFP) — Case 841B-01

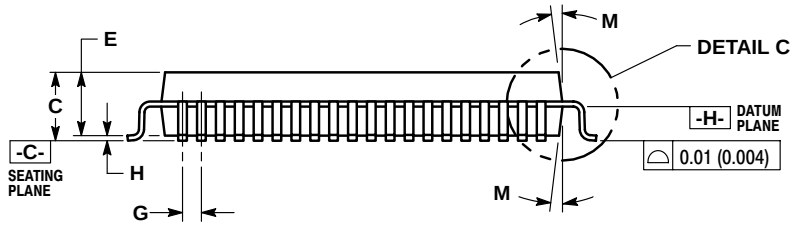


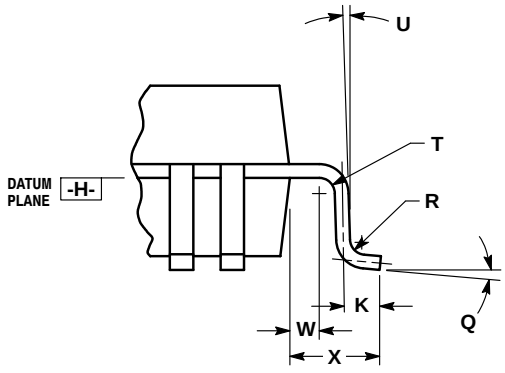


DETAIL A



SECTION B-B





DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	13.90	14.10	0.547	0.555
B	13.90	14.10	0.547	0.555
C	2.15	2.45	0.084	0.096
D	0.22	0.38	0.009	0.015
E	2.00	2.40	0.079	0.094
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	12.35 BSC		0.486 BSC	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
P	0.325 BSC		0.013 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	16.95	17.45	0.667	0.687
T	0.13	—	0.005	—
U	0°	—	0°	—
V	16.95	17.45	0.667	0.687
W	0.35	0.45	0.014	0.018
X	1.6 REF		0.06 REF	

The current MCU ordering form is also available through the Motorola Freeware Bulletin Board Service (BBS). The telephone number is (512) 891-FREE. After making the connection, type bbs in lowercase letters. Then press the return key to start the BBS software.

14.4 Application Program Media

Please deliver the application program to Motorola in one of the following media:

- Macintosh®[1] 3 1/2-inch diskette (double-sided 800 K or double-sided high-density 1.4 M)
- MS-DOS®[2] or PC-DOS™[3] 3 1/2-inch diskette (double-sided 720 K or double-sided high-density 1.44 M)
- MS-DOS® or PC-DOS™ 5 1/4-inch diskette (double-sided double-density 360 K or double-sided high-density 1.2 M)

Use positive logic for data and addresses.

When submitting the application program on a diskette, clearly label the diskette with the following information:

- Customer name
- Customer part number
- Project or product name
- File name of object code
- Date
- Name of operating system that formatted diskette
- Formatted capacity of diskette

On diskettes, the application program must be in Motorola's S-record format (S1 and S9 records), a character-based object file format generated by M6805 cross assemblers and linkers.

1. Macintosh is a registered trademark of Apple Computer, Inc.
2. MS-DOS is a registered trademark of Microsoft Corporation.
3. PC-DOS is a trademark of International Business Machines Corporation.

A.7 Programming Voltage (V_{PP})

In single-chip (user) mode, the V_{PP} pin should be tied to V_{DD} level.

A.8 Modes of Operation

The MC68HC705L5 has two operating modes: single-chip mode (SCM) and bootstrap mode.

Single-chip mode, also called user mode, allows maximum use of pins for on-chip peripheral functions.

The bootstrap mode is provided for EPROM programming, dumping EPROM contents, and loading programs into the internal RAM and executing them. This is a very versatile mode because there are essentially no limitations on the special-purpose program that is boot-loaded into the internal RAM.

A.8.1 Mode Entry

Mode entry is done at the rising edge of the $\overline{\text{RESET}}$ pin. Once the device enters one of the modes, the mode cannot be changed by software. Only an external reset can change the mode.

At the rising edge of the $\overline{\text{RESET}}$ pin, the device latches the states of $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$ and places itself in the specified mode. While the $\overline{\text{RESET}}$ pin is low, all pins are configured as single-chip mode. **Table A-3** shows the states of $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$ for each mode entry.

High voltage $V_{TST} = 2 \times V_{DD}$ is required to select modes other than single-chip mode.

Table A-3. Mode Select Summary

Modes	$\overline{\text{RESET}}$	PC6/$\overline{\text{IRQ1}}$	PC7/$\overline{\text{IRQ2}}$
Single-chip (user) mode	↑	V_{SS} or V_{DD}	V_{SS} or V_{DD}
Boot-strap mode		V_{TST}	V_{DD}

A.14.2 Operating Temperature Range

Characteristic	Symbol	Value	Unit
Operating temperature range MC68HC705L5 (standard)	T_A	T_L to T_H 0 to +70	°C

A.14.3 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance 80-pin plastic quad flat pack	θ_{JA}	120	°C/W

A.15 Recommended Operating Conditions

Rating[1]	Symbol	Min	Typ	Max	Unit
(f_{OP} = 2.1 MHz)	V_{DD}	4.5	5.0	5.5	V
(f_{OP} = 1.0 MHz)	V_{DD}	3.0	—	5.5	V
Supply voltage	V_{LCD1}	V_{DD} – 1/3 V_{LCD}			V
	V_{LCD2}	V_{DD} – 2/3 V_{LCD}			V
	V_{LCD3}	V_{DD} – 3/3 V_{LCD}			V
Fast clock oscillation frequency	f_{OSC}	—	3.52	4.2	MHz
External capacitance (f_{OSC} = 3.52 MHz)	C1 C2	— —	33 33	— —	pF
Slow clock oscillation frequency	f_{XOSC}	—	32.768	—	MHz
External capacitance (f_{XOSC} = 32.768 kHz)	CX1 CX2	— —	18 22	— —	pF

1. +3.0 ≤ V_{DD} ≤ +5.5 Vdc, V_{SS} = 0 Vdc, $T_L \le T_A \le T_H$, unless otherwise noted

A.15.1 EPROM Programming Voltage

Characteristics[1]	Symbol	Min	Typ	Max	Unit
EPROM programming voltage	V_{PP}	12.0	12.5	13.0	V

1. V_{DD} = 5.0 Vdc, V_{SS} = 0 Vdc, T_A = 25 °C