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XMOS - XS1-L8A-128-QF124-I10 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	XCore
Core Size	32-Bit 8-Core
Speed	1000MIPS
Connectivity	Configurable
Peripherals	-
Number of I/O	84
Program Memory Size	128KB (32K x 32)
Program Memory Type	SRAM
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	0.95V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	124-TFQFN Dual Rows, Exposed Pad
Supplier Device Package	124-QFN DualRow (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/xmos/xs1-l8a-128-qf124-i10

Email: info@E-XFL.COM

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2 XS1-L8A-128-QF124 Features

► Multicore Microcontroller with Advanced Multi-Core RISC Architecture

- Eight real-time logical cores on 2 xCORE tiles
- Cores share up to 500 MIPS
- Each logical core has:
 - Guaranteed throughput of 1/4 of tile MIPS
 - 16x32bit dedicated registers
- 159 high-density 16/32-bit instructions
 - All have single clock-cycle execution (except for divide)
 - 32x32 \rightarrow 64-bit MAC instructions for DSP, arithmetic and user-definable cryptographic functions

Programmable I/O

- 28 general-purpose I/O pins, configurable as input or output
 - Up to 32 x 1 bit port, 12 x 4bit port, 7 x 8bit port, 3 x 16bit port
 4 xCONNECT links
- Port sampling rates of up to 60 MHz with respect to an external clock
- 64 channel ends for communication with other cores, on or off-chip

Memory

- 128KB internal single-cycle SRAM (max 64KB per tile) for code and data storage
- 8KB internal OTP (max 8KB per tile) for application boot code

Hardware resources

- 12 clock blocks (6 per tile)
- 20 timers (10 per tile)
- 8 locks (4 per tile)

► JTAG Module for On-Chip Debug

Security Features

• Programming lock disables debug and prevents read-back of memory contents

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• AES bootloader ensures secrecy of IP held on external flash memory

► Ambient Temperature Range

- Commercial qualification: 0°C to 70°C
- Industrial qualification: -40 °C to 85 °C

Speed Grade

- 10: 1000 MIPS
- 8: 800 MIPS
- Power Consumption
 - Active Mode
 - 400 mA at 500 MHz (typical)
 - 320 mA at 400 MHz (typical)
 - Standby Mode
 - 28 mA
- 124-pin QF124 package 0.5 mm pitch



3 Pin Configuration



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4 Signal Description

This section lists the signals and I/O pins available on the XS1-L8A-128-QF124. The device provides a combination of 1 bit, 4 bit, 8 bit and 16 bit ports, as well as wider ports that are fully or partially (gray) bonded out. All pins of a port provide either output or input, but signals in different directions cannot be mapped onto the same port.

Pins may have one or more of the following properties:

PD/PU: The IO pin a weak pull-down or pull-up resistor. On GPIO pins this resistor can be enabled.

Power pins (6)									
Signal	Function	Туре	Properties						
GND	Digital ground	GND							
OTP_VCC	OTP power supply	PWR							
PLL_AGND	Analog ground for PLL	GND							
PLL_AVDD	Analog PLL power	PWR							
VDD	Digital tile power	PWR							
VDDIO	Digital I/O power	PWR							

ST: The IO pin has a Schmitt Trigger on its input.

Clocks pins (2)										
Signal	Function	Туре	Properties							
CLK	PLL reference clock	Input	PD, ST							
MODE[4:0]	Boot mode select	Input	PU, ST							

JTAG pins (7)										
Signal	Function	Туре	Properties							
DEBUG_N	Multi-chip debug	I/O	PU							
RST_N	Global reset input	Input	PU, ST							
ТСК	Test clock	Input	PU, ST							
TDI	Test data input	Input	PU, ST							
TDO	Test data output	Output	PD, OT							
TMS	Test mode select	Input	PU, ST							
TRST_N	Test reset input	Input	PU, ST							

I/O pins (84)											
Signal	Function	Туре	Properties								
X0D00	1A ⁰	I/O	PD _S , R _S								



pins (5)									
Signal	Function	Туре	Properties						
PCU_CLK	Clock input								
PCU_GATE	Power control gate control								
PCU_VDD	PCU tile power								
PCU_VDDIO	PCU I/O supply								
PCU_WAKE	Wakeup reset								





Data is transferred between the pins and core using a FIFO that comprises a SERDES and transfer register, providing options for serialization and buffered data.

Each port has a 16-bit counter that can be used to control the time at which data is transferred between the port value and transfer register. The counter values can be obtained at any time to find out when data was obtained, or used to delay I/O until some time in the future. The port counter value is automatically saved as a timestamp, that can be used to provide precise control of response times.

The ports and xCONNECT links are multiplexed onto the physical pins. If an xConnect Link is enabled, the pins of the underlying ports are disabled. If a port is enabled, it overrules ports with higher widths that share the same pins. The pins on the wider port that are not shared remain available for use when the narrower port is enabled. Ports always operate at their specified width, even if they share pins with another port.

5.4 Clock blocks

xCORE devices include a set of programmable clocks called clock blocks that can be used to govern the rate at which ports execute. Each xCORE tile has six clock blocks: the first clock block provides the tile reference clock and runs at a default frequency of 100MHz; the remaining clock blocks can be set to run at different frequencies.

A clock block can use a 1-bit port as its clock source allowing external application clocks to be used to drive the input and output interfaces.

In many cases I/O signals are accompanied by strobing signals. The xCORE ports can input and interpret strobe (known as readyln and readyOut) signals generated by external sources, and ports can generate strobe signals to accompany output data.



Figure 5: Switch, links and channel ends

6 PLL

The PLL creates a high-speed clock that is used for the switch, tile, and reference clock.

The PLL multiplication value is selected through the two MODE pins, and can be changed by software to speed up the tile or use less power. The MODE pins are set as shown in Figure 6:

PLL v N

	Oscillator	MC	DDE	Tile	PLL Ratio	PLL	setting	gs
	Frequency	1	0	Frequency		OD	F	R
Figure 6:	5-13 MHz	0	0	130-399.75 MHz	30.75	1	122	0
multiplier	13-20 MHz	1	1	260-400.00 MHz	20	2	119	0
alues and	20-48 MHz	1	0	167-400.00 MHz	8.33	2	49	0
IODE pins	48-100 MHz	0	1	196-400.00 MHz	4	2	23	0

Figure 6 also lists the values of OD, F and R, which are the registers that define the ratio of the tile frequency to the oscillator frequency:

$$F_{core} = F_{osc} \times \frac{F+1}{2} \times \frac{1}{R+1} \times \frac{1}{OD+1}$$

OD, *F* and *R* must be chosen so that $0 \le R \le 63$, $0 \le F \le 4095$, $0 \le OD \le 7$, and $260MHz \le F_{osc} \times \frac{F+1}{2} \times \frac{1}{R+1} \le 1.3GHz$. The *OD*, *F*, and *R* values can be modified by writing to the digital node PLL configuration register.

The MODE pins must be held at a static value during and after deassertion of the system reset.

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If a different tile frequency is required (eg, 500 MHz), then the PLL must be reprogrammed after boot to provide the required tile frequency. The XMOS tools perform this operation by default. Further details on configuring the clock can be found in the XS1-L Clock Frequency Control document, X1433.

7 Boot Procedure

The device is kept in reset by driving RST_N low. When in reset, all GPIO pins are high impedance. When the device is taken out of reset by releasing RST_N the processor starts its internal reset process. After 15-150 μ s (depending on the input clock), all GPIO pins have their internal pull-resistor enabled, and the processor boots at a clock speed that depends on MODE0 and MODE1.

The xCORE Tile boot procedure is illustrated in Figure 7. In normal usage, MODE[4:2] controls the boot source according to the table in Figure 8. If bit 5 of the security register (*see* §8.1) is set, the device boots from OTP.



The boot image has the following format:

A 32-bit program size *s* in words.

- 2. Input a word on channel-end 0. It will use this word as a channel to acknowledge the boot. Provide the null-channel-end 0x0000FF02 if no acknowledgment is required.
- 3. Input the boot image specified above, including the CRC.
- 4. Input an END control token.
- 5. Output an END control token to the channel-end received in step 2.
- 6. Free channel-end 0.
- 7. Jump to the loaded code.

7.3 Boot from OTP

If an xCORE tile is set to use secure boot (see Figure 7), the boot image is read from address 0 of the OTP memory in the tile's security module.

This feature can be used to implement a secure bootloader which loads an encrypted image from external flash, decrypts and CRC checks it with the processor, and discontinues the boot process if the decryption or CRC check fails. XMOS provides a default secure bootloader that can be written to the OTP along with secret decryption keys.

Each tile has its own individual OTP memory, and hence some tiles can be booted from OTP while others are booted from SPI or the channel interface. This enables systems to be partially programmed, dedicating one or more tiles to perform a particular function, leaving the other tiles user-programmable.

7.4 Security register

The security register enables security features on the xCORE tile. The features shown in Figure 10 provide a strong level of protection and are sufficient for providing strong IP security.

8 Memory

8.1 OTP

Each xCORE Tile integrates 8 KB one-time programmable (OTP) memory along with a security register that configures system wide security features. The OTP holds data in four sectors each containing 512 rows of 32 bits which can be used to implement secure bootloaders and store encryption keys. Data for the security register is loaded from the OTP on power up. All additional data in OTP is copied from the OTP to SRAM and executed first on the processor.

The OTP memory is programmed using three special I/O ports: the OTP address port is a 16-bit port with resource ID 0x100200, the OTP data is written via a 32-bit

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The JTAG chain structure is illustrated in Figure 11. Directly after reset, two TAP controllers are present in the JTAG chain for each xCORE Tile: the boundary scan TAP and the chip TAP. The boundary scan TAP is a standard 1149.1 compliant TAP that can be used for boundary scan of the I/O pins. The chip TAP provides access into the xCORE Tile, switch and OTP for loading code and debugging.

The TRST_N pin must be asserted low during and after power up for 100 ns. If JTAG is not required, the TRST_N pin can be tied to ground to hold the JTAG module in reset.

The DEBUG_N pin is used to synchronize the debugging of multiple xCORE Tiles. This pin can operate in both output and input mode. In output mode and when configured to do so, DEBUG_N is driven low by the device when the processor hits a debug break point. Prior to this point the pin will be tri-stated. In input mode and when configured to do so, driving this pin low will put the xCORE Tile into debug mode. Software can set the behavior of the xCORE Tile based on this pin. This pin should have an external pull up of $4K7-47K\Omega$ or left not connected in single core applications.

The JTAG device identification register can be read by using the IDCODE instruction. Its contents are specified in Figure 12.

Figure 12	Bit	31											De	evice	lde	ntifi	catio	on Re	egist	er										Bi					
Figure 12:	Version					Part Number															Manufacturer Identity										1				
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1	1			
return value		C)			()			. (D			()			2	2			(5			3	3			3					

The JTAG usercode register can be read by using the USERCODE instruction. Its contents are specified in Figure 13. The OTP User ID field is read from bits [22:31] of the security register on xCORE Tile 0, *see* §8.1 (all zero on unprogrammed devices).

Figure 13: USERCODE return value

Bit	31												ι	Jser	code	Reg	giste	r												В	it0
	OTP User ID								Unused Silicon Revision																						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0 0				()			ž	2			8	3			()			(C			C)					



12 Package Information



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Bits	Perm	Init	Description
31:24	RO	-	Reserved
23:16	RO		xCORE tile number on the switch.
15:9	RO	-	Reserved
8	RO		Set to 1 if boot from OTP is enabled.
7:0	RO		The boot mode pins MODE0, MODE1,, specifying the boot frequency, boot source, etc.

0x03: xCORE Tile boot status

B.5 Security configuration: 0x05

Copy of the security register as read from OTP.

0x05: Security configuration

Bits	Perm	Init	Description
31:0	RO		Value.

B.6 Ring Oscillator Control: 0x06

There are four free-running oscillators that clock four counters. The oscillators can be started and stopped using this register. The counters should only be read when the ring oscillator is stopped. The counter values can be read using four subsequent registers. The ring oscillators are asynchronous to the xCORE tile clock and can be used as a source of random bits.

0x06 Ring Oscillator Control

-	Bits	Perm	Init	Description
):	31:2	RO	-	Reserved
a r	1	RW	0	Set to 1 to enable the xCORE tile ring oscillators
l	0	RW	0	Set to 1 to enable the peripheral ring oscillators

B.7 Ring Oscillator Value: 0x07

This register contains the current count of the xCORE Tile Cell ring oscillator. This value is not reset on a system reset.

0x07: Ring Oscillator Value

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RO	-	Ring oscillator counter data.

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B.8 Ring Oscillator Value: 0x08

This register contains the current count of the xCORE Tile Wire ring oscillator. This value is not reset on a system reset.

0x08: Ring Oscillator Value

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RO	-	Ring oscillator counter data.

B.9 Ring Oscillator Value: 0x09

This register contains the current count of the Peripheral Cell ring oscillator. This value is not reset on a system reset.

0x09 Ring Oscillator Value

:	Bits	Perm	Init	Description
-	31:16	RO	-	Reserved
2	15:0	RO	-	Ring oscillator counter data.

B.10 Ring Oscillator Value: 0x0A

This register contains the current count of the Peripheral Wire ring oscillator. This value is not reset on a system reset.

0x0A: Ring Oscillator Value

A :	Bits	Perm	Init	Description
9 Dr	31:16	RO	-	Reserved
e	15:0	RO	-	Ring oscillator counter data.

B.11 Debug SSR: 0x10

This register contains the value of the SSR register when the debugger was called.

0x10:	Bits	Perm	Init	Description
Debug SSR	31:0	RO	-	Reserved

B.12 Debug SPC: 0x11

This register contains the value of the SPC register when the debugger was called.

0x50 .. 0x53: Data watchpoint address 1

Data point	Bits	Perm	Init	Description
ess 1	31:0	DRW		Value.

B.23 Data watchpoint address 2: 0x60 .. 0x63

This set of registers contains the second address for the four data watchpoints.

0x60 .. 0x63: Data watchpoint address 2

a It	Bits	Perm	Init	Description
2	31:0	DRW		Value.

B.24 Data breakpoint control register: 0x70 .. 0x73

This set of registers controls each of the four data watchpoints.

	Bits	Perm	Init	Description
	31:24	RO	-	Reserved
	23:16	DRW	0	A bit for each logical core in the tile allowing the breakpoint to be enabled individually for each logical core.
	15:3	RO	-	Reserved
	2	DRW	0	Set to 1 to enable breakpoints to be triggered on loads. Breakpoints always trigger on stores.
3: a it	1	DRW	0	By default, data watchpoints trigger if memory in the range [Address1Address2] is accessed (the range is inclusive of Address1 and Address2). If set to 1, data watchpoints trigger if memory outside the range (Address2Address1) is accessed (the range is exclusive of Address2 and Address1).
er	0	DRW	0	When 1 the instruction breakpoint is enabled.

0x70 .. 0x73: Data breakpoint control register

B.25 Resources breakpoint mask: 0x80 .. 0x83

This set of registers contains the mask for the four resource watchpoints.

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Bits	Perm	Init	Description
31:28	RW	0	The direction for packets whose first mismatching bit is 7.
27:24	RW	0	The direction for packets whose first mismatching bit is 6.
23:20	RW	0	The direction for packets whose first mismatching bit is 5.
19:16	RW	0	The direction for packets whose first mismatching bit is 4.
15:12	RW	0	The direction for packets whose first mismatching bit is 3.
11:8	RW	0	The direction for packets whose first mismatching bit is 2.
7:4	RW	0	The direction for packets whose first mismatching bit is 1.
3:0	RW	0	The direction for packets whose first mismatching bit is 0.

0x0C: Directions 0-7

D.9 Directions 8-15: 0x0D

This register contains eight directions, for packets with a mismatch in bits 15..8 of the node-identifier. The direction in which a packet will be routed is goverened by the most significant mismatching bit.

Bits	Perm	Init	Description
31:28	RW	0	The direction for packets whose first mismatching bit is 15.
27:24	RW	0	The direction for packets whose first mismatching bit is 14.
23:20	RW	0	The direction for packets whose first mismatching bit is 13.
19:16	RW	0	The direction for packets whose first mismatching bit is 12.
15:12	RW	0	The direction for packets whose first mismatching bit is 11.
11:8	RW	0	The direction for packets whose first mismatching bit is 10.
7:4	RW	0	The direction for packets whose first mismatching bit is 9.
3:0	RW	0	The direction for packets whose first mismatching bit is 8.

0x0D: Directions 8-15

D.10 DEBUG_N configuration: 0x10

Configures the behavior of the DEBUG_N pin.

	Bits	Perm	Init	Description
	31:2	RO	-	Reserved
-):	1	RW	0	Set to 1 to enable signals on DEBUG_N to generate DCALL on the core.
N n	0	RW	0	When set to 1, the DEBUG_N wire will be pulled down when the node enters debug mode.

0x10 DEBUG_N configuration

D.11 Debug source: 0x1F

Contains the source of the most recent debug event.

Bits	Perm	Init	Description
31:5	RO	-	Reserved
4	RW		If set, the external DEBUG_N pin is the source of the most recent debug interrupt.
3:1	RO	-	Reserved
0	RW		If set, the xCORE Tile is the source of the most recent debug interrupt.

0x1F: Debug source

D.12 Link status, direction, and network: 0x20 .. 0x27

These registers contain status information for low level debugging (read-only), the network number that each link belongs to, and the direction that each link is part of. The registers control links C, D, A, B, G, H, E, and F in that order.

Bits	Perm	Init	Description
31:26	RO	-	Reserved
25:24	RO		If this link is currently routing data into the switch, this field specifies the type of link that the data is routed to: 0: plink 1: external link 2: internal control link
23:16	RO	0	If the link is routing data into the switch, this field specifies the destination link number to which all tokens are sent.
15:12	RO	-	Reserved
11:8	RW	0	The direction that this this link is associated with; set for rout- ing.
7:6	RO	-	Reserved
5:4	RW	0	Determines the network to which this link belongs, set for quality of service.
3	RO	-	Reserved
2	RO	0	Set to 1 if the current packet is junk and being thrown away. A packet is considered junk if, for example, it is not routable.
1	RO	0	Set to 1 if the switch is routing data into the link, and if a route exists from another link.
0	RO	0	Set to 1 if the link is routing data into the switch, and if a route is created to another link on the switch.

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0x20 .. 0x27: Link status, direction, and network

H.4 Clock

- The CLK input pin is supplied with a clock with monotonic rising edges and low jitter.
- The PCU_CLK pin is supplied with a clock, for example it is tied to the main CLK (Section 9.1).
- The PCU_WAKE and PCU_GATE pins should be left unconnected (Section 9.1).
- Pins MODE0 and MODE1 are set to the correct value for the chosen oscillator frequency. The MODE settings are shown in the Oscillator section, Section 6. If you have a choice between two values, choose the value with the highest multiplier ratio since that will boot faster.

H.5 USB ULPI Mode

This section can be skipped if you do not have an external USB PHY.

- □ If using ULPI, the ULPI signals are connected to specific ports as shown in Section E.
- □ If using ULPI, the ports that are used internally are not connected, see Section E. (Note that this limitation only applies when the ULPI is enabled, they can still be used before or after the ULPI is being used.)

H.6 Boot

- The device is connected to a SPI flash for booting, connected to X0D0, X0D01, X0D10, and X0D11 (Section 7). If not, you must boot the device through OTP or JTAG.
- □ The device that is connected to flash has both MODE2 and MODE3 connected to pin 3 on the xSYS Header (MSEL). If no debug adapter connection is supported (not recommended) MODE2 and MODE3 are to be left NC (Section 7). MODE4 is set in accordance with Section 7.
- □ The SPI flash that you have chosen is supported by **xflash**, or you have created a specification file for it.

H.7 JTAG, XScope, and debugging

 \Box You have decided as to whether you need an XSYS header or not (Section G)

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- □ If you included an XSYS header, you connected pin 3 to any MODE2/MODE3 pin that would otherwise be NC (Section G).
- \Box If you have not included an XSYS header, you have devised a method to program the SPI-flash or OTP (Section G).

H.8 GPIO

You have not mapped both inputs and outputs to the same multi-bit port.

H.9 Multi device designs

Skip this section if your design only includes a single XMOS device.

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- \Box One device is connected to a SPI flash for booting.
- Devices that boot from link have MODE2 grounded and MODE3 NC. These device must have link XLB connected to a device to boot from (see 7).
- □ If you included an XSYS header, you have included buffers for RST_N, TRST_N, TMS, TCK, MODE2, and MODE3 (Section F).

I PCB Layout Design Check List

✓ This section is a checklist for use by PCB designers using the XS1-L8A-128-QF124. Each of the following sections contains items to check for each design.

I.1 Land pattern and solder stencil

- \Box You have used a land pattern suitable for the small QFN pads. (Section 10.1)
- You have used a solder stencil with the correct aperture and thinness. (Section 10.1)

I.2 Ground Plane

- Multiple vias (eg, 9) have been used to connect the center pad to the PCB ground plane. These minimize impedance and conduct heat away from the device. (Section 10.3).
- Other than ground vias, there are no (or only a few) vias underneath or closely around the device. This create a good, solid, ground plane.

I.3 Power supply decoupling

- \Box The decoupling capacitors are all placed close to a supply pin (Section 10).
- \Box The decoupling capacitors are spaced around the device (Section 10).
- The ground side of each decoupling capacitor has a direct path back to the center ground of the device.

I.4 PLL_AVDD

The PLL_AVDD filter (especially the capacitor) is placed close to the PLL_AVDD pin (Section 10).

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L Revision History

Date	Description
2013-01-30	New datasheet - revised part numbering
2013-02-26	New multicore microcontroller introduction
	Moved configuration sections to appendices
2013-07-19	Updated Features list with available ports and links - Section 2
	Simplified link bits in Signal Description - Section 4
	New JTAG, xSCOPE and Debugging appendix - Section G
	New Schematics Design Check List - Section H
	New PCB Layout Design Check List - Section I
2013-09-16	Removed references to PCU. Pins set to GND - Section 3
2013-12-09	Added Industrial Ambient Temperature - Section 11.1
2013-12-17	Added references to PCU - Section 3 and 9.1
2014-03-25	Updated BOTTOM VIEW in mechanical drawing - Section 12
2014-06-25	Added PCU_GATE, PCU_CLK, PCU_VDD, PCU_VDDIO to Schematics Checklist - Section H
2015-04-14	Updated Introduction - Section 1; Pin Configuration - Section 3; Signal Descrip- tion - Section 4

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