Trenz Electronic GmbH - TE0782-02-035-2I Datasheet

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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Obsolete
Module/Board Type	MCU, FPGA
Core Processor	ARM Cortex-A9
Co-Processor	Zynq-7000 (Z-7035)
Speed	-
Flash Size	32MB
RAM Size	1GB
Connector Type	Samtec QTH
Size / Dimension	3.35" x 3.35" (85mm x 85mm)
Operating Temperature	-40°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0782-02-035-2i

1 Table of Contents

2 Overview

The Trenz Electronic TE0782 is a high-performance, industrial-grade SoM (System on Module) with industrial temperature range based on Xilinx Zynq-7000 SoC (XC7Z035, XC7Z045 or XC7Z100).

These highly integrated modules with an economical price-performance-ratio have a form-factor of 8,5 x 8,5 cm and are available in several versions.

All parts cover at least industrial temperature range of -40°C to +85°C. The module operating temperature range depends on customer design and cooling solution. Please contact us for options and for modified PCB-equipping due increasing cost-performance-ratio and prices for large-scale order.

Refer to http://trenz.org/te0782-info for the current online version of this manual and other available documentation.

2.1 Key Features

- Xilinx Zynq-7000 XC7Z035, XC7Z045 or XC7Z100 SoC
- Rugged for shock and high vibration
- Large number of configurable I/Os are provided via rugged high-speed stacking strips
- Dual ARM Cortex-A9 MPCore
    - 1 GByte RAM (32-Bit wide DDR3)
    - 32 MByte QSPI Flash memory
    - 2 x Hi-Speed USB2 ULPI transceiver PHY
    - 2 x Gigabit (10/100/1000 Mbps) Ethernet transceiver PHY
    - 4 GByte eMMC (optional up to 64 GByte)
- 2 x MAC-address EEPROMs
- Optional 2x 64 MByte HyperFLASH or 2x 8 MByte HyperRAM (max 2x 32 MByte HyperRAM)
- Temperature compensated RTC (real-time clock)
- Si5338A programmable quad PLL clock generator for GTX transceiver clocks
- Plug-on module with 3 x 160-pin high-speed strips
    - 16 GTX high-performance transceiver
    - 2x GT transceiver clock inputs
    - 254 FPGA I/O's (125 LVDS pairs)
- On-board high-efficiency switch-mode DC-DC converters
- System management
- eFUSE bit-stream encryption
- AES bit-stream encryption
- Evenly-spread supply pins for good signal integrity
- User LED

Assembly options for cost or performance optimization available upon request.

Additional assembly options are available for cost or performance optimization upon request.

2.2 Block Diagram

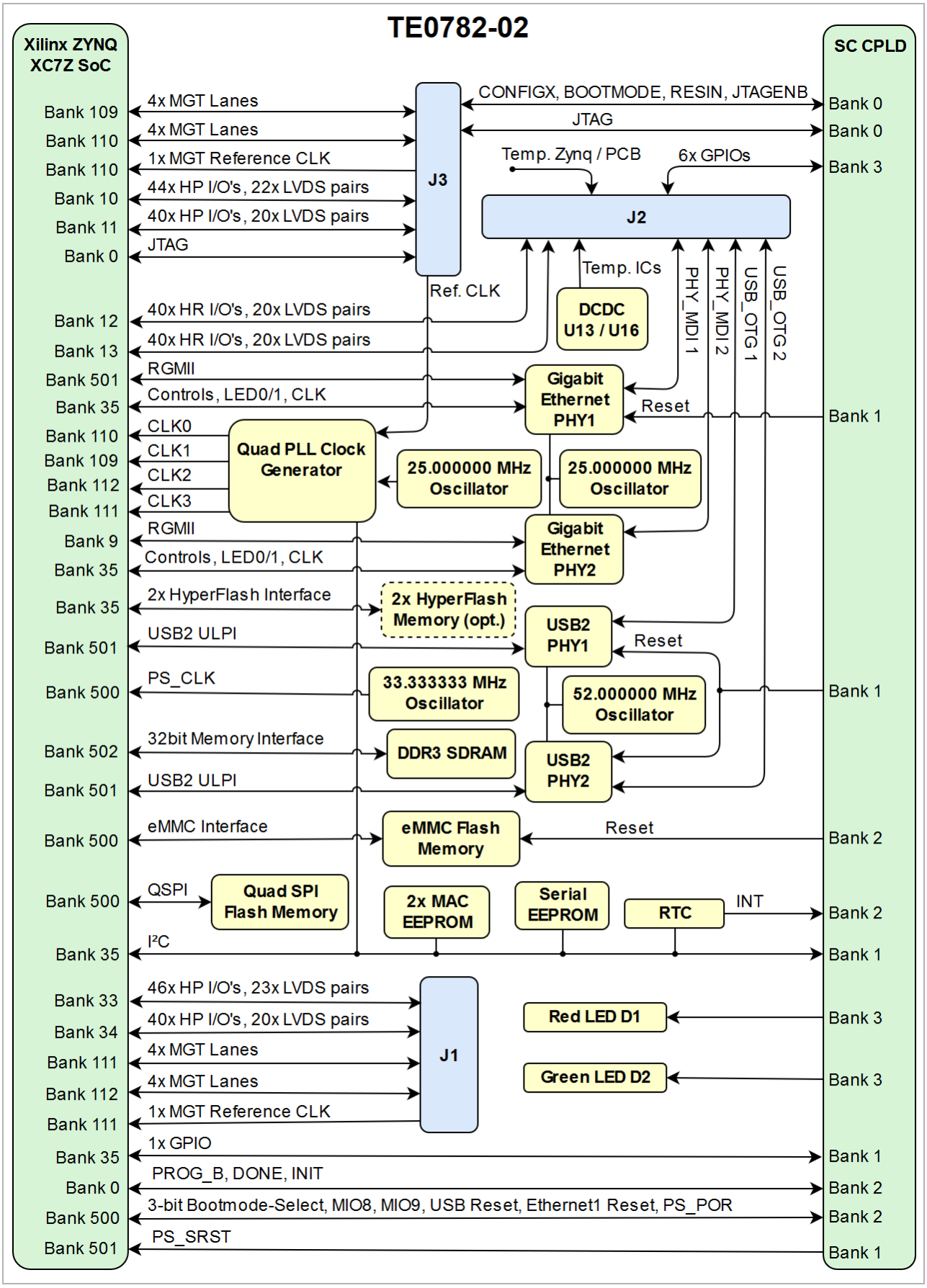

Figure 1: TE0782-02 block diagram

2.3 Main Components

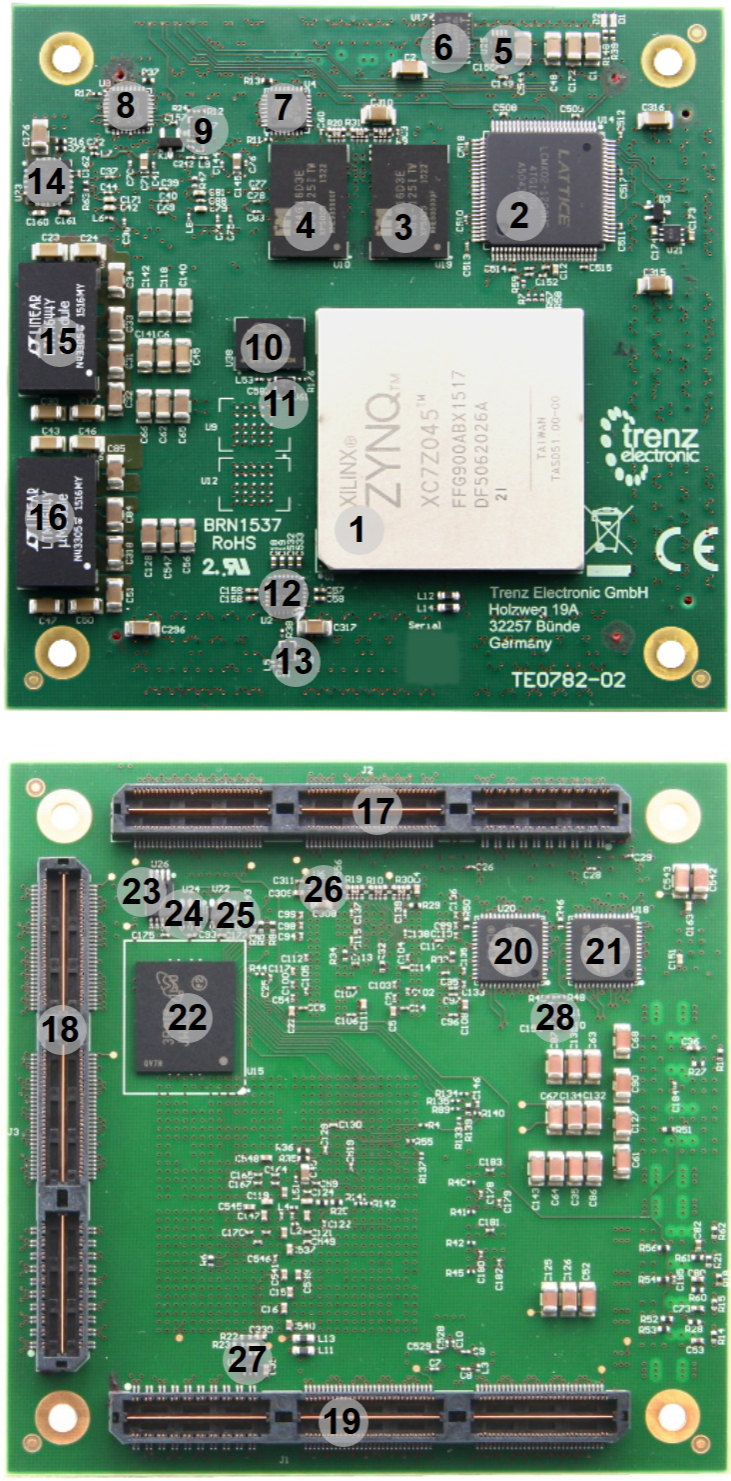

Figure 2: TE0782-02 main components

1. Xilinx Zynq UltraScale+ MPSoC, U1
2. Lattice Semiconductor MachXO2 1200HC CPLD, U14

Bank	Type	Lane	Signal Name	B2B Pin	FPGA Pin
		1	• MGT_RX5_P • MGT_RX5_N • MGT_TX5_P • MGT_TX5_N	• J3-12 • J3-10 • J3-11 • J3-9	• MGTXRXP1_110 • MGTXRXN1_110 • MGTXTXP1_110 • MGTXTXN1_110
		2	• MGT_RX6_P • MGT_RX6_N • MGT_TX6_P • MGT_TX6_N	• J3-8 • J3-6 • J3-7 • J3-5	• MGTXRXP2_110 • MGTXRXN2_110 • MGTXTXP2_110 • MGTXTXN2_110
		3	• MGT_RX7_P • MGT_RX7_N • MGT_TX7_P • MGT_TX7_N	• J3-4 • J3-2 • J3-3 • J3-1	• MGTXRXP3_110 • MGTXRXN3_110 • MGTXTXP3_110 • MGTXTXN3_110
111	GTX	0	• MGT_RX8_P • MGT_RX8_N • MGT_TX8_P • MGT_TX8_N	• J3-1 • J3-3 • J3-2 • J3-4	• MGTXRXP0_111 • MGTXRXN0_111 • MGTXTXP0_111 • MGTXTXN0_111
		1	• MGT_RX9_P • MGT_RX9_N • MGT_TX9_P • MGT_TX9_N	• J3-5 • J3-7 • J3-6 • J3-8	• MGTXRXP1_111 • MGTXRXN1_111 • MGTXTXP1_111 • MGTXTXN1_111
		2	• MGT_RX10_P • MGT_RX10_N • MGT_TX10_P • MGT_TX10_N	• J3-9 • J3-11 • J3-10 • J3-12	• MGTXRXP2_111 • MGTXRXN2_111 • MGTXTXP2_111 • MGTXTXN2_111
		3	• MGT_RX11_P • MGT_RX11_N • MGT_TX11_P • MGT_TX11_N	• J3-13 • J3-15 • J3-14 • J3-16	• MGTXRXP3_111 • MGTXRXN3_111 • MGTXTXP3_111 • MGTXTXN3_111
112	GTX	0	• MGT_RX12_P • MGT_RX12_N • MGT_TX12_P • MGT_TX12_N	• J3-17 • J3-19 • J3-18 • J3-20	• MGTXRXP0_112 • MGTXRXN0_112 • MGTXTXP0_112 • MGTXTXN0_112
		1	• MGT_RX13_P • MGT_RX13_N • MGT_TX13_P • MGT_TX13_N	• J3-21 • J3-23 • J3-22 • J3-24	• MGTXRXP1_112 • MGTXRXN1_112 • MGTXTXP1_112 • MGTXTXN1_112
		2	• MGT_RX14_P • MGT_RX14_N • MGT_TX14_P • MGT_TX14_N	• J3-25 • J3-27 • J3-26 • J3-28	• MGTXRXP2_112 • MGTXRXN2_112 • MGTXTXP2_112 • MGTXTXN2_112
		3	• MGT_RX15_P • MGT_RX15_N • MGT_TX15_P • MGT_TX15_N	• J3-29 • J3-31 • J3-30 • J3-32	• MGTXRXP3_112 • MGTXRXN3_112 • MGTXTXP3_112 • MGTXTXN3_112

Table 3: MGT lanes

There are 2 clock sources for the GTX transceivers. MGT_CLK1 and MGT_CLK4 are connected directly to B2B connector J3 and J1, so the clock can be provided by the carrier board. Clocks MGT_CLK0, MGT_CLK3, MGT_CLK5

and MGT_CLK6 are provided by the on-board clock generator (U2). As there are no capacitive coupling of the data and clock lines that are connected to the connectors, these may be required on the user's PCB depending on the application.

Bank	Type	Clock signal	Source	FPGA Pin	Notes
109	GTX	MGT_CLK3_P	U2, CLK3A	MGTREFCLK1P_109, AF10	Supplied by on-board Si5338A
		MGT_CLK3_N	U2, CLK3B	MGTREFCLK1N_109, AF9	
110	GTX	MGT_CLK0_P	U2, CLK2A	MGTREFCLK0P_110, AA8	Supplied by on-board Si5338A
		MGT_CLK0_N	U2, CLK2B	MGTREFCLK0N_110, AA7	
		MGT_CLK1_N	J3-39	MGTREFCLK1P_110, AC8	Supplied by B2B connector J3
		MGT_CLK1_P	J3-37	MGTREFCLK1N_110, AA7	
111	GTX	MGT_CLK4_N	J1-40	MGTREFCLK0P_111, U8	Supplied by B2B connector J1
		MGT_CLK4_P	J1-38	MGTREFCLK0N_111, U7	
		MGT_CLK5_P	U2, CLK1A	MGTREFCLK1P_111, W8	Supplied by on-board Si5338A
		MGT_CLK5_N	U2, CLK1B	MGTREFCLK1N_111, W7	
112	GTX	MGT_CLK6_P	U2, CLK0A	MGTREFCLK0P_112, N8	Supplied by on-board Si5338A
		MGT_CLK6_N	U2, CLK0B	MGTREFCLK0N_112, N7	

Table 4: MGT reference clock sources

4.3 JTAG Interface

JTAG access to the Xilinx Zynq-7000 is provided through B2B connector J3.

JTAG Signal	B2B Connector Pin
TMS	J3-142
TDI	J3-147
TDO	J3-148
TCK	J3-141

Table 5: Zynq JTAG interface signals

JTAG access to the LCMXO2-1200HC System Controller CPLD U14 is provided through B2B connector J3.

JTAG Signal	B2B Connector Pin
M_TMS	J3-82
M_TDI	J3-87
M_TDO	J3-88
M_TCK	J3-81

Table 6: System Controller CPLD JTAG interface signals

Pin J3-136 'JTAGENB' of B2B connector J3 is used to access the JTAG interface of the SC CPLD. Set high to program the System Controller CPLD via JTAG interaface.

4.4 System Controller CPLD I/O Pins

Special purpose pins are connected to System Controller CPLD and have following default configuration:

Pin Name	Direction	Function	Default Configuration
BOOTMODE	in	in	signal forwarded to MIO9 and currently used as UART RX line
CONFIGX	in	out	signal forwarded to MIO8 and currently used as UART TX line
RESIN	in	nRESET	external Board Reset
M_TDO	out	CPLD JTAG interface	-
M_TDI	in		
M_TCK	in		
M_TMS	in		
JTAGENB	in	enable JTAG	pull high for programming SC CPLD firmware
I2C_SCL	in / out	I^2C data line	I^2C bus of board
I2C_SDA	in	I^2C clock	
CPLD_IO	in / out	user GPIO	currently not used
ETH1_RESET	out	reset GbE PHY U18	see current SC CPLD firmware
OTG-RST	out	reset USB2 PHYs U4 and U8	see current SC CPLD firmware
RTC_INT	in	interrupt	interrupt from RTC
PS_SRST	out	Zynq control signal	reset PS of Zynq-7000 SoC
DONE	in		PL configuration completed
PROG_B	out		PL configuration reset signal
INIT	in		Low active FPGA initialization pin or configuration error signal
PS_POR	out		PS power-on reset
BM0/MIO5	out		Bootmode Pins currently configured in SC CPLD firmare to boot from QSPI Flash
BM2/MIO4	out		
BM3/MIO2	out		
MIO8	in	user MIO pins	currently used as UART interface
MIO9	out		
MMC_RST	out	Reset MMC Flash	see current SC CPLD firmware
ETH1-RESET33	in	reset GbE PHY U18	reset signal from Zynq-7000 level shifted to 1.8V
OTG-RST33	in	reset USB2 PHYs U4 and U8	reset signal from Zynq-7000 level shifted to 1.8V
LED1 ... LED2	out	LED status signal	see current CPLD firmware

4.8 I2C Interface

The on-board I^{2}C components are connected to bank 35 pins L15 (I2C_SDA) and L14 (I2C_SCL).

I^{2}C addresses for on-board components:

Device	IC	Designator	I2C-Address	Notes
EEPROM	24LC128-I/ST	U26	0x53	user data
EEPROM	24AA025E48T-I/OT	U22	0x50	MAC address EEPROM
EEPROM	24AA025E48T-I/OT	U24	0x51	MAC address EEPROM
RTC	ISL12020MIRZ	U17	0x6F	Temperature compensated real time clock
Battery backed RAM	ISL12020MIRZ	U17	0x57	Integrated in RTC
PLL	SI5338A-B-GMR	U2	0x70	-
SC CPLD	LCMXO2-1200HC-4TG100I	U14	user	-

Table 13: Address table of the I^{2}C bus slave devices

4.9 Pin Definitions

Pins with names ending with _VRN and _VRP are connected to Zynq PL HP bank special purpose pins VRN/VRP and can be routed to DCI calibration resistors on the baseboard. Otherwise they are usable as general purpose I/Os.

Bank 35 has 100 ohm DCI calibration resistors installed, it is also possible to "borrow" the DCI calibration from bank 35 for banks 34 and 33. For more detailed information about the DCI check Xilinx documentation.

5 On-board Peripherals

5.1 System Controller CPLD

The System Controller CPLD (U14) is provided by Lattice Semiconductor LCMXO2-1200HC (MachXO2 product family). It is the central system management unit with module specific firmware installed to monitor and control various signals of the FPGA, on-board peripherals, I/O interfaces and module as a whole.

See also TE0782 CPLD reference Wiki page.

5.2 eMMC Flash Memory

eMMC Flash memory device (U15) is connected to the Zynq PS MIO bank 500 pins MIO10..MIO15. eMMC chips MTFC4GMVEA-4M IT (Flash NAND-IC 2x 16 Gbit) is used with 4 GByte of memory density.

5.3 DDR4 Memory

By default TE0782-02 module has two 16-bit wide IM (Intelligent Memory) IM4G16D3FABG-125I DDR3L SDRAM (DDR3-1600 Speedgrade) chips arranged into 32-bit wide memory bus providing total of 1 GBytes of on-board RAM.

5.4 Quad SPI Flash Memory

Two quad SPI compatible serial bus flash memory for FPGA configuration file storage is provided by Spansion S25FL256SAGBHI20 with 256 Mbit (32 MByte) memory density. After configuration completes the remaining free memory can be used for application data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths to be used. The maximum data transfer rate depends on the bus width and clock frequency.

5.5 Gigabit Ethernet PHYs

On-board Gigabit Ethernet PHYs (U18, U20) are provided by Marvell Alaska 88E1512. The Ethernet PHYs' RGMII interfaces are connected to the Zynq's PS MIO bank 501 and to PL bank 9. I/O voltage is fixed at 1.8V for HSTL signaling. The reference clock input of both PHYs is supplied from an on-board 25.000000 MHz oscillator (U11).

5.6 High-speed USB ULPI PHYs

Hi-speed USB ULPI PHYs (U4. U8) are provided with USB3320 from Microchip. The ULPI interfaces are connected to the Zynq PS USB0 and USB1 via MIO28..51, bank 501 (see also section USB interface). The I/O voltage is fixed at 1.8V and PHY reference clock input is supplied from the on-board 52.000000 MHz oscillator (U7).

5.7 MAC Address EEPROMs

Two Microchip 24AA025E48 serial EEPROMs (U22, U24) contain globally unique 48-bit node address, which are compatible with EUI-48(TM) specification. The devices are organized as two blocks of 128 x 8 Kbit memory. One of the blocks stores the 48-bit node address and is write protected, the other block is available for application use. The MAC address EEPROMS areaccessible over I^2C bus (see also section I^2C interface).

Clock Source	Schematic Name	Frequency	Clock Destination
SiTime SiT8008AI oscillator, U61	PS_CLK	33.333333 MHz	Zynq SoC U1, pin A22
SiTime SiT8008BI oscillator, U21	-	25.000000 MHz	Quad PLL clock generator U2, pin 3
SiTime SiT8008AI oscillator, U7	-	52.000000 MHz	USB2 PHYs U4 and U8, pin 26
SiTime SiT8008BI oscillator, U11	-	25.000000 MHz	GbE PHYs U18 and U20, pin 34

Table 15: Reference clock signals

5.11 On-board LEDs

LED	Color	Connected to	Description and Notes
D1	Red	System Controller CPLD U14, bank 3	Exact function is defined by SC CPLD firmware
D2	Green	System Controller CPLD U14, bank 3	

Table 16: On-board LEDs

6 Power and Power-on Sequence

6.1 Power Supply

Power supply with minimum current capability of 4A for system startup is recommended.

6.2 Power Consumption

Power Input	Typical Current
VIN	TBD*
C3.3V	TBD*

Table 17: Power consumption

* TBD - To Be Determined soon with reference design setup.

To avoid any damage to the module, check for stabilized on-board voltages should be carried out (i.e. power good and enable signals) before powering up any Zynq's I/O bank voltages VCCO_x. All I/Os should be tri-stated during power-on sequence.

6.3 Power Distribution Dependencies

The Trenz TE0782 SoM is equipped with two quad DC-DC voltage regulators to generate required on-board voltage levels 1V, 3.3V, 1.8V, 1.2V_MGT, 1V_MGT. Additional voltage regulators are used to generate voltages 1.5V, VTT, VTTREF and 1.8V_MGT.

The power supply voltage 'C3.3V' of System Controller CPLD of the SoM have to be externally supplied with 3.3V nominal.

There are following dependencies how the initial voltages of the power rails on the B2B connectors are distributed to the on-board DC-DC converters, which power up further DC-DC converters and the particular on-board voltages:

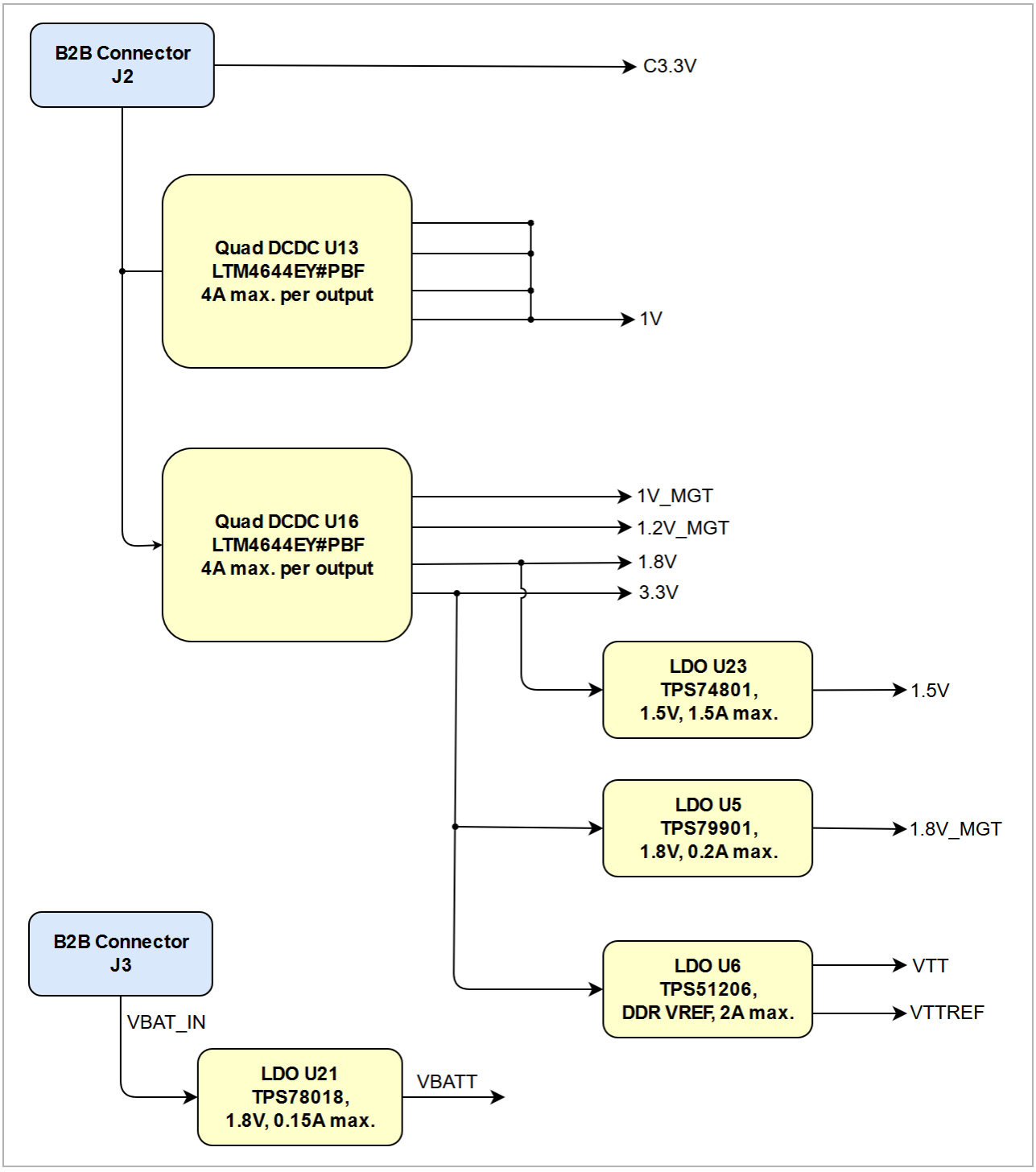

Figure 3: TE0782-02 Power Distribution Diagram

See also Xilinx datasheet DS191 for additional information. User should also check related base board documentation when intending base board design for TE0782 module.

6.4 Power-On Sequence

Power-on sequence is handled by the System Controller CPLD using "Power good"-signals from the voltage regulators:

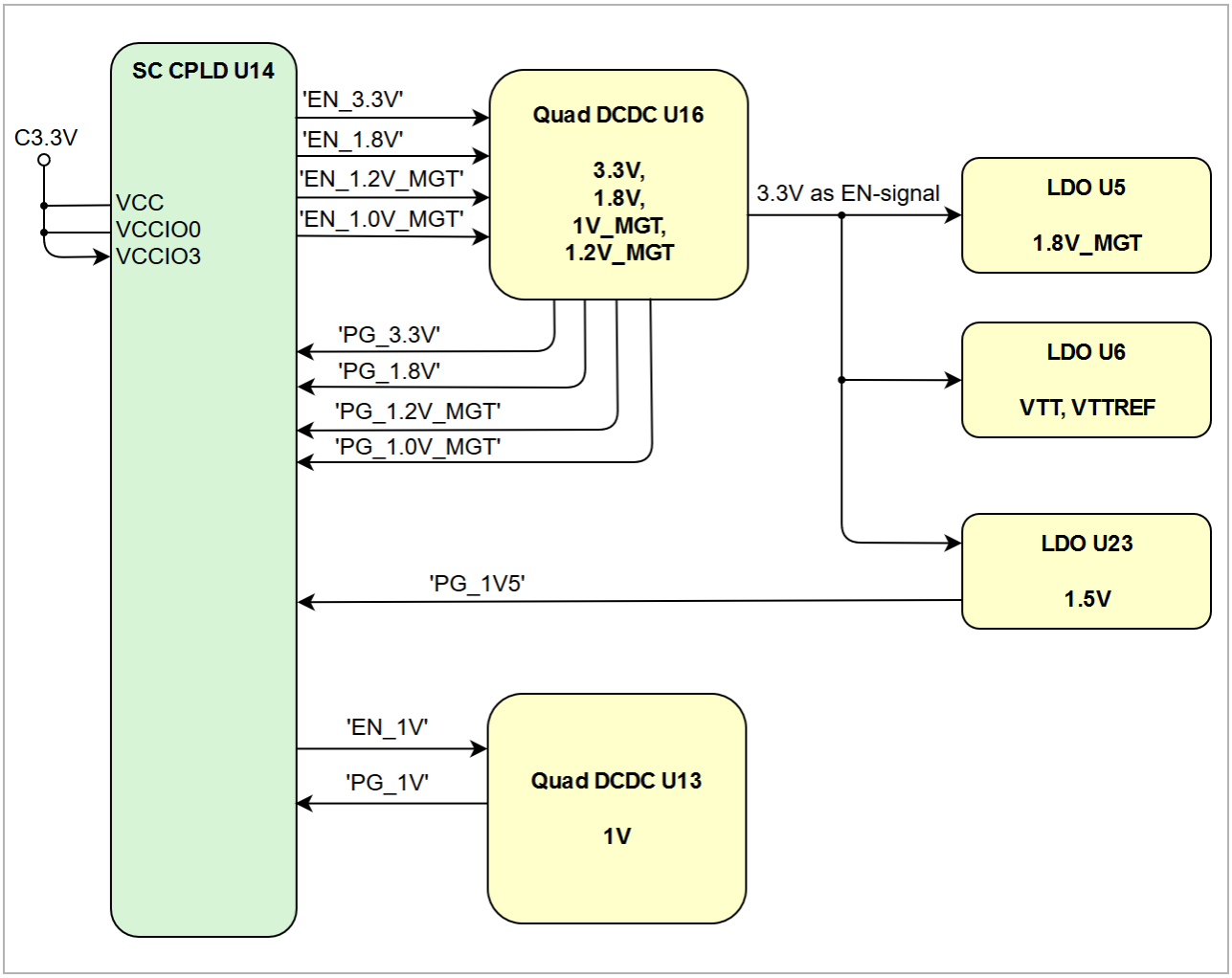

Figure 4: TE0782-02 Power-on Sequence Diagram

6.5 Power Rails

Power Rail Name on B2B Connector	J1 Pins	J2 Pins	J3 Pins	Direction	Notes
VIN	-	165, 166, 167, 168	-	Input	external power supply voltage
C3.3V	-	147, 148	-	Input	external 3.3V power supply voltage
3.3V	-	111, 112, 123, 124, 135 136 169, 170, 171, 172	-	Output	internal 3.3V voltage level
1.8V	169, 170, 171, 172	-	-	Output	internal 1.8V voltage level
VCCIO_10	-	-	99, 100	Input	high range I/O bank voltage

7 Board to Board Connectors

The TE0782 SoM has three 160-pin double-row ASP-122952-01 Samtec connectors on the bottom side which mate with ASP-122953-01 Samtec connectors on the baseboard. Mating height is 5 mm.

8 Variants Currently In Production

Trenz shop TE0782 overview page	
English page	German page

9 Technical Specifications

9.1 Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
VIN supply voltage	-0.3	15	V	LTM4644 datasheet
C3.3V supply voltage	-0.3	3.6	V	LTM4644 datasheet
VBAT supply voltage	-0.3	6	V	TPS780180 datasheet
PS I/O supply voltage, VCCO_PSIO	-0.5	3.6	V	Xilinx document DS191
PS I/O input voltage	-0.4	VCCO_PSIO + 0.55	V	Xilinx document DS191
HP I/O bank supply voltage, VCCO	-0.5	2.0	V	Xilinx document DS191
HP I/O bank input voltage	-0.55	VCCO + 0.55	V	Xilinx document DS191
HR I/O bank supply voltage, VCCO	-0.5	3.6	V	Xilinx document DS191
HR I/O bank input voltage	-0.55	VCCO + 0.55	V	Xilinx document DS191
Reference Voltage pin	-0.5	2	V	Xilinx document DS191
Differential input voltage	-0.4	2.625	V	Xilinx document DS191
MGT reference clocks absolute input voltage	-0.5	1.32	V	Xilinx document DS191
MGT absolute input voltage	-0.5	1.26	V	Xilinx document DS191
Voltage on SC CPLD pins	-0.5	3.75	V	Lattice Semiconductor MachXO2 datasheet
Storage temperature	-40	+85	°C	See eMMC MTFC4GMVEA datasheet

Table 20: Module absolute maximum ratings

9.2 Recommended Operating Conditions

Parameter	Min	Max	Units	Notes
VIN supply voltage	11.4	12.6	V	LTM4644 datasheet, 12V nominal
C3.3V supply voltage	3.3	3.465	V	LCMXO2-256HC, LTM4644 datasheet
VBAT supply voltage	2.2	5.5	V	TPS780180 datasheet
PS I/O supply voltage, VCCO_PSIO	1.710	3.465	V	Xilinx document DS191
PS I/O input voltage	–0.20	VCCO_PSIO + 0.20	V	Xilinx document DS191
HP I/O banks supply voltage, VCCO	1.14	1.89	V	Xilinx document DS191
HP I/O banks input voltage	-0.20	VCCO + 0.20	V	Xilinx document DS191
HR I/O banks supply voltage, VCCO	1.14	3.465	V	Xilinx document DS191
HR I/O banks input voltage	-0.20	VCCO + 0.20	V	Xilinx document DS191

10 Revision History

10.1 Hardware Revision History

Date	Revision	Notes	PCN Link	Documentation Link
-	02	current available board revision	-	TE0782-02
2015-05-27	01	Prototype only	-	-

Table 22: Hardware revision history table

Figure 6: Module hardware revision number

10.2 Document Change History

10.3 Document Change History

Date	Revision	Contributors	Description
2018-07-20	33	John Hartfiel	• small style update
19.07.2018	v.32	Ali Naseri	• Update TRM to new format and style
2018-05-15	v.22	Ali Naseri	• corrected minimum recommended VBAT supply voltage
2018-01-31	v.21	Ali Naseri	• updated Power section, added diagramms
2017-06-07	v.19	Jan Kumann	• Minor formatting
2017-05-23	v.13	Jan Kumann	• New block diagram • New product images • New physical dimensions drawing
2017-01-24	v.12	Ali Naseri	• New numbered pictures describing main components • Added variants in production
2016-06-27	v.10	Ali Naseri, Jan Kumann	• Initial release

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02.09.2017