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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Obsolete
Module/Board Type	MCU, FPGA
Core Processor	ARM Cortex-A9
Co-Processor	Zynq-7000 (Z-7045)
Speed	-
Flash Size	32MB
RAM Size	1GB
Connector Type	Samtec QTH
Size / Dimension	3.35" x 3.35" (85mm x 85mm)
Operating Temperature	-40°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0782-02-045-2i

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2.3 Main Components

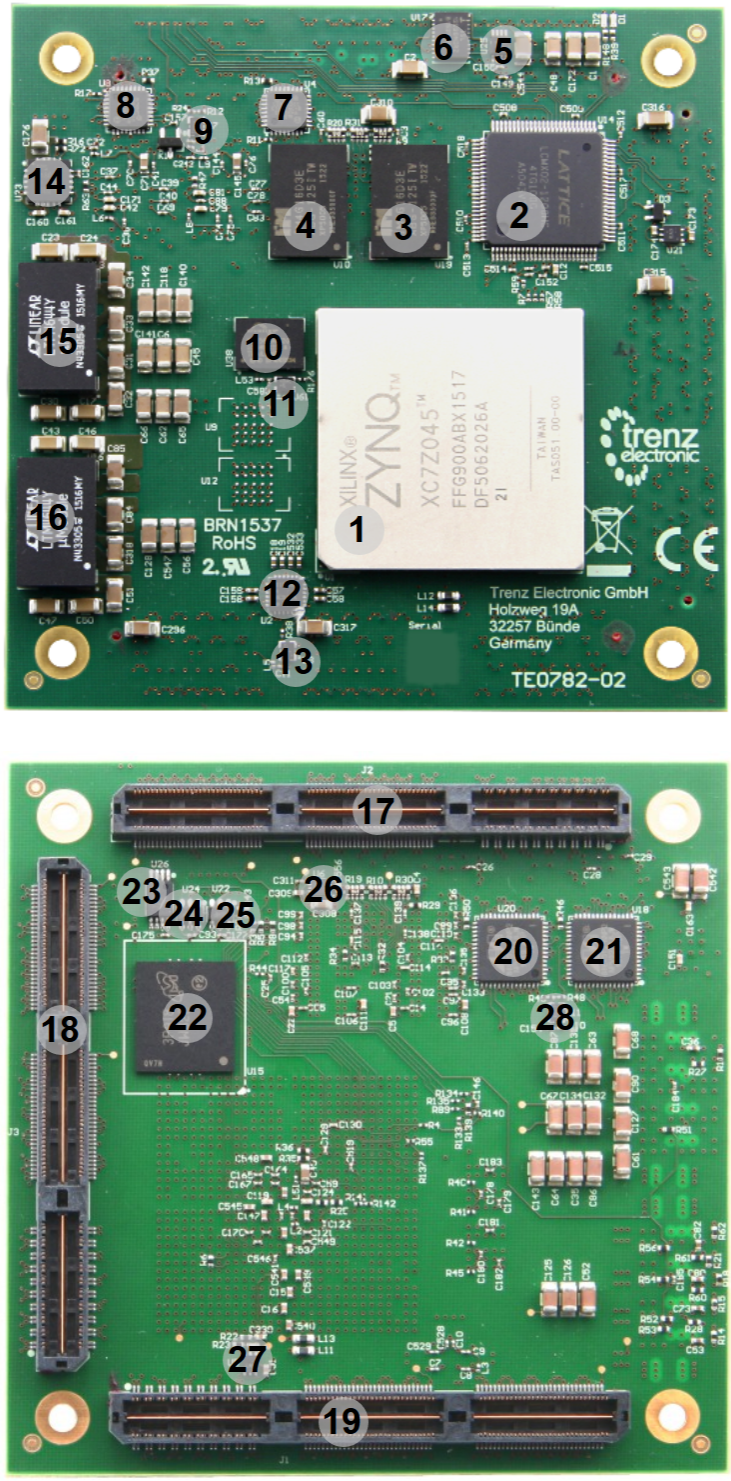

Figure 2: TE0782-02 main components

1. Xilinx Zynq UltraScale+ MPSoC, U1
2. Lattice Semiconductor MachXO2 1200HC CPLD, U14

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3. 4Gbit DDR3L SDRAM, U19
4. 4Gbit DDR3L SDRAM, U10
5. I^2C voltage translator, U25
6. Intersil ISL12020MIRZ Real Time Clock, U17
7. Microchip USB3320C USB PHY transceiver, U4
8. Microchip USB3320C USB PHY transceiver, U8
9. SiTime SiT8008 52.000000 MHz oscillator, U7
10. 32 MByte QSPI Flash memory, U38
11. SiTime SiT8008 33.333333 MHz oscillator, U61
12. SI5338A programmable quad PLL clock generator, U2
13. SiTime SiT8008 25.000000 MHz oscillator, U3
14. TPS74801 LDO @1.5V, U23
15. LT quad 4A PowerSoC DC-DC converter (@1.0V), U13
16. LT quad 4A PowerSoC DC-DC converter (@3.3V, @1,8V, @1.2V_MGT, @1.0V_MGT), U16
17. Samtec ASP-122952-01 160-pin stacking strip (2 rows a 80 positions), J2
18. Samtec ASP-122952-01 160-pin stacking strip (2 rows a 80 positions), J3
19. Samtec ASP-122952-01 160-pin stacking strip (2 rows a 80 positions), J1
20. Marvell Alaska 88E1512 Gigabit Ethernet PHY, 20
21. Marvell Alaska 88E1512 Gigabit Ethernet PHY, U18
22. Micron Technology 4 GByte eMMC, U15
23. Microchip 128Kbit I^2C EEPROM, U26
24. Microchip 2Kbit I^2C MAC EEPROM, U24
25. Microchip 2Kbit I^2C MAC EEPROM, U22
26. TPS51206 DDR reference voltage and termination regulator, U6
27. TPS799 LDO @1.8V_MGT, U5
28. SiTime SiT8008 25.000000 MHz oscillator, U11

2.4 Initial Delivery State

Storage device name	Content	Notes
24LC128-I/ST	not programmed	User content
24AA025E48 EEPROM's	User content not programmed	Valid MAC Address from manufacturer
Si5338A OTP Area	not programmed	-
eMMC Flash Memory	Empty, not programmed	Except serial number programmed by flash vendor
SPI Flash OTP Area	Empty, not programmed	Except serial number programmed by flash vendor
SPI Flash Quad Enable bit	Programmed	-
SPI Flash main array	demo design	-
HyperFlash Memory	not programmed	-
eFUSE USER	Not programmed	-
eFUSE Security	Not programmed	-

Table 1: Initial delivery state of programmable devices on the module

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3 Boot Process

4 of the 7 boot mode strapping pins (MIO2 ... MIO8) of the Xilinx Zynq-7000 SoC device are hardware programmed on the board, 3 of them are set be the SC CPLD firmware. They are evaluated by the Zynq device soon after the 'PS_POR' signal is deasserted to begin the boot process (see section "Boot Mode Pin Settings" of Xilinx manual UG585).

The TE0782 board is programmed in the SC CPLD firmware to boot initially from the on-board QSPI Flash memory U38. See section Bootmode in the TE0782 SC CPLD reference Wiki page.

The JTAG interface of the module is provided for storing the data to the QSPI Flash memory through the Zynq-7000 device.

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Bank	Type	Lane	Signal Name	B2B Pin	FPGA Pin
		1	• MGT_RX5_P • MGT_RX5_N • MGT_TX5_P • MGT_TX5_N	• J3-12 • J3-10 • J3-11 • J3-9	• MGTXRXP1_110 • MGTXRXN1_110 • MGTXTXP1_110 • MGTXTXN1_110
		2	• MGT_RX6_P • MGT_RX6_N • MGT_TX6_P • MGT_TX6_N	• J3-8 • J3-6 • J3-7 • J3-5	• MGTXRXP2_110 • MGTXRXN2_110 • MGTXTXP2_110 • MGTXTXN2_110
		3	• MGT_RX7_P • MGT_RX7_N • MGT_TX7_P • MGT_TX7_N	• J3-4 • J3-2 • J3-3 • J3-1	• MGTXRXP3_110 • MGTXRXN3_110 • MGTXTXP3_110 • MGTXTXN3_110
111	GTX	0	• MGT_RX8_P • MGT_RX8_N • MGT_TX8_P • MGT_TX8_N	• J3-1 • J3-3 • J3-2 • J3-4	• MGTXRXP0_111 • MGTXRXN0_111 • MGTXTXP0_111 • MGTXTXN0_111
		1	• MGT_RX9_P • MGT_RX9_N • MGT_TX9_P • MGT_TX9_N	• J3-5 • J3-7 • J3-6 • J3-8	• MGTXRXP1_111 • MGTXRXN1_111 • MGTXTXP1_111 • MGTXTXN1_111
		2	• MGT_RX10_P • MGT_RX10_N • MGT_TX10_P • MGT_TX10_N	• J3-9 • J3-11 • J3-10 • J3-12	• MGTXRXP2_111 • MGTXRXN2_111 • MGTXTXP2_111 • MGTXTXN2_111
		3	• MGT_RX11_P • MGT_RX11_N • MGT_TX11_P • MGT_TX11_N	• J3-13 • J3-15 • J3-14 • J3-16	• MGTXRXP3_111 • MGTXRXN3_111 • MGTXTXP3_111 • MGTXTXN3_111
112	GTX	0	• MGT_RX12_P • MGT_RX12_N • MGT_TX12_P • MGT_TX12_N	• J3-17 • J3-19 • J3-18 • J3-20	• MGTXRXP0_112 • MGTXRXN0_112 • MGTXTXP0_112 • MGTXTXN0_112
		1	• MGT_RX13_P • MGT_RX13_N • MGT_TX13_P • MGT_TX13_N	• J3-21 • J3-23 • J3-22 • J3-24	• MGTXRXP1_112 • MGTXRXN1_112 • MGTXTXP1_112 • MGTXTXN1_112
		2	• MGT_RX14_P • MGT_RX14_N • MGT_TX14_P • MGT_TX14_N	• J3-25 • J3-27 • J3-26 • J3-28	• MGTXRXP2_112 • MGTXRXN2_112 • MGTXTXP2_112 • MGTXTXN2_112
		3	• MGT_RX15_P • MGT_RX15_N • MGT_TX15_P • MGT_TX15_N	• J3-29 • J3-31 • J3-30 • J3-32	• MGTXRXP3_112 • MGTXRXN3_112 • MGTXTXP3_112 • MGTXTXN3_112

Table 3: MGT lanes

There are 2 clock sources for the GTX transceivers. MGT_CLK1 and MGT_CLK4 are connected directly to B2B connector J3 and J1, so the clock can be provided by the carrier board. Clocks MGT_CLK0, MGT_CLK3, MGT_CLK5

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4.4 System Controller CPLD I/O Pins

Special purpose pins are connected to System Controller CPLD and have following default configuration:

Pin Name	Direction	Function	Default Configuration
BOOTMODE	in	in	signal forwarded to MIO9 and currently used as UART RX line
CONFIGX	in	out	signal forwarded to MIO8 and currently used as UART TX line
RESIN	in	nRESET	external Board Reset
M_TDO	out	CPLD JTAG interface	-
M_TDI	in		
M_TCK	in		
M_TMS	in		
JTAGENB	in	enable JTAG	pull high for programming SC CPLD firmware
I2C_SCL	in / out	I^2C data line	I^2C bus of board
I2C_SDA	in	I^2C clock	
CPLD_IO	in / out	user GPIO	currently not used
ETH1_RESET	out	reset GbE PHY U18	see current SC CPLD firmware
OTG-RST	out	reset USB2 PHYs U4 and U8	see current SC CPLD firmware
RTC_INT	in	interrupt	interrupt from RTC
PS_SRST	out	Zynq control signal	reset PS of Zynq-7000 SoC
DONE	in		PL configuration completed
PROG_B	out		PL configuration reset signal
INIT	in		Low active FPGA initialization pin or configuration error signal
PS_POR	out		PS power-on reset
BM0/MIO5	out		Bootmode Pins currently configured in SC CPLD firmare to boot from QSPI Flash
BM2/MIO4	out		
BM3/MIO2	out		
MIO8	in	user MIO pins	currently used as UART interface
MIO9	out		
MMC_RST	out	Reset MMC Flash	see current SC CPLD firmware
ETH1-RESET33	in	reset GbE PHY U18	reset signal from Zynq-7000 level shifted to 1.8V
OTG-RST33	in	reset USB2 PHYs U4 and U8	reset signal from Zynq-7000 level shifted to 1.8V
LED1 ... LED2	out	LED status signal	see current CPLD firmware

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4.6 Gigabit Ethernet

The TE0782 is equipped with two Marvell Alaska 88E1512 Gigabit Ethernet PHYs (U18 (ETH1) and U20 (ETH2)). The transceiver PHY of ETH1 is connected to the Zynq PS Ethernet GEM0. The I/O Voltage is fixed at 1.8V for HSTL signaling. The reference clock input for both PHYs is supplied from an on board 25MHz oscillator (U11), the 125MHz output clock of both PHYs are connected to Zynq's PL bank 35.

ETH1 PHY connection:

PHY PIN	Zynq PS / PL	System Controller CPLD	Notes
MDC/MDIO	MIO52, MIO53	-	-
LED0	Bank 35, Pin B12	-	-
LED1	Bank 35, Pin C12	-	-
Interrupt	Bank 35, Pin A15	-	-
CONFIG	Bank 35, Pin F14	-	When pin connected to GND, PHY Address is strapped to 0x00 by default
RESETn	-	Pin 53	ETH1_RESET33 (MIO7) -> SC CPLD -> ETH1_RESET
RGMII	MIO16..MIO27		-
MDI	-	-	on B2B J2 connector

Table 9: General overview of the Gigabit Ethernet1 PHY signals

ETH2 PHY connection:

PHY PIN	Zynq PS / PL	System Controller CPLD	Notes
MDC/MDIO	Bank 35, Pin C17/B17	-	-
LED0	Bank 35, Pin K15	-	-
LED1	Bank 35, Pin B16	-	-
Interrupt	Bank 35, Pin A17	-	-
CONFIG	Bank 35, Pin E15	-	When pin connected to GND, PHY Address is strapped to 0x00 by default
RESETn	Bank 35, Pin B15	-	-
RGMII	Bank 9	-	-
MDI	-	-	on B2B J2 connector

Table 10: General overview of the Gigabit Ethernet2 PHY signals

4.7 USB Interface

The TE0782 is equipped with two USB PHY's USB3320 from Microchip (U4 (USB0) and U8 (USB1)). The ULPI interface of USB0 is connected to the Zynq PS USB0, ULPI interface of USB1 to Zynq PS USB1. The I/O Voltage is fixed at 1.8V.

The reference clock input of both PHY's is supplied from an on board 52MHz oscillator (U7).

USB0 PHY connection:

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PHY Pin	Zynq PS / PL	CPLD	B2B Connector J2	Notes
ULPI	MIO28..39	-	-	Zynq USB0 MIO pins are connected to the PHY
REFCLK	-	-	-	52MHz from on board oscillator (U7)
REFSEL[0..2]	-	-	-	000 GND, select 52MHz reference Clock
RESETB	MIO0	OTG_RESET33	-	OTG_RESET33 -> SC CPLD -> OTG_RESET
CLKOUT	MIO36	-	-	Connected to 1.8V selects reference clock operation mode
DP,DM	-	-	USB1_D_P, USB1_D_N	USB Data lines
CPEN	-	-	VBUS1_V_EN	External USB power switch active high enable signal
VBUS	-	-	USB1_VBUS	Connect to USB VBUS via a series resistor. Check reference schematic.
ID	-	-	OTG1_ID	For an A-Device connect to ground, for a B-Device left floating

Table 11: General overview of the USB0 PHY signals

USB1 PHY connection:

PHY Pin	Zynq PS / PL	CPLD	B2B Connector J2	Notes
ULPI	MIO40..51	-	-	Zynq USB1 MIO pins are connected to the PHY
REFCLK	-	-	-	52MHz from on board oscillator (U7)
REFSEL[0..2]	-	-	-	000 GND, select 52MHz reference Clock
RESETB	MIO0	OTG_RESET33	-	OTG_RESET33 -> SC CPLD -> OTG_RESET
CLKOUT	MIO48	-	-	Connected to 1.8V selects reference clock operation mode
DP,DM	-	-	USB2_D_P, USB2_D_N	USB Data lines
CPEN	-	-	VBUS2_V_EN	External USB power switch active high enable signal
VBUS	-	-	USB2_VBUS	Connect to USB VBUS via a series resistor. Check reference schematic.
ID	-	-	OTG2_ID	For an A-Device connect to ground, for a B-Device left floating

Table 12: General overview of the USB1 PHY signals

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4.8 I2C Interface

The on-board I^{2}C components are connected to bank 35 pins L15 (I2C_SDA) and L14 (I2C_SCL).

I^{2}C addresses for on-board components:

Device	IC	Designator	I2C-Address	Notes
EEPROM	24LC128-I/ST	U26	0x53	user data
EEPROM	24AA025E48T-I/OT	U22	0x50	MAC address EEPROM
EEPROM	24AA025E48T-I/OT	U24	0x51	MAC address EEPROM
RTC	ISL12020MIRZ	U17	0x6F	Temperature compensated real time clock
Battery backed RAM	ISL12020MIRZ	U17	0x57	Integrated in RTC
PLL	SI5338A-B-GMR	U2	0x70	-
SC CPLD	LCMXO2-1200HC-4TG100I	U14	user	-

Table 13: Address table of the I^{2}C bus slave devices

4.9 Pin Definitions

Pins with names ending with _VRN and _VRP are connected to Zynq PL HP bank special purpose pins VRN/VRP and can be routed to DCI calibration resistors on the baseboard. Otherwise they are usable as general purpose I/Os.

Bank 35 has 100 ohm DCI calibration resistors installed, it is also possible to "borrow" the DCI calibration from bank 35 for banks 34 and 33. For more detailed information about the DCI check Xilinx documentation.

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5.8 Configuration EEPROM

The TE0782 board contains one EEPROM (U26) for configuration and general user purposes. The EEPROMs is provided by Microchip 24LC128-I/ST with 128 KBit memory density, the EEPROM is areaccessible over I^2C bus (see also section I^2C interface).

5.9 Programmable Clock Generator

There is a Silicon Labs I^2C programmable clock generator Si5338A (U2) chip on-board. It's output frequencies can be programmed using the I^2C bus address 0x70 or 0x71. Default address is 0x70, IN4/I2C_LSB pin must be set to high for address 0x71.

A 25.000000 MHz oscillator (U3) is connected to the pin IN3 and is used to generate the output clocks. The output voltage of the oscillator is provided by the 1.8V power rail, thus making output frequency available as soon as 1.8V is present. All 4 of the Si5338 clock outputs are connected to the MGT banks of the Zynq device. It is possible to use the clocks connected to the GTR bank in the user's logic design. This is achieved by instantiating a IBUFDSGTE buffer in the design.

Once running, the frequency and other parameters can be changed by programming the device using the I^2C bus connected between the FPGA (master) and clock generator (slave). For this, proper I^2C bus logic has to be implemented in FPGA.

Signal	Frequency	Notes
IN1/IN2	user	External clock signal supply from B2B connector J3, pins J3-38 / J3-40
IN3	25.000000 MHz	Fixed input clock signal from reference clock generator SiT8008BI-73-18S-25.000000E (U3)
IN4	-	LSB of the default I^2C address, wired to ground mean address is 0x70
IN5	-	Not connected
IN6	-	Wired to ground
CLK0 A/B	-	reference clock 0 of Bank 112 GTX
CLK1 A/B	-	reference clock 1 of Bank 111 GTX
CLK2 A/B	-	reference clock 0 of Bank 110 GTX
CLK3 A/B	-	reference clock 1 of Bank 109 GTX

Table 14: General overview of the on-board quad clock generator I/O signals

5.10 Oscillators

The module has following reference clock signals provided by on-board oscillators and external source from carrier board:

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Clock Source	Schematic Name	Frequency	Clock Destination
SiTime SiT8008AI oscillator, U61	PS_CLK	33.333333 MHz	Zynq SoC U1, pin A22
SiTime SiT8008BI oscillator, U21	-	25.000000 MHz	Quad PLL clock generator U2, pin 3
SiTime SiT8008AI oscillator, U7	-	52.000000 MHz	USB2 PHYs U4 and U8, pin 26
SiTime SiT8008BI oscillator, U11	-	25.000000 MHz	GbE PHYs U18 and U20, pin 34

Table 15: Reference clock signals

5.11 On-board LEDs

LED	Color	Connected to	Description and Notes
D1	Red	System Controller CPLD U14, bank 3	Exact function is defined by SC CPLD firmware
D2	Green	System Controller CPLD U14, bank 3	

Table 16: On-board LEDs

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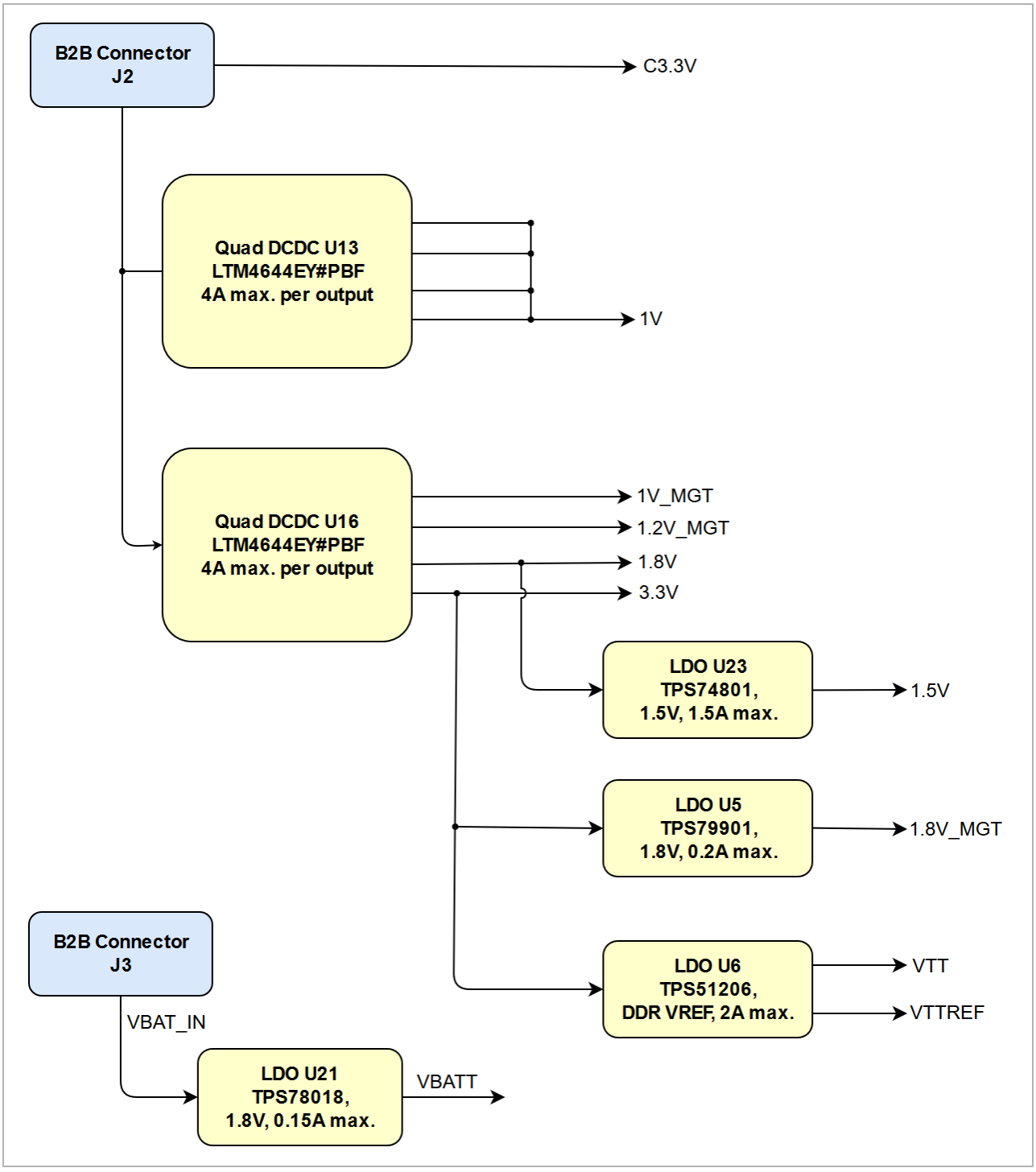

Figure 3: TE0782-02 Power Distribution Diagram

See also Xilinx datasheet DS191 for additional information. User should also check related base board documentation when intending base board design for TE0782 module.

6.4 Power-On Sequence

Power-on sequence is handled by the System Controller CPLD using "Power good"-signals from the voltage regulators:

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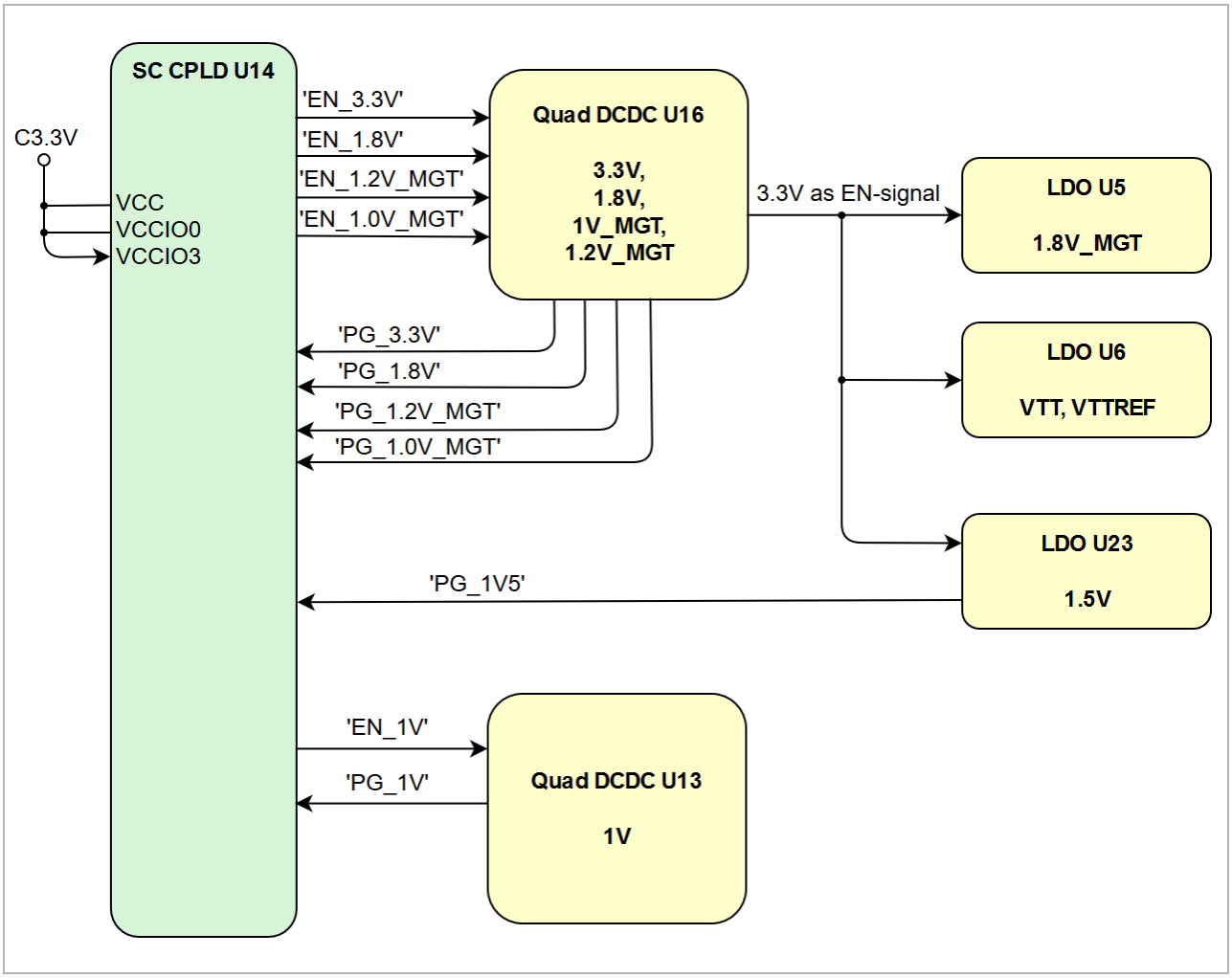

Figure 4: TE0782-02 Power-on Sequence Diagram

6.5 Power Rails

Power Rail Name on B2B Connector	J1 Pins	J2 Pins	J3 Pins	Direction	Notes
VIN	-	165, 166, 167, 168	-	Input	external power supply voltage
C3.3V	-	147, 148	-	Input	external 3.3V power supply voltage
3.3V	-	111, 112, 123, 124, 135 136 169, 170, 171, 172	-	Output	internal 3.3V voltage level
1.8V	169, 170, 171, 172	-	-	Output	internal 1.8V voltage level
VCCIO_10	-	-	99, 100	Input	high range I/O bank voltage

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Power Rail Name on B2B Connector	J1 Pins	J2 Pins	J3 Pins	Direction	Notes
VCCIO_11	-	-	159, 160	Input	high range I/O bank voltage
VCCIO_12	-	159, 160	-	Input	high range I/O bank voltage
VCCIO_13	-	99, 100	-	Input	high range I/O bank voltage
VCCIO_33	99, 100	-	-	Input	high performance I/O bank voltage
VCCIO_34	159, 160	-	-	Input	high performance I/O bank voltage
VBAT_IN	-	-	124	Input	backup battery voltage

Table 18: Module power rails

6.6 Bank Voltages

Bank	Schematic Name	Voltage	Range	Notes
0	-	3.3 V	-	FPGA configuration
502	-	1.5 V	-	DDR3-RAM port
109 / 110 / 111 / 112	-	1.2 V	-	MGT
500 / 501	-	3.3 V	-	MIO banks
9 (HR)	-	1.8 V	1.2V to 3.3V	ETH2 RGMII
10 (HR)	VCCIO_10	user	1.2V to 3.3V	-
11 (HR)	VCCIO_11	user	1.2V to 3.3V	-
12 (HR)	VCCIO_12	user	1.2V to 3.3V	-
13 (HR)	VCCIO_13	user	1.2V to 3.3V	-
33 (HP)	VCCIO_33	user	1.2V to 1.8V	-
34 (HP)	VCCIO_34	user	1.2V to 1.8V	-
35 (HP)	-	1.8 V	1.2V to 1.8V	Hyper-RAM, Ethernet, I^2C

Table 19: Module I/O bank voltages

See Xilinx Zynq-7000 datasheet DS191 for the voltage ranges allowed.

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8 Variants Currently In Production

Trenz shop TE0782 overview page	
English page	German page

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9 Technical Specifications

9.1 Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
VIN supply voltage	-0.3	15	V	LTM4644 datasheet
C3.3V supply voltage	-0.3	3.6	V	LTM4644 datasheet
VBAT supply voltage	-0.3	6	V	TPS780180 datasheet
PS I/O supply voltage, VCCO_PSIO	-0.5	3.6	V	Xilinx document DS191
PS I/O input voltage	-0.4	VCCO_PSIO + 0.55	V	Xilinx document DS191
HP I/O bank supply voltage, VCCO	-0.5	2.0	V	Xilinx document DS191
HP I/O bank input voltage	-0.55	VCCO + 0.55	V	Xilinx document DS191
HR I/O bank supply voltage, VCCO	-0.5	3.6	V	Xilinx document DS191
HR I/O bank input voltage	-0.55	VCCO + 0.55	V	Xilinx document DS191
Reference Voltage pin	-0.5	2	V	Xilinx document DS191
Differential input voltage	-0.4	2.625	V	Xilinx document DS191
MGT reference clocks absolute input voltage	-0.5	1.32	V	Xilinx document DS191
MGT absolute input voltage	-0.5	1.26	V	Xilinx document DS191
Voltage on SC CPLD pins	-0.5	3.75	V	Lattice Semiconductor MachXO2 datasheet
Storage temperature	-40	+85	°C	See eMMC MTFC4GMVEA datasheet

Table 20: Module absolute maximum ratings

9.2 Recommended Operating Conditions

Parameter	Min	Max	Units	Notes
VIN supply voltage	11.4	12.6	V	LTM4644 datasheet, 12V nominal
C3.3V supply voltage	3.3	3.465	V	LCMXO2-256HC, LTM4644 datasheet
VBAT supply voltage	2.2	5.5	V	TPS780180 datasheet
PS I/O supply voltage, VCCO_PSIO	1.710	3.465	V	Xilinx document DS191
PS I/O input voltage	–0.20	VCCO_PSIO + 0.20	V	Xilinx document DS191
HP I/O banks supply voltage, VCCO	1.14	1.89	V	Xilinx document DS191
HP I/O banks input voltage	-0.20	VCCO + 0.20	V	Xilinx document DS191
HR I/O banks supply voltage, VCCO	1.14	3.465	V	Xilinx document DS191
HR I/O banks input voltage	-0.20	VCCO + 0.20	V	Xilinx document DS191

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Parameter	Min	Max	Units	Notes
Differential input voltage	-0.2	2.625	V	Xilinx document DS191
Voltage on SC CPLD pins	-0.3	3.6	V	Lattice Semiconductor MachXO2 datasheet
Operating Temperature Range	-40	85	°C	Xilinx document DS191, industrial grade Zynq temperarure range

Table 21: Recommended operating conditions

Module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

⚠ See Xilinx datasheet DS191 for more information about absolute maximum and recommended operating ratings for the Zynq-7000 chips.

9.3 Physical Dimensions

- Module size: 85 mm × 85 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 5 mm
- PCB thickness: 1.7 mm

All dimensions are shown in millimeters.

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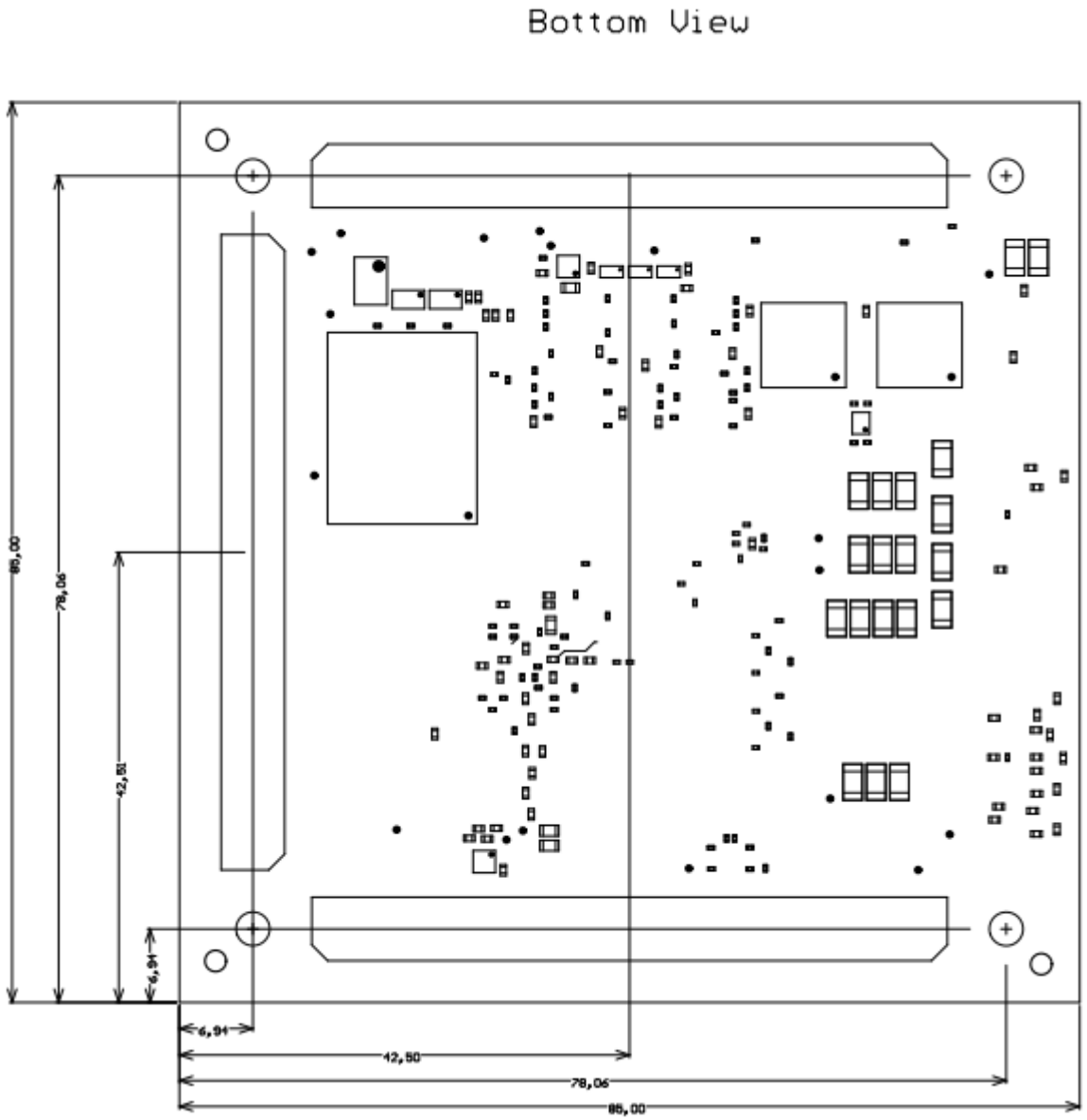

Figure 5: Module physical dimensions drawing

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11 Disclaimer

11.1 Data privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

11.2 Document Warranty

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11.6 Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

11.7 REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release

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any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

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