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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Host/Peripheral Controller
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	CYUSB
RAM Size	256K x 8
Interface	GPIF, I²C, I²S, MMC/SD/SDIO, SPI, UART
Number of I/O	60
Voltage - Supply	1.15V ~ 1.25V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-FBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyusb3031-bzxc

Host Processor Interface (P-Port)

A configurable interface enables FX3S to communicate with various devices such as Sensor, FPGA, Host Processor, or a Bridge chip. FX3S supports the following P-Port interfaces.

- GPIF II (16-bit)
- Slave FIFO Interface
- 16-bit Asynchronous SRAM Interface
- 16-bit Asynchronous address/data multiplexed (ADMux) Interface
- 16-bit Synchronous address/data multiplexed (ADMux) Interface
- Processor MMC slave Interface compatible with MMC System specification, MMCA Technical Committee, Version 4.2 with eMMC 4.3 and 4.4 Pass-Through boot

The following sections describe these P-Port interfaces.

GPIF II

The high-performance GPIF II interface enables functionality similar to, but more advanced than, FX2LP's GPIF and Slave FIFO interfaces.

The GPIF II is a programmable state machine that enables a flexible interface that may function either as a master or slave in industry-standard or proprietary interfaces. Both parallel and serial interfaces may be implemented with GPIF II.

Here are a list of GPIF II features:

- Functions as master or slave
- Provides 256 firmware programmable states
- Supports 8-bit and 16-bit parallel data bus
- Enables interface frequencies up to 100 MHz
- Supports 16 configurable control pins when a 16/8 data bus is used. All control pins can be either input/output or bi-directional.

GPIF II state transitions are based on control input signals. The control output signals are driven as a result of the GPIF II state transitions. The INT# output signal can be controlled by GPIF II. Refer to the GPIFII Designer tool. The GPIF II state machine's behavior is defined by a GPIF II descriptor. The GPIF II descriptor is designed such that the required interface specifications are met. 8 kB of memory (separate from the 512 kB of embedded SRAM) is dedicated to the GPIF II waveform where the GPIF II descriptor is stored in a specific format.

Cypress's GPIF II Designer Tool enables fast development of GPIF II descriptors and includes examples for common interfaces.

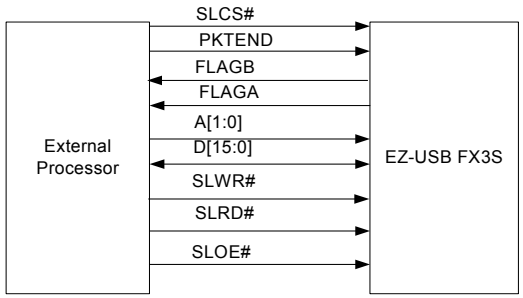
Example implementations of GPIF II are the asynchronous slave FIFO and synchronous slave FIFO interfaces.

Slave FIFO Interface

The Slave FIFO interface signals are shown in Figure 6. This interface allows an external processor to directly access up to four buffers internal to FX3S. Further details of the Slave FIFO interface are described on page 35.

Note Access to all 32 buffers is also supported over the slave FIFO interface. For details, contact Cypress Applications Support.

Figure 6. Slave FIFO Interface



Note: Multiple Flags may be configured.

Asynchronous SRAM

This interface consists of standard asynchronous SRAM interface signals as shown in Figure 7. This interface is used to access both the configuration registers and buffer memory of FX3S. Both single-cycle and burst accesses are supported by asynchronous interface signals.

The most significant address bit, A[7], determines whether the configuration registers or buffer memory are accessed. When the configuration registers are selected by asserting the address bit A[7], the address bus bits A[6:0] point to a configuration register. When A[7] is deasserted, the buffer memory is accessed as indicated by the P-Port DMA transfer register and the transfer size is determined by the P-Port DMA transfer size register.

Application processors with a DMA controller that use address auto-increment during DMA transfers, can override this by connecting any higher-order address line (such as A[15]/A[23]/A[31]) of the application processor to FX3S's A[7].

In the asynchronous SRAM mode, when reading from a buffer memory, FX3S supports two methods of reading out next data from the buffer. The next data may be read out on the rising edge of OE# or by toggling the least significant address bit A[0].

In this mode, the P-Port interface works with a 32.5-ns minimum access cycle providing an interface data rate of up to 61.5 MB per second.

Table 6. Entry and Exit Methods for Low-Power Modes (continued)

Low-Power Mode	Characteristics	Methods of Entry	Methods of Exit
Suspend Mode with USB 3.0 PHY Disabled (L2)	■ The power consumption in this mode does not exceed ISB_2 ■ USB 3.0 PHY is disabled and the USB interface is in suspend mode ■ The clocks are shut off. The PLLs are disabled ■ All I/Os maintain their previous state ■ USB interface maintains the previous state ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually ■ The states of the configuration registers, buffer memory and all internal RAM are maintained ■ All transactions must be completed before FX3S enters Suspend mode (state of outstanding transactions are not preserved) ■ The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion) because the program counter does not reset	■ Firmware executing on ARM926EJ-S core can put FX3S into suspend mode. For example, on USB suspend condition, firmware may decide to put FX3S into suspend mode ■ External Processor, through the use of mailbox registers can put FX3S into suspend mode	■ D+ transitioning to low or high ■ D- transitioning to low or high ■ Impedance change on OTG_ID pin ■ Resume condition on SSRX± ■ Detection of VBUS ■ Level detect on UART_CTS (programmable polarity) ■ GPIF II interface assertion of CTL[0] ■ Assertion of RESET#
Standby Mode (L3)	■ The power consumption in this mode does not exceed ISB3 ■ All configuration register settings and program/data RAM contents are preserved. However, data in the buffers or other parts of the data path, if any, is not guaranteed. Therefore, the external processor should take care that the data needed is read before putting FX3S into this Standby Mode ■ The program counter is reset after waking up from Standby ■ GPIO pins maintain their configuration ■ Crystal oscillator is turned off ■ Internal PLL is turned off ■ USB transceiver is turned off ■ ARM926EJ-S core is powered down. Upon wakeup, the core re-starts and runs the program stored in the program/data RAM ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually	■ Firmware executing on ARM926EJ-S core or external processor configures the appropriate register	■ Detection of VBUS ■ Level detect on UART_CTS (Programmable Polarity) ■ GPIF II interface assertion of CTL[0] ■ Assertion of RESET#

Configuration Options

Configuration options are available for specific usage models. Contact Cypress Applications or Marketing for details.

Digital I/Os

FX3S has internal firmware-controlled pull-up or pull-down resistors on all digital I/O pins. An internal 50-kΩ resistor pulls the pins high, while an internal 10-kΩ resistor pulls the pins low to prevent them from floating. The I/O pins may have the following states:

- Tristated (High-Z)
- Weak pull-up (via internal 50 kΩ)
- Pull-down (via internal 10 kΩ)
- Hold (I/O hold its value) when in low-power modes
- The JTAG TDI, TMC, and TRST# signals have fixed 50-kΩ internal pull-ups, and the TCK signal has a fixed 10-kΩ pull-down resistor.

All unused I/Os should be pulled high by using the internal pull-up resistors. All unused outputs should be left floating. All I/Os can be driven at full-strength, three-quarter strength, half-strength, or quarter-strength. These drive strengths are configured separately for each interface.

GPIOs

EZ-USB enables a flexible pin configuration both on the GPIF II and the serial peripheral interfaces. Any unused control pins (except CTL[15]) on the GPIF II interface can be used as GPIOs. Similarly, any unused pins on the serial peripheral interfaces may be configured as GPIOs. See the Pin Description on page 18 for pin configuration options.

All GPIF II and GPIO pins support an external load of up to 16 pF for every pin.

EMI

FX3S meets EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. FX3S can tolerate reasonable EMI, conducted by the aggressor, outlined by these specifications and continue to function as expected.

System-level ESD

FX3S has built-in ESD protection on the D+, D–, and GND pins on the USB interface. The ESD protection levels provided on these ports are:

- ±2.2-KV human body model (HBM) based on JESD22-A114 Specification
- ±6-KV contact discharge and ±8-KV air gap discharge based on IEC61000-4-2 level 3A
- ± 8-KV Contact Discharge and ±15-KV Air Gap Discharge based on IEC61000-4-2 level 4C.

This protection ensures the device continues to function after ESD events up to the levels stated in this section.

The SSRX+, SSRX–, SSTX+, and SSTX– pins only have up to ±2.2-KV HBM internal ESD protection.

Figure 11. FX3S Ball Map (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	U3VSSQ	U3RXVDDQ	SSRXM	SSRXP	SSTXP	SSTXM	AVDD	VSS	DP	DM	NC
B	VIO4	FSLC[0]	R_USB3	FSLC[1]	U3TXVDDQ	CVDDQ	AVSS	VSS	VSS	VDD	TRST#
C	GPIO[54]	GPIO[55]	VDD	GPIO[57]	RESET#	XTALIN	XTALOUT	R_USB2	OTG_ID	TDO	VIO5
D	GPIO[50]	GPIO[51]	GPIO[52]	GPIO[53]	GPIO[56]	CLKIN_32	CLKIN	VSS	I2C_GPIO[58]	I2C_GPIO[59]	O[60]
E	GPIO[47]	VSS	VIO3	GPIO[49]	GPIO[48]	FSLC[2]	TDI	TMS	VDD	VBATT	VBUS
F	VIO2	GPIO[45]	GPIO[44]	GPIO[41]	GPIO[46]	TCK	GPIO[2]	GPIO[5]	GPIO[1]	GPIO[0]	VDD
G	VSS	GPIO[42]	GPIO[43]	GPIO[30]	GPIO[25]	GPIO[22]	GPIO[21]	GPIO[15]	GPIO[4]	GPIO[3]	VSS
H	VDD	GPIO[39]	GPIO[40]	GPIO[31]	GPIO[29]	GPIO[26]	GPIO[20]	GPIO[24]	GPIO[7]	GPIO[6]	VIO1
J	GPIO[38]	GPIO[36]	GPIO[37]	GPIO[34]	GPIO[28]	GPIO[16]	GPIO[19]	GPIO[14]	GPIO[9]	GPIO[8]	VDD
K	GPIO[35]	GPIO[33]	VSS	VSS	GPIO[27]	GPIO[23]	GPIO[18]	GPIO[17]	GPIO[13]	GPIO[12]	GPIO[10]
L	VSS	VSS	VSS	GPIO[32]	VDD	VSS	VDD	INT#	VIO1	GPIO[11]	VSS

FX3S Pin Description				
Pin	**Power Domain**	**I/O**	**Name**	**USB Port**
C9	VBUS/ VBATT	I	OTG_ID	OTG_ID
A3	U3RX VDDQ	I	SSRXM	SSRX-
A4	U3RX VDDQ	I	SSRXP	SSRX+
A6	U3TX VDDQ	O	SSTXM	SSTX-
A5	U3TX VDDQ	O	SSTXP	SSTX+
A9	VBUS/ VBATT	I/O	DP	D+
A10	VBUS/ VBATT	I/O	DM	D–
A11			NC	No connect
				Crystal/Clocks
B2	CVDDQ	I	FSLC[0]	FSLC[0]
C6	AVDD	I/O	XTALIN	XTALIN
C7	AVDD	I/O	XTALOUT	XTALOUT
B4	CVDDQ	I	FSLC[1]	FSLC[1]
E6	CVDDQ	I	FSLC[2]	FSLC[2]
D7	CVDDQ	I	CLKIN	CLKIN
D6	CVDDQ	I	CLKIN_32	CLKIN_32
				I2C and JTAG
D9	VIO5	I/O	I2C_GPIO[58]	I2C_SCL
D10	VIO5	I/O	I2C_GPIO[59]	I2C_SDA
E7	VIO5	I	TDI	TDI
C10	VIO5	O	TDO	TDO
B11	VIO5	I	TRST#	TRST#
E8	VIO5	I	TMS	TMS
F6	VIO5	I	TCK	TCK
D11	VIO5	O	O[60]	Charger detect output

FX3S Pin Description				
Pin	**Power Domain**	**I/O**	**Name**	**Power**
E10		PWR	VBATT	
B10		PWR	VDD	
A1		PWR	U3VSSQ	
E11		PWR	VBUS	
D8		PWR	VSS	
H11		PWR	VIO1	
E2		PWR	VSS	
L9		PWR	VIO1	
G1		PWR	VSS	
F1		PWR	VIO2	
G11		PWR	VSS	
E3		PWR	VIO3	
L1		PWR	VSS	
B1		PWR	VIO4	
L6		PWR	VSS	
B6		PWR	CVDDQ	
B5		PWR	U3TXVDDQ	
A2		PWR	U3RXVDDQ	
C11		PWR	VIO5	
L11		PWR	VSS	
A7		PWR	AVDD	
B7		PWR	AVSS	
C3		PWR	VDD	
B8		PWR	VSS	
E9		PWR	VDD	
B9		PWR	VSS	
F11		PWR	VDD	
H1		PWR	VDD	
L7		PWR	VDD	
J11		PWR	VDD	
L5		PWR	VDD	
K4		PWR	VSS	
L3		PWR	VSS	
K3		PWR	VSS	
L2		PWR	VSS	
A8		PWR	VSS	
				Precision Resistors
C8	VBUS/ VBATT	I/O	R_usb2	Precision resistor for USB 2.0 (Connect a 6.04 kΩ ±1% resistor between this pin and GND)
B3	U3TX VDDQ	I/O	R_usb3	Precision resistor for USB 3.0 (Connect a 200 Ω ±1% resistor between this pin and GND)

DC Specifications (continued)

Parameter	Description	Min	Max	Units	Notes
V_{IL}	Input LOW voltage	–0.3	0.25 × V_{CC}	V	V_{CC} is the corresponding I/O voltage supply.
V_{OH}	Output HIGH voltage	0.9 × V_{CC}	–	V	I_{OH} (max) = –100 µA tested at quarter drive strength. V_{CC} is the corresponding I/O voltage supply.
V_{OL}	Output LOW voltage	–	0.1 × VCC	V	I_{OL} (min) = +100 µA tested at quarter drive strength. V_{CC} is the corresponding I/O voltage supply.
I_{IX}	Input leakage current for all pins except SSTXP/SSXM/SSRXP/SSRXM	–1	1	µA	All I/O signals held at V_{DDQ} (For I/Os with a pull-up or pull-down resistor connected, the leakage current increases by V_{DDQ}/R_{pu} or V_{DDQ}/R_{PD}
I_{OZ}	Output High-Z leakage current for all pins except SSTXP/ SSXM/ SSRXP/SSRXM	–1	1	µA	All I/O signals held at V_{DDQ}
I_{CC} Core	Core and analog voltage operating current	–	200	mA	Total current through A_{VDD}, V_{DD}
I_{CC} USB	USB voltage supply operating current	–	60	mA	
I_{SB1}	Total suspend current during suspend mode with USB 3.0 PHY enabled (L1)	–	–	mA	Core current: 1.5 mA I/O current: 20 µA USB current: 2 mA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB2}	Total suspend current during suspend mode with USB 3.0 PHY disabled (L2)	–	–	mA	Core current: 250 µA I/O current: 20 µA USB current: 1.2 mA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB3}	Total standby current during standby mode (L3)	–	–	µA	Core current: 60 µA I/O current: 20 µA USB current: 40 µA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB4}	Total standby current during core power-down mode (L4)	–	–	µA	Core current: 0 µA I/O current: 20 µA USB current: 40 µA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C.)
V_{RAMP}	Voltage ramp rate on core and I/O supplies	0.2	50	V/ms	Voltage ramp must be monotonic
V_N	Noise level permitted on V_{DD} and I/O supplies	–	100	mV	Max p-p noise level permitted on all supplies except A_{VDD}
V_{N_AVDD}	Noise level permitted on A_{VDD} supply	–	20	mV	Max p-p noise level permitted on A_{VDD}

AC Timing Parameters

GPIF II Timing

Figure 12. GPIF II Timing in Synchronous Mode

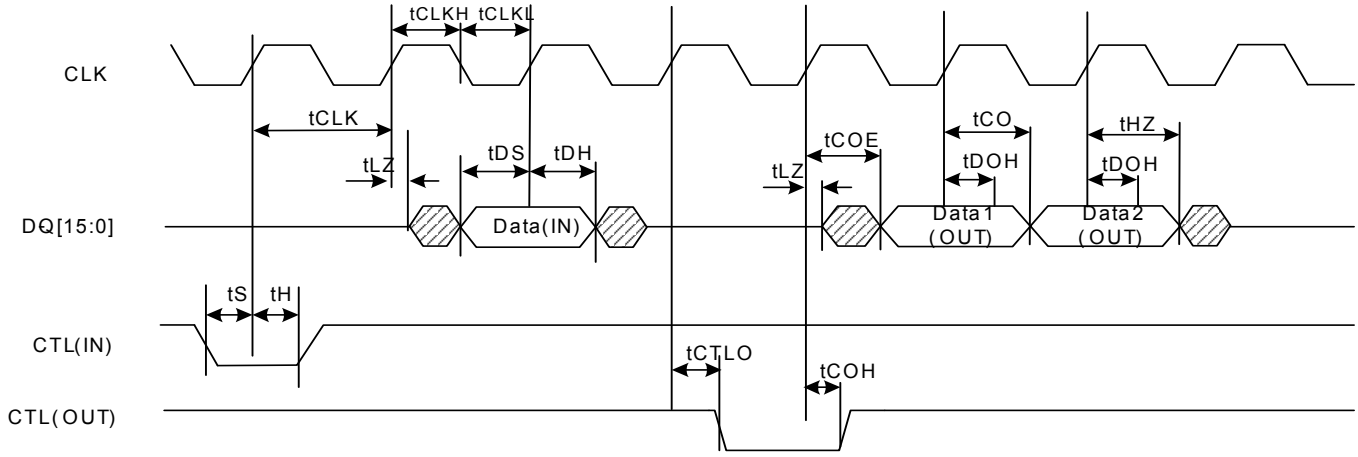


Table 7. GPIF II Timing Parameters in Synchronous Mode [3]

Parameter	Description	Min	Max	Units
Frequency	Interface clock frequency	–	100	MHz
tCLK	Interface clock period	10	–	ns
tCLKH	Clock high time	4	–	ns
tCLKL	Clock low time	4	–	ns
tS	CTL input to clock setup time (Sync speed = 1)	2	–	ns
tH	CTL input to clock hold time (Sync speed = 1)	0.5	–	ns
tDS	Data in to clock setup time (Sync speed = 1)	2	–	ns
tDH	Data in to clock hold time (Sync speed = 1)	0.5	–	ns
tCO	Clock to data out propagation delay when DQ bus is already in output direction (Sync speed = 1)	–	8	ns
tCOE	Clock to data out propagation delay when DQ lines change to output from tristate and valid data is available on the DQ bus (Sync speed = 1)	-	9	
tCTLO	Clock to CTL out propagation delay (Sync speed = 1)	–	8	ns
tDOH	Clock to data out hold	2	–	ns
tCOH	Clock to CTL out hold	0	–	ns
tHZ	Clock to high-Z	–	8	ns
tLZ	Clock to low-Z (Sync speed = 1)	0	–	ns
tS_ss0	CTL input/data input to clock setup time (Sync speed = 0)	5	–	ns
tH_ss0	CTL input/data input to clock hold time (Sync speed = 0)	2.5	–	ns
tCO_ss0	Clock to data out / CTL out propagation delay (sync speed = 0)	–	15	ns
tLZ_ss0	Clock to low-Z (sync speed = 0)	2	–	ns

Note
3. All parameters guaranteed by design and validated through characterization.

Table 8. GPIF II Timing in Asynchronous Mode [4]

Note The following parameters assume one state transition.

Parameter	Description	Min	Max	Units
tDS	Data In to DLE setup time. Valid in DDR async mode.	2.3	–	ns
tDH	Data In to DLE hold time. Valid in DDR async mode.	2	–	ns
tAS	Address In to ALE setup time	2.3	–	ns
tAH	Address In to ALE hold time	2	–	ns
tCTLassert	CTL I/O asserted width for CTRL inputs without DQ input association and for outputs.	7	–	ns
tCTLdeassert	CTL I/O deasserted width for CTRL inputs without DQ input association and for outputs.	7	–	ns
tCTLassert_DQassert	CTL asserted pulse width for CTL inputs that signify DQ inputs valid at the asserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	20	–	ns
tCTLdeassert_DQassert	CTL deasserted pulse width for CTL inputs that signify DQ input valid at the asserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	7	–	ns
tCTLassert_DQdeassert	CTL asserted pulse width for CTL inputs that signify DQ inputs valid at the deasserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	7	–	ns
tCTLdeassert_DQdeassert	CTL deasserted pulse width for CTL inputs that signify DQ inputs valid at the deasserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	20	–	ns
tCTLassert_DQlatch	CTL asserted pulse width for CTL inputs that employ in-built latches (ALE/DLE) to latch the DQ inputs. In this non-DDR case, in-built latches are always close at the deasserting edge.	7	–	ns
tCTLdeassert_DQlatch	CTL deasserted pulse width for CTL inputs that employ in-built latches (ALE/DLE) to latch the DQ inputs. In this non-DDR case, in-built latches always close at the deasserting edge.	10	–	ns
tCTLassert_DQlatchDDR	CTL asserted pulse width for CTL inputs that employ in-built latches (DLE) to latch the DQ inputs in DDR mode.	10	–	ns
tCTLdeassert_DQlatchDDR	CTL deasserted pulse width for CTL inputs that employ in-built latches (DLE) to latch the DQ inputs in DDR mode.	10	–	ns
tAA	DQ/CTL input to DQ output time when DQ change or CTL change needs to be detected and affects internal updates of input and output DQ lines.	–	30	ns
tDO	CTL to data out when the CTL change merely enables the output flop update whose data was already established.	–	25	ns
tOELZ	CTL designated as OE to low-Z. Time when external devices should stop driving data.	0	–	ns
tOEHZ	CTL designated as OE to high-Z	8	8	ns
tCLZ	CTL (non-OE) to low-Z. Time when external devices should stop driving data.	0	–	ns
tCHZ	CTL (non-OE) to high-Z	30	30	ns
tCTLalpha	CTL to alpha change at output	–	25	ns
tCTLbeta	CTL to beta change at output	–	30	ns
tDST	Addr/data setup when DLE/ALE not used	2	–	ns
tDHT	Addr/data hold when DLE/ALE not used	20	–	ns

Note
4. All parameters guaranteed by design and validated through characterization.

Figure 16. Non-multiplexed Asynchronous SRAM Write Timing (WE# and CE# Controlled)

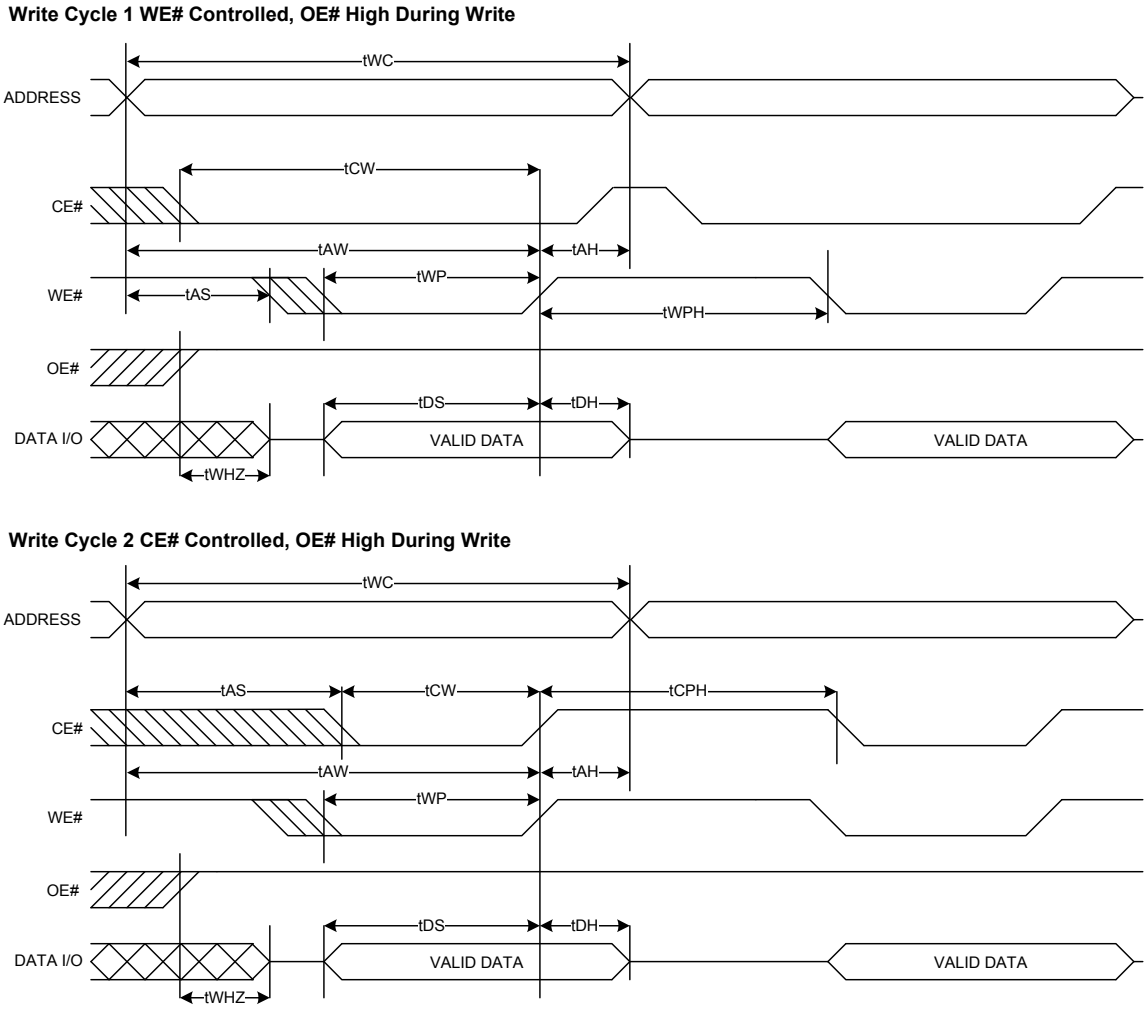
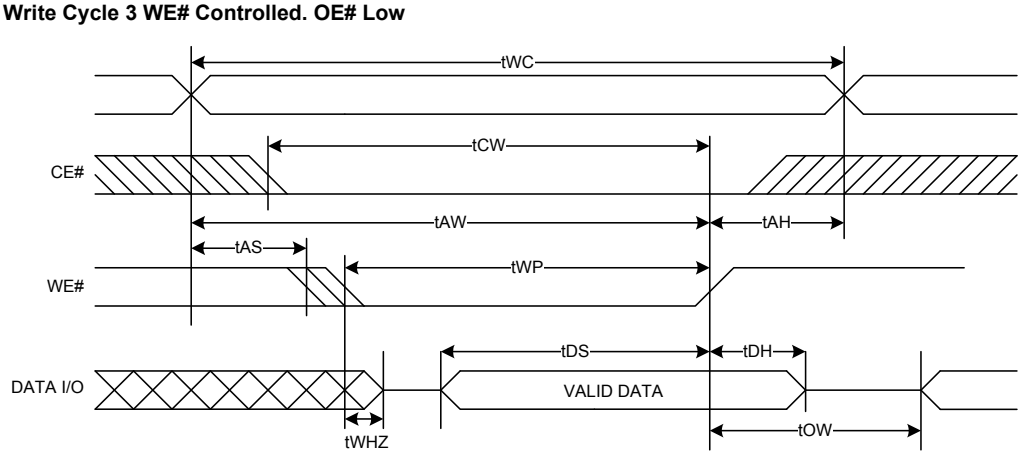


Figure 17. Non-multiplexed Asynchronous SRAM Write Timing (WE# Controlled, OE# LOW)



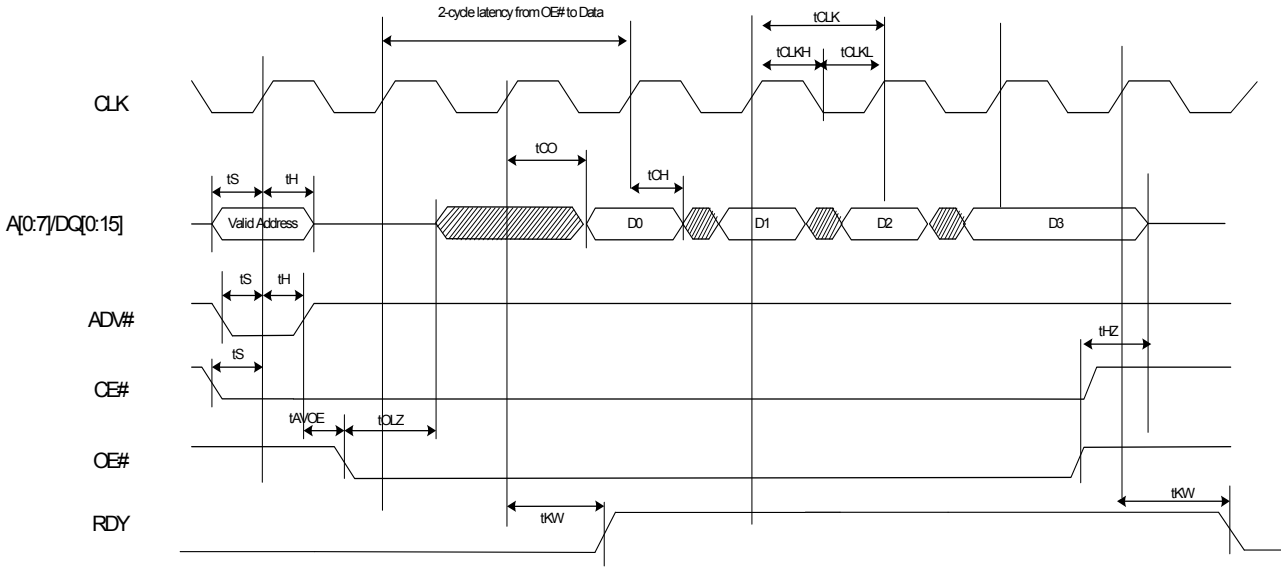
Note: tWP must be adjusted such that tWP > tWHZ + tDS

Table 9. Asynchronous SRAM Timing Parameters[5]

Parameter	Description	Min	Max	Units
–	SRAM interface bandwidth	–	61.5	MBps
tRC	Read cycle time	32.5	–	ns
tAA	Address to data valid	–	30	ns
tAOS	Address to OE# LOW setup time	7	–	ns
tOH	Data output hold from address change	3	–	ns
tOHH	OE# HIGH hold time	7.5	–	ns
tOHC	OE# HIGH to CE# HIGH	2	–	ns
tOE	OE# LOW to data valid	–	25	ns
tOLZ	OE# LOW to LOW-Z	0	–	ns
tWC	Write cycle time	30	–	ns
tCW	CE# LOW to write end	30	–	ns
tAW	Address valid to write end	30	–	ns
tAS	Address setup to write start	7	–	ns
tAH	Address hold time from CE# or WE#	2	–	ns
tWP	WE# pulse width	20	–	ns
tWPH	WE# HIGH time	10	–	ns
tCPH	CE# HIGH time	10	–	ns
tDS	Data setup to write end	7	–	ns
tDH	Data hold to write end	2	–	ns
tWHZ	Write to DQ HIGH-Z output	–	22.5	ns
tOEZ	OE# HIGH to DQ HIGH-Z output	–	22.5	ns
tOW	End of write to LOW-Z output	0	–	ns

Note
5. All parameters guaranteed by design and validated through characterization.

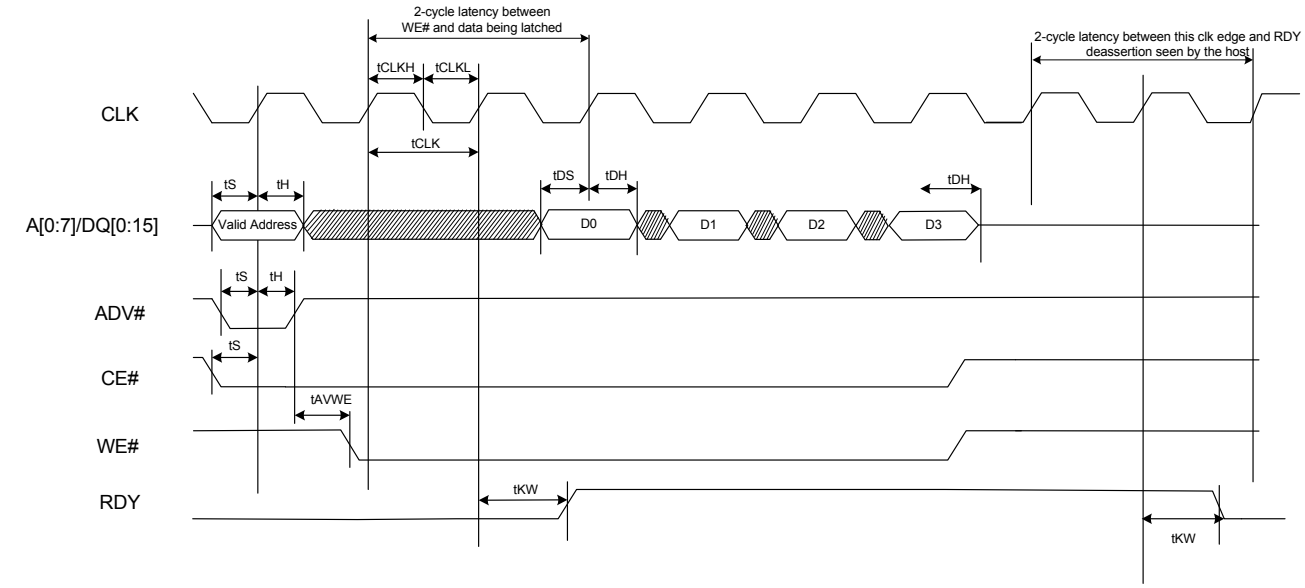
Figure 22. Synchronous ADMux Interface – Burst Read Timing



Note:

1) External P-Port processor and FX3S work operate on the same clock edge
2) External processor sees RDY assert 2 cycles after OE # asserts andand sees RDY deassert a cycle after the last burst data appears on the output
3) Valid output data appears 2 cycle after OE # asserted. The last burst data is held until OE # deasserts
4) Burst size of 4 is shown. Transfer size for the operation must be a multiple of burst size. Burst size is usually power of 2. RDY will not deassert in the middle of the burst.
5) External processor cannot deassert OE in the middle of a burst. If it does so, any bytes remaining in the burst packet could get lost.
6) Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

Figure 23. Sync ADMux Interface – Burst Write Timing



Note:

1) External P-Port processor and FX3S operate on the same clock edge
2) External processor sees RDY assert 2 cycles after WE # asserts and deasserts 3 cycles after the edge sampling the last burst data.
3) Transfer size for the operation must be a multiple of burst size. Burst size is usually power of 2. RDY will not deassert in the middle of the burst. Burst size of 4 is shown
4) External processor cannot deassert WE in the middle of a burst. If it does so, any bytes remaining in the burst packet could get lost.
5)Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

Table 11. Synchronous ADMux Timing Parameters[7]

Parameter	Description	Min	Max	Unit
FREQ	Interface clock frequency	–	100	MHz
tCLK	Clock period	10	–	ns
tCLKH	Clock HIGH time	4	–	ns
tCLKL	Clock LOW time	4	–	ns
tS	CE#/WE#/DQ setup time	2	–	ns
tH	CE#/WE#/DQ hold time	0.5	–	ns
tCH	Clock to data output hold time	0	–	ns
tDS	Data input setup time	2	–	ns
tDH	Clock to data input hold	0.5	–	ns
tAVDOE	ADV# HIGH to OE# LOW	0	–	ns
tAVDWE	ADV# HIGH to WE# LOW	0	–	ns
tHZ	CE# HIGH to Data HIGH-Z	–	8	ns
tOHZ	OE# HIGH to Data HIGH-Z	–	8	ns
tOLZ	OE# LOW to Data LOW-Z	0	–	ns
tKW	Clock to RDY valid	–	8	ns

Note
7. All parameters guaranteed by design and validated through characterization.

Slave FIFO Interface

Synchronous Slave FIFO Sequence Description

- FIFO address is stable and SLCS is asserted
- FLAG indicates FIFO not empty status
- SLOE is asserted. SLOE is an output-enable only, whose sole function is to drive the data bus.
- SLRD is asserted

The FIFO pointer is updated on the rising edge of the PCLK, while the SLRD is asserted. This starts the propagation of data from the newly addressed location to the data bus. After a propagation delay of tco (measured from the rising edge of PCLK), the new data value is present. N is the first data value read from the FIFO. To have data on the FIFO data bus, SLOE must also be asserted.

The same sequence of events is shown for a burst read.

FLAG Usage:

The FLAG signals are monitored for flow control by the external processor. FLAG signals are outputs from FX3 that may be configured to show empty, full, or partial status for a dedicated thread or the current thread that is addressed.

Socket Switching Delay (Tssd):

The socket-switching delay is measured from the time EPSWITCH# is asserted by the master, with the new socket address on the address bus, to the time the Current_Thread_DMA_Ready flag is asserted. For the Producer socket, the flag is asserted when it is ready to receive data in the DMA buffer. For the Consumer socket, the flag is asserted when it is ready to drive data out of the DMA buffer. For a synchronous slave FIFO interface, the switching delay is measured in the number of GPIF interface clock cycles; for an asynchronous slave FIFO interface, in PIB clock cycles. This is applicable only for the 5-bit Slave FIFO interface; there is no socket-switching delay in FX3's 2-bit Slave FIFO interface, which makes use of thread switching in the GPIF™ II state machine.

Note For burst mode, the SLRD# and SLOE# are asserted during the entire duration of the read. When SLOE# is asserted, the data bus is driven (with data from the previously addressed FIFO). For each subsequent rising edge of PCLK, while the SLRD# is asserted, the FIFO pointer is incremented and the next data value is placed on the data bus.

Figure 24. Synchronous Slave FIFO Read Mode

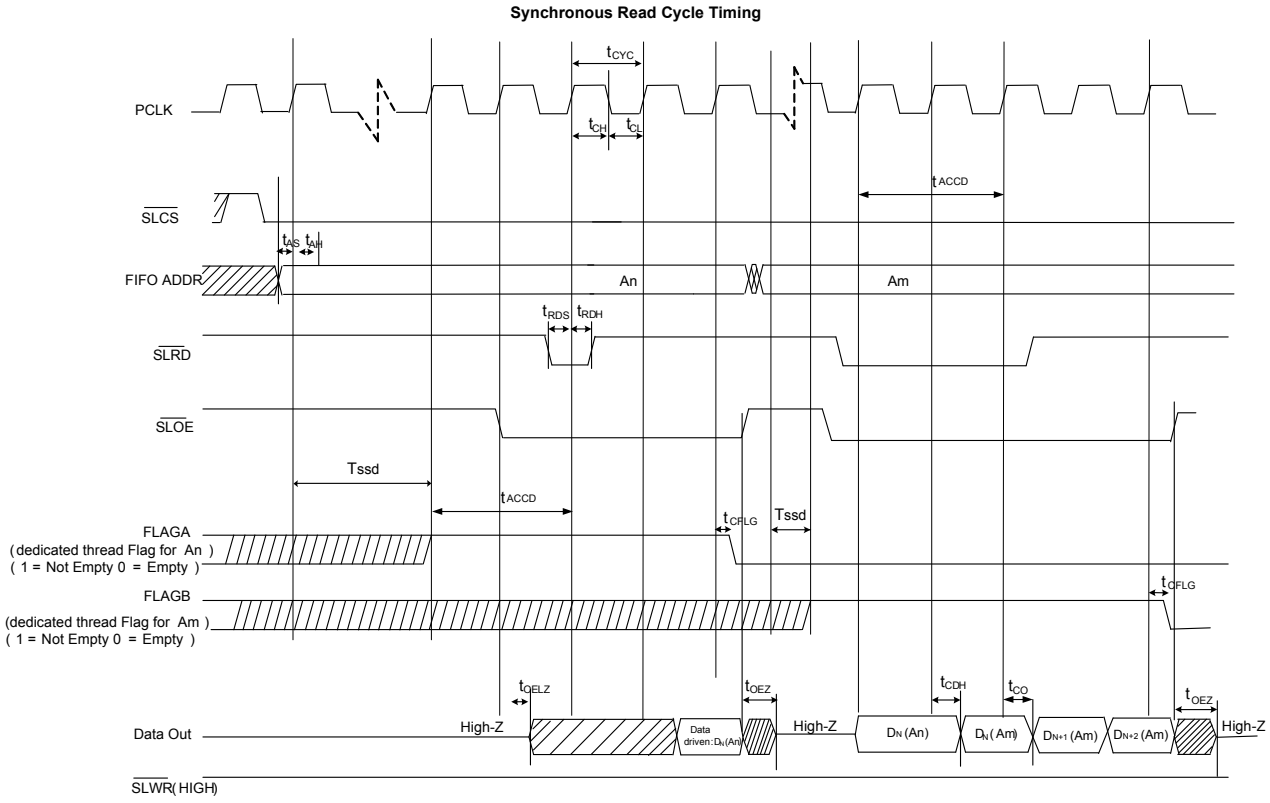


Table 12. Synchronous Slave FIFO Parameters[8]

Parameter	Description	Min	Max	Units
FREQ	Interface clock frequency	–	100	MHz
tCYC	Clock period	10	–	ns
tCH	Clock high time	4	–	ns
tCL	Clock low time	4	–	ns
tRDS	SLRD# to CLK setup time	2	–	ns
tRDH	SLRD# to CLK hold time	0.5	–	ns
tWRS	SLWR# to CLK setup time	2	–	ns
tWRH	SLWR# to CLK hold time	0.5	–	ns
tCO	Clock to valid data	–	8	ns
tDS	Data input setup time	2	–	ns
tDH	CLK to data input hold	0.5	–	ns
tAS	Address to CLK setup time	2	–	ns
tAH	CLK to address hold time	0.5	–	ns
tOELZ	SLOE# to data low-Z	0	–	ns
tCFLG	CLK to flag output propagation delay	–	8	ns
tOEZ	SLOE# deassert to Data Hi Z	–	8	ns
tPES	PKTEND# to CLK setup	2	–	ns
tPEH	CLK to PKTEND# hold	0.5	–	ns
tCDH	CLK to data output hold	2	–	ns
tSSD	Socket switching delay	2	68	Clock cycles
tACCD	Latency from SLRD# to Data	2	2	Clock cycles
tFAD	Latency from SLWR# to FLAG	3	3	Clock cycles
Note Three-cycle latency from ADDR to DATA/FLAGS				

Asynchronous Slave FIFO Read Sequence Description

- FIFO address is stable and the SLCS# signal is asserted.
- SLOE# is asserted. This results in driving the data bus.
- SLRD # is asserted.
- Data from the FIFO is driven after assertion of SLRD#. This data is valid after a propagation delay of tRDO from the falling edge of SLRD#.
- FIFO pointer is incremented on deassertion of SLRD#

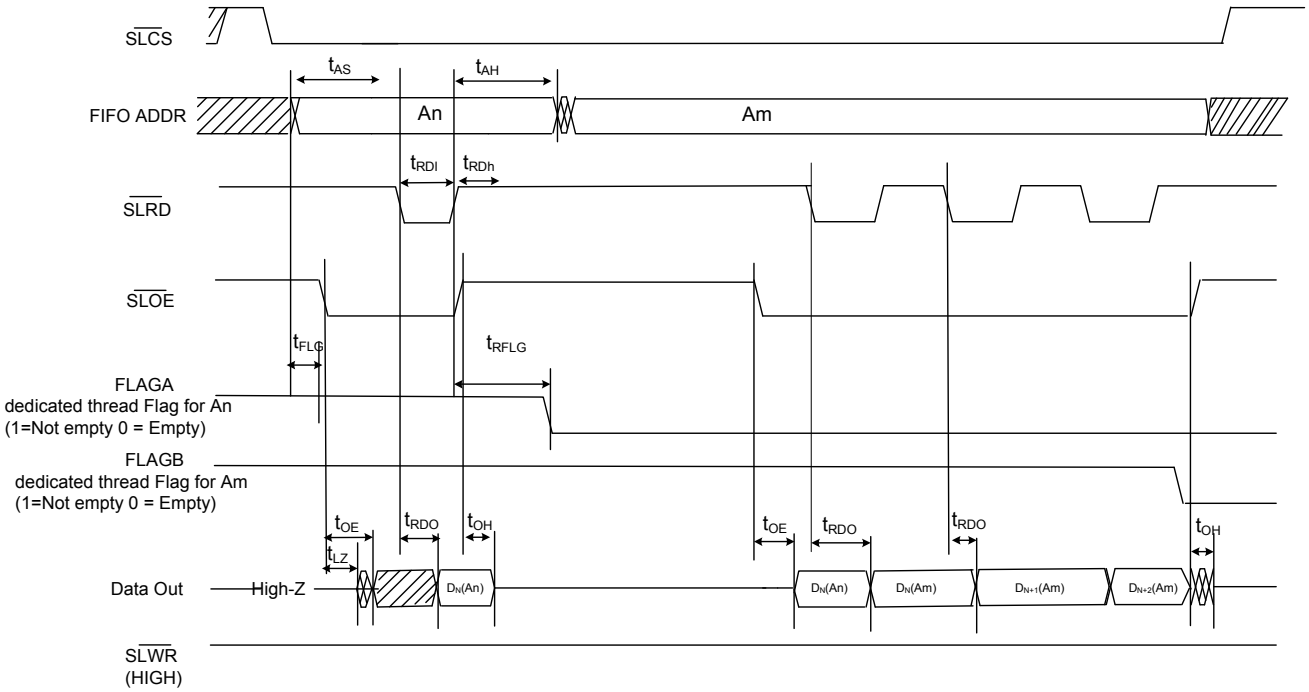
In Figure 26 on page 38, data N is the first valid data read from the FIFO. For data to appear on the data bus during the read cycle, SLOE# must be in an asserted state. SLRD# and SLOE# can also be tied.

The same sequence of events is also shown for a burst read.

Note In the burst read mode, during SLOE# assertion, the data bus is in a driven state (data is driven from a previously addressed FIFO). After assertion of SLRD# data from the FIFO is driven on the data bus (SLOE# must also be asserted). The FIFO pointer is incremented after deassertion of SLRD#.

Note
8. All parameters guaranteed by design and validated through characterization.

Figure 26. Asynchronous Slave FIFO Read Mode



Asynchronous Slave FIFO Write Sequence Description

- FIFO address is driven and SLCS# is asserted
- SLWR# is asserted. SLCS# must be asserted with SLWR# or before SLWR# is asserted
- Data must be present on the tWRS bus before the deasserting edge of SLWR#
- Deassertion of SLWR# causes the data to be written from the data bus to the FIFO, and then the FIFO pointer is incremented
- The FIFO flag is updated after the tWFLG from the deasserting edge of SLWR.

The same sequence of events is shown for a burst write.

Note that in the burst write mode, after SLWR# deassertion, the data is written to the FIFO, and then the FIFO pointer is incremented.

Short Packet: A short packet can be committed to the USB host by using the PKTEND#. The external device or processor should be designed to assert the PKTEND# along with the last word of data and SLWR# pulse corresponding to the last word. The FIFOADDR lines must be held constant during the PKTEND# assertion.

Zero-Length Packet: The external device or processor can signal a zero-length packet (ZLP) to FX3S simply by asserting PKTEND#, without asserting SLWR#. SLCS# and the address must be driven as shown in Figure 27 on page 39.

FLAG Usage: The FLAG signals are monitored by the external processor for flow control. FLAG signals are FX3S outputs that can be configured to show empty, full, and partial status for a dedicated address or the current address.

Serial Peripherals Timing

I^2C Timing

Figure 28. I^2C Timing Definition

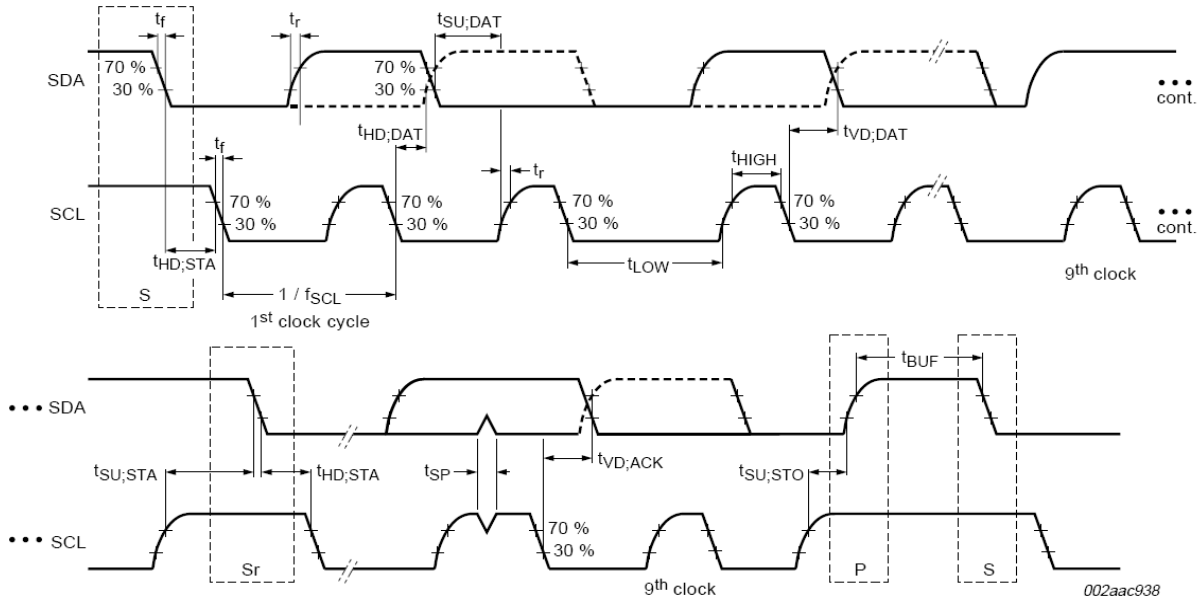


Table 15. I²C Timing Parameters[11]

Parameter	Description	Min	Max	Units
I²C Standard Mode Parameters				
fSCL	SCL clock frequency	0	100	kHz
tHD:STA	Hold time START condition	4	–	µs
tLOW	LOW period of the SCL	4.7	–	µs
tHIGH	HIGH period of the SCL	4	–	µs
tSU:STA	Setup time for a repeated START condition	4.7	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	250	–	ns
tr	Rise time of both SDA and SCL signals	–	1000	ns
tf	Fall time of both SDA and SCL signals	–	300	ns
tSU:STO	Setup time for STOP condition	4	–	µs
tBUF	Bus free time between a STOP and START condition	4.7	–	µs
tVD:DAT	Data valid time	–	3.45	µs
tVD:ACK	Data valid ACK	–	3.45	µs
tSP	Pulse width of spikes that must be suppressed by input filter	n/a	n/a	
I²C Fast Mode Parameters				
fSCL	SCL clock frequency	0	400	kHz
tHD:STA	Hold time START condition	0.6	–	µs
tLOW	LOW period of the SCL	1.3	–	µs
tHIGH	HIGH period of the SCL	0.6	–	µs
tSU:STA	Setup time for a repeated START condition	0.6	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	100	–	ns
tr	Rise time of both SDA and SCL signals	–	300	ns
tf	Fall time of both SDA and SCL signals	–	300	ns
tSU:STO	Setup time for STOP condition	0.6	–	µs
tBUF	Bus free time between a STOP and START condition	1.3	–	µs
tVD:DAT	Data valid time	–	0.9	µs
tVD:ACK	Data valid ACK	–	0.9	µs
tSP	Pulse width of spikes that must be suppressed by input filter	0	50	ns
I²C Fast Mode Plus Parameters (Not supported at I2C_VDDQ=1.2 V)				
fSCL	SCL clock frequency	0	1000	kHz
tHD:STA	Hold time START condition	0.26	–	µs
tLOW	LOW period of the SCL	0.5	–	µs
tHIGH	HIGH period of the SCL	0.26	–	µs
tSU:STA	Setup time for a repeated START condition	0.26	–	µs

Note
11. All parameters guaranteed by design and validated through characterization.

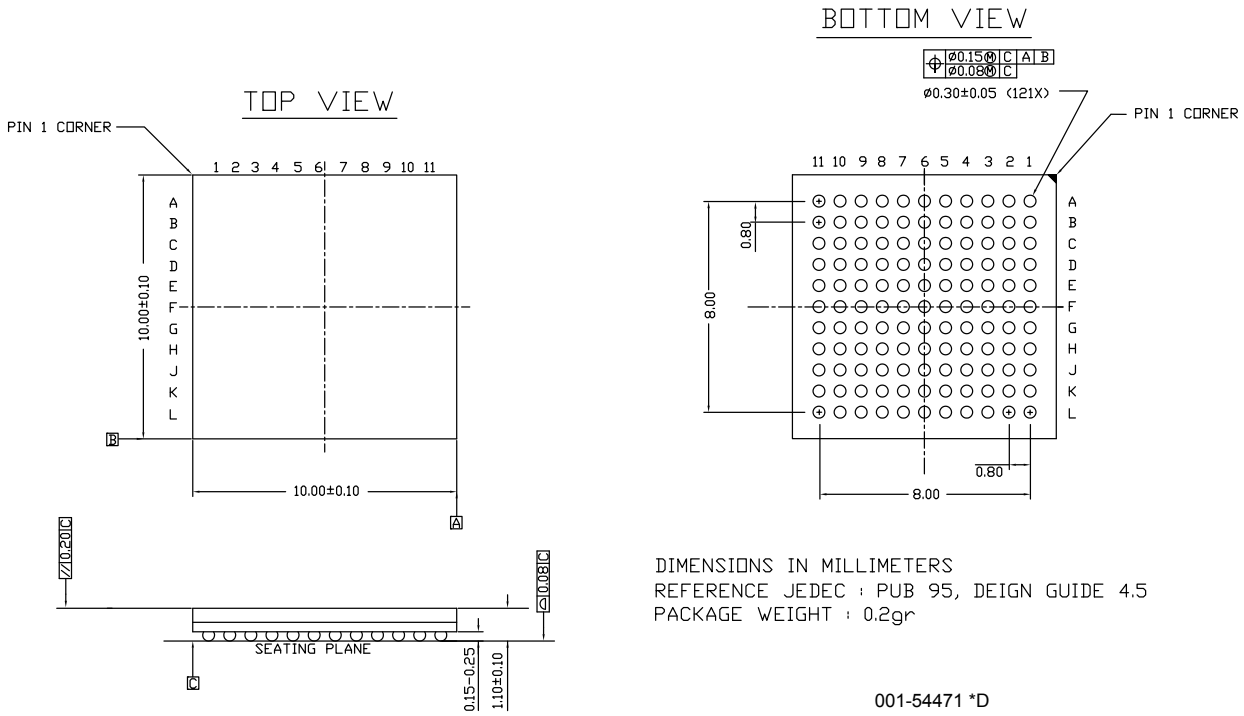
Table 17. SPI Timing Parameters[13]

Parameter	Description	Min	Max	Units
fop	Operating frequency	0	33	MHz
tsck	Cycle time	30	–	ns
twsck	Clock high/low time	13.5	–	ns
tlead	SSN-SCK lead time	1/2 tsck[14]-5	1.5 tsck[14]+ 5	ns
tlag	Enable lag time	0.5	1.5 tsck[14]+5	ns
trf	Rise/fall time	–	8	ns
tsdd	Output SSN to valid data delay time	–	5	ns
tdv	Output data valid time	–	5	ns
tdi	Output data invalid	0	–	ns
tssnh	Minimum SSN high time	10	–	ns
tsdi	Data setup time input	8	–	ns
thoi	Data hold time input	0	–	ns
tdis	Disable data output on SSN high	0	–	ns

Notes
13. All parameters guaranteed by design and validated through characterization.
14. Depends on LAG and LEAD setting in the SPI_CONFIG register.

Package Diagram

Figure 32. 121-ball FBGA (10 × 10 × 1.2 mm (0.30 mm Ball Diameter)) Package Outline, 001-54471



Acronyms

Acronym	Description
DMA	Direct Memory Access
HNP	Host Negotiation Protocol
MMC	Multimedia Card
MTP	Media Transfer Protocol
PLL	Phase Locked Loop
PMIC	Power Management IC
SD	Secure Digital
SDIO	Secure Digital Input/Output
SLC	Single-Level Cell
SLCS	Slave Chip Select
SLOE	Slave Output Enable
SLRD	Slave Read
SLWR	Slave Write
SPI	Serial Peripheral Interface
SRP	Session Request Protocol
USB	Universal Serial Bus
WLCSP	Wafer Level Chip Scale Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Mbps	megabits per second
MBps	megabytes per second
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt