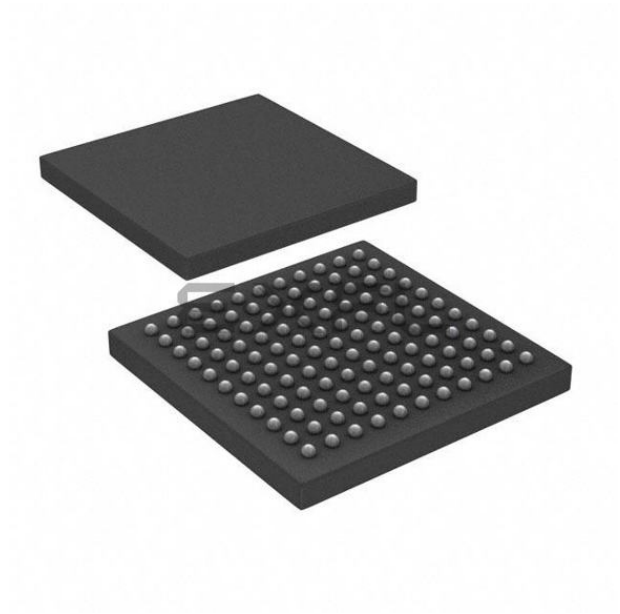

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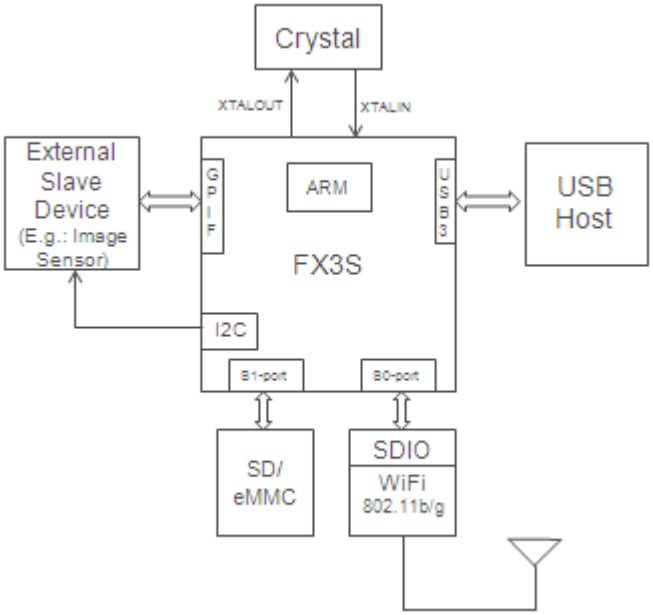
Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Host/Peripheral Controller
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	CYUSB
RAM Size	512K x 8
Interface	GPIF, I²C, I²S, MMC/SD/SDIO, SPI, UART, USB
Number of I/O	60
Voltage - Supply	1.15V ~ 1.25V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-FBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyusb3033-bzxc

Figure 2. EZ-USB FX3S as Main Processor



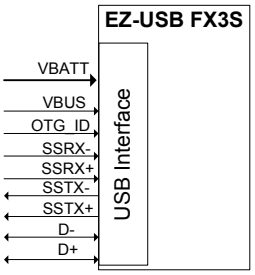
USB Interface

FX3S complies with the following specifications and supports the following features:

- Supports USB peripheral functionality compliant with the USB 3.0 Specification Revision 1.0 and is also backward compatible with the USB 2.0 Specification.
- Complies with OTG Supplement Revision 2.0. It supports High-Speed, Full-Speed, and Low-Speed OTG dual-role device capability. As a peripheral, FX3S is capable of SuperSpeed, High-Speed, and Full-Speed. As a host, it is capable of High-Speed, Full-Speed, and Low-Speed.
- Supports Carkit Pass-Through UART functionality on USB D+/D– lines based on the CEA-936A specification.
- Supports up to 16 IN and 16 OUT endpoints.
- Supports the USB 3.0 Streams feature. It also supports USB Attached SCSI (UAS) device-class to optimize mass-storage access performance.
- As a USB peripheral, FX3S supports UAS, USB Video Class (UVC), Mass Storage Class (MSC), and Media Transfer Protocol (MTP) USB peripheral classes. As a USB peripheral, all other device classes are supported only in the pass-through mode when handled entirely by a host processor external to the device.
- As an OTG host, FX3S supports MSC and HID device classes.

Note When the USB port is not in use, disable the PHY and transceiver to save power.

Figure 3. USB Interface Signals



OTG

FX3S is compliant with the OTG Specification Revision 2.0. In the OTG mode, FX3S supports both A and B device modes and supports Control, Interrupt, Bulk, and Isochronous data transfers.

FX3S requires an external charge pump (either standalone or integrated into a PMIC) to power VBUS in the OTG A-device mode.

The Target Peripheral List for OTG host implementation consists of MSC- and HID-class devices.

FX3S does not support Attach Detection Protocol (ADP).

The MMC slave interface features are as follows:

- Interface operations are compatible with the MMC-System Specification, MMCA Technical Committee, Version 4.2.
- Supports booting from an eMMC device connected to the S-Port. This feature is supported for eMMC devices operating up to 52-MHz SDR.
- Supports PMMC interface voltage ranges of 1.7 V to 1.95 V and 2.7 V to 3.6 V.
- Supports open drain (both drive and receive open drain signals) on CMD pin to allow GO_IRQ_STATE (CMD40) for PMMC.
- Interface clock-frequency range: 0 to 52 MHz.
- Supports 1-bit, 4-bit, or 8-bit mode of operation. This configuration is determined by the MMC initialization procedure.
- FX3S responds to standard initialization phase commands as specified for the MMC 4.2 slave device.
- PMMC mode MMC 4.2 command classes: Class 0 (Basic), Class 2 (Block read), and Class 4 (Block write), Class 9 (I/O).

FX3S supports the following PMMC commands:

- Class 0: Basic

  CMD0, CMD1, CMD2, CMD3, CMD4, CMD6, CMD7, CMD8, CMD9, CMD10, CMD12, CMD13, CMD15, CMD19, CMD5 (wakeup support)
- Class 2: Block Read

  CMD16, CMD17, CMD18, CMD23
- Class 4: Block Write

  CMD16, CMD23, CMD24, CMD25
- Class 9: I-O

  CMD39, CMD40

Boot Options

FX3S can load boot images from various sources, selected by the configuration of the PMODE pins. Following are the FX3S boot options:

- Boot from USB
- Boot from I^2C
- Boot from SPI (SPI devices supported are M25P16 (16 Mbit), M25P80 (8 Mbit), and M25P40 (4 Mbit)) or their equivalents
- Boot from eMMC (S0-port)
- Boot from GPIF II ASync ADMux mode
- Boot from GPIF II Sync ADMux mode
- Boot from GPIF II ASync SRAM mode
- Boot from PMMC (P-Port)

Table 2. FX3S Booting Options

PMODE[2:0] [2]	Boot From
F00	Sync ADMux (16-bit)
F01	Async ADMux (16-bit)
F10	PMMC Legacy
F11	USB boot
F0F	Async SRAM (16-bit)
F1F	I^2C, On Failure, USB Boot is Enabled
1FF	I^2C only
0F1	SPI, On Failure, USB Boot is Enabled
000	S0-Port (eMMC) On failure, USB boot is enabled
100	S0-port (eMMC)

Reset

Hard Reset

A hard reset is initiated by asserting the Reset# pin on FX3S. The specific reset sequence and timing requirements are detailed in Figure 31 on page 49 and Table 18 on page 49. All I/Os are tristated during a hard reset.

Soft Reset

In a soft reset, the processor sets the appropriate bits in the PP_INIT control register. There are two types of Soft Reset:

- CPU Reset – The CPU Program Counter is reset. Firmware does not need to be reloaded following a CPU Reset.
- Whole Device Reset – This reset is identical to Hard Reset.
- The firmware must be reloaded following a Whole Device Reset.

Note
2. F indicates Floating.

Power

FX3S has the following power supply domains:

- **IO_VDDQ**: This is a group of independent supply domains for digital I/Os. The voltage level on these supplies is 1.8 V to 3.3 V. FX3S provides six independent supply domains for digital I/Os listed as follows (see Pin Description on page 18 for details on each of the power domain signals):
  - VIO1: GPIF II I/O
  - VIO2: S0-Port Supply
  - VIO3: S1-Port Supply
  - VIO4: S1-Port and Low Speed Peripherals (UART/SPI/I2S) Supply
  - VIO5: I^2C and JTAG (supports 1.2 V to 3.3 V)
  - CVDDQ: Clock
  - V_{DD}: This is the supply voltage for the logic core. The nominal supply-voltage level is 1.2 V. This supplies the core logic circuits. The same supply must also be used for the following:
    - AVDD: This is the 1.2-V supply for the PLL, crystal oscillator, and other core analog circuits
    - U3TXVDDQ/U3RXVDDQ: These are the 1.2-V supply voltages for the USB 3.0 interface.
- VBATT/VBUS: This is the 3.2-V to 6-V battery power supply for the USB I/O and analog circuits. This supply powers the USB transceiver through FX3S's internal voltage regulator. VBATT is internally regulated to 3.3 V.

Power Modes

FX3S supports the following power modes:

- Normal mode: This is the full-functional operating mode. The internal CPU clock and the internal PLLs are enabled in this mode.
  - Normal operating power consumption does not exceed the sum of I_{CC} Core max and I_{CC} USB max (see the DC Specifications table for current consumption specifications).
  - The I/O power supplies VIO2, VIO3, VIO4, and VIO5 can be turned off when the corresponding interface is not in use. VIO1 cannot be turned off at any time if the GPIF II interface is used in the application.
- Low-power modes (see Table 6):
  - Suspend mode with USB 3.0 PHY enabled (L1)
  - Suspend mode with USB 3.0 PHY disabled (L2)
  - Standby mode (L3)
  - Core power-down mode (L4)

Table 6. Entry and Exit Methods for Low-Power Modes

Low-Power Mode	Characteristics	Methods of Entry	Methods of Exit
Suspend Mode with USB 3.0 PHY Enabled (L1)	■ The power consumption in this mode does not exceed ISB_1 ■ USB 3.0 PHY is enabled and is in U3 mode (one of the suspend modes defined by the USB 3.0 specification). This one block alone is operational with its internal clock while all other clocks are shut down ■ All I/Os maintain their previous state ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually ■ The states of the configuration registers, buffer memory, and all internal RAM are maintained ■ All transactions must be completed before FX3S enters Suspend mode (state of outstanding transactions are not preserved) ■ The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion) because the program counter does not reset	■ Firmware executing on ARM926EJ-S core can put FX3S into suspend mode. For example, on USB suspend condition, firmware may decide to put FX3S into suspend mode ■ External Processor, through the use of mailbox registers, can put FX3S into suspend mode	■ D+ transitioning to low or high ■ D- transitioning to low or high ■ Impedance change on OTG_ID pin ■ Resume condition on SSRX± ■ Detection of VBUS ■ Level detect on UART_CTS (programmable polarity) ■ GPIF II interface assertion of CTL[0] ■ Assertion of RESET#

FX3S Pin Description										
Pin	Power Domain	I/O	Name	S0-Port						
				8b MMC		SD+GPIO		GPIO		
K2	VIO2	I/O	GPIO[33]	S0_SD0		S0_SD0		GPIO		
J4	VIO2	I/O	GPIO[34]	S0_SD1		S0_SD1		GPIO		
K1	VIO2	I/O	GPIO[35]	S0_SD2		S0_SD2		GPIO		
J2	VIO2	I/O	GPIO[36]	S0_SD3		S0_SD3		GPIO		
J3	VIO2	I/O	GPIO[37]	S0_SD4		GPIO		GPIO		
J1	VIO2	I/O	GPIO[38]	S0_SD5		GPIO		GPIO		
H2	VIO2	I/O	GPIO[39]	S0_SD6		GPIO		GPIO		
H3	VIO2	I/O	GPIO[40]	S0_SD7		GPIO		GPIO		
F4	VIO2	I/O	GPIO[41]	S0_CMD		S0_CMD		GPIO		
G2	VIO2	I/O	GPIO[42]	S0_CLK		S0_CLK		GPIO		
G3	VIO2	I/O	GPIO[43]	S0_WP		S0_WP		GPIO		
F3	VIO2	I/O	GPIO[44]	S0S1_INS		S0S1_INS		GPIO		
F2	VIO2	I/O	GPIO[45]	MMC0_RST_OUT		GPIO		GPIO		
				S1-Port						
				8b MMC	SD+UART	SD+SPI	SD+GPIO	GPIO	GPIO+UART +I2S	SD+I2S	UART+SPI +I2S
F5	VIO3	I/O	GPIO[46]	S1_SD0	S1_SD0	S1_SD0	S1_SD0	GPIO	GPIO	S1_SD0	UART_RTS
E1	VIO3	I/O	GPIO[47]	S1_SD1	S1_SD1	S1_SD1	S1_SD1	GPIO	GPIO	S1_SD1	UART_CTS
E5	VIO3	I/O	GPIO[48]	S1_SD2	S1_SD2	S1_SD2	S1_SD2	GPIO	GPIO	S1_SD2	UART_TX
E4	VIO3	I/O	GPIO[49]	S1_SD3	S1_SD3	S1_SD3	S1_SD3	GPIO	GPIO	S1_SD3	UART_RX
D1	VIO3	I/O	GPIO[50]	S1_CMD	S1_CMD	S1_CMD	S1_CMD	GPIO	I2S_CLK	S1_CMD	I2S_CLK
D2	VIO3	I/O	GPIO[51]	S1_CLK	S1_CLK	S1_CLK	S1_CLK	GPIO	I2S_SD	S1_CLK	I2S_SD
D3	VIO3	I/O	GPIO[52]	S1_WP	S1_WP	S1_WP	S1_WP	GPIO	I2S_WS	S1_WP	I2S_WS
D4	VIO4	I/O	GPIO[53]	S1_SD4	UART_RTS	SPI_SCK	GPIO	GPIO	UART_RTS	GPIO	SPI_SCK
C1	VIO4	I/O	GPIO[54]	S1_SD5	UART_CTS	SPI_SSN	GPIO	GPIO	UART_CTS	I2S_CLK	SPI_SSN
C2	VIO4	I/O	GPIO[55]	S1_SD6	UART_TX	SPI_MISO	GPIO	GPIO	UART_TX	I2S_SD	SPI_MISO
D5	VIO4	I/O	GPIO[56]	S1_SD7	UART_RX	SPI_MOSI	GPIO	GPIO	UART_RX	I2S_WS	SPI_MOSI
C4	VIO4	I/O	GPIO[57]	MMC1_RST_OUT	GPIO	GPIO	GPIO	GPIO	I2S_MCLK	I2S_MCLK	I2S_MCLK

FX3S Pin Description				
Pin	**Power Domain**	**I/O**	**Name**	**Power**
E10		PWR	VBATT	
B10		PWR	VDD	
A1		PWR	U3VSSQ	
E11		PWR	VBUS	
D8		PWR	VSS	
H11		PWR	VIO1	
E2		PWR	VSS	
L9		PWR	VIO1	
G1		PWR	VSS	
F1		PWR	VIO2	
G11		PWR	VSS	
E3		PWR	VIO3	
L1		PWR	VSS	
B1		PWR	VIO4	
L6		PWR	VSS	
B6		PWR	CVDDQ	
B5		PWR	U3TXVDDQ	
A2		PWR	U3RXVDDQ	
C11		PWR	VIO5	
L11		PWR	VSS	
A7		PWR	AVDD	
B7		PWR	AVSS	
C3		PWR	VDD	
B8		PWR	VSS	
E9		PWR	VDD	
B9		PWR	VSS	
F11		PWR	VDD	
H1		PWR	VDD	
L7		PWR	VDD	
J11		PWR	VDD	
L5		PWR	VDD	
K4		PWR	VSS	
L3		PWR	VSS	
K3		PWR	VSS	
L2		PWR	VSS	
A8		PWR	VSS	
				Precision Resistors
C8	VBUS/ VBATT	I/O	R_usb2	Precision resistor for USB 2.0 (Connect a 6.04 kΩ ±1% resistor between this pin and GND)
B3	U3TX VDDQ	I/O	R_usb3	Precision resistor for USB 3.0 (Connect a 200 Ω ±1% resistor between this pin and GND)

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power supplied (Industrial) ..... –40 °C to +85 °C

Supply voltage to ground potential

V_{DD}, A_{VDDQ} ..... 1.25 V

V_{IO1},V_{IO2}, V_{IO3}, V_{IO4}, V_{IO5} ..... 3.6 V

$U3TX_{VDDQ}$, $U3RX_{VDDQ}$ ..... 1.25 V

DC input voltage to any input pin ..... V_{CC} + 0.3

DC voltage applied to outputs in high Z state ..... V_{CC} + 0.3

(VCC is the corresponding I/O voltage)

Static discharge voltage ESD protection levels:

- ± 2.2-KV HBM based on JESD22-A114
- Additional ESD protection levels on D+, D–, and GND pins, and serial peripheral pins
- ± 6-KV contact discharge, ± 8-KV air gap discharge based on IEC61000-4-2 level 3A, ± 8-KV contact discharge, and ± 15-KV air gap discharge based on IEC61000-4-2 level 4C

Latch-up current ..... > 200 mA

Maximum output short-circuit current for all I/O configurations. (Vout = 0 V) ..... –100 mA

Operating Conditions

T_A (ambient temperature under bias)

Industrial ..... –40 °C to +85 °C

V_{DD}, A_{VDDQ}, $U3TX_{VDDQ}$, $U3RX_{VDDQ}$

Supply voltage ..... 1.15 V to 1.25 V

V_{BATT} supply voltage ..... 3.2 V to 6 V

V_{IO1}, V_{IO2}, V_{IO3}, V_{IO4}, C_{VDDQ}

Supply voltage ..... 1.7 V to 3.6 V

V_{IO5} supply voltage ..... 1.15 V to 3.6 V

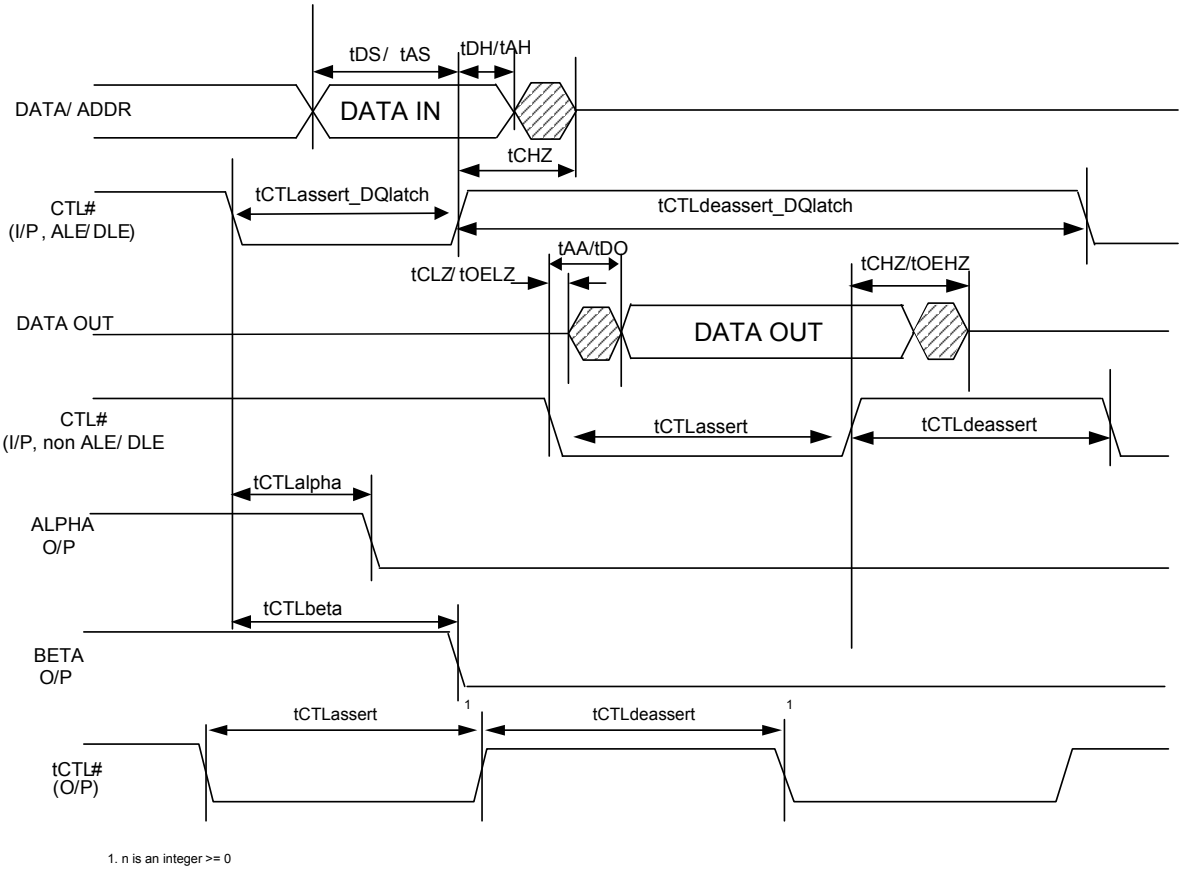
DC Specifications

Parameter	Description	Min	Max	Units	Notes
V_{DD}	Core voltage supply	1.15	1.25	V	1.2-V typical
A_{VDD}	Analog voltage supply	1.15	1.25	V	1.2-V typical
V_{IO1}	GPIF II I/O power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO2}	S0-Port power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO3}	S1-Port power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO4}	S1-Port and UART/SPI/I2S power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{BATT}	USB voltage supply	3.2	6	V	3.7-V typical
V_{BUS}	USB voltage supply	4.0	6	V	5-V typical
$U3TX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply.
$U3RX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply.
C_{VDDQ}	Clock voltage supply	1.7	3.6	V	1.8-, 3.3-V typical
V_{IO5}	I^2C and JTAG voltage supply	1.15	3.6	V	1.2-, 1.8-, 2.5-, and 3.3-V typical
V_{IH1}	Input HIGH voltage 1	0.625 × V_{CC}	V_{CC} + 0.3	V	For 2.0 V ≤ V_{CC} ≤ 3.6 V (except USB port).V_{CC} is the corresponding I/O voltage supply.
V_{IH2}	Input HIGH voltage 2	V_{CC} – 0.4	V_{CC} + 0.3	V	For 1.7 V ≤ V_{CC} ≤ 2.0 V (except USB port).V_{CC} is the corresponding I/O voltage supply.

DC Specifications (continued)

Parameter	Description	Min	Max	Units	Notes
V_{IL}	Input LOW voltage	–0.3	0.25 × V_{CC}	V	V_{CC} is the corresponding I/O voltage supply.
V_{OH}	Output HIGH voltage	0.9 × V_{CC}	–	V	I_{OH} (max) = –100 µA tested at quarter drive strength. V_{CC} is the corresponding I/O voltage supply.
V_{OL}	Output LOW voltage	–	0.1 × VCC	V	I_{OL} (min) = +100 µA tested at quarter drive strength. V_{CC} is the corresponding I/O voltage supply.
I_{IX}	Input leakage current for all pins except SSTXP/SSXM/SSRXP/SSRXM	–1	1	µA	All I/O signals held at V_{DDQ} (For I/Os with a pull-up or pull-down resistor connected, the leakage current increases by V_{DDQ}/R_{pu} or V_{DDQ}/R_{PD}
I_{OZ}	Output High-Z leakage current for all pins except SSTXP/ SSXM/ SSRXP/SSRXM	–1	1	µA	All I/O signals held at V_{DDQ}
I_{CC} Core	Core and analog voltage operating current	–	200	mA	Total current through A_{VDD}, V_{DD}
I_{CC} USB	USB voltage supply operating current	–	60	mA	
I_{SB1}	Total suspend current during suspend mode with USB 3.0 PHY enabled (L1)	–	–	mA	Core current: 1.5 mA I/O current: 20 µA USB current: 2 mA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB2}	Total suspend current during suspend mode with USB 3.0 PHY disabled (L2)	–	–	mA	Core current: 250 µA I/O current: 20 µA USB current: 1.2 mA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB3}	Total standby current during standby mode (L3)	–	–	µA	Core current: 60 µA I/O current: 20 µA USB current: 40 µA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB4}	Total standby current during core power-down mode (L4)	–	–	µA	Core current: 0 µA I/O current: 20 µA USB current: 40 µA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C.)
V_{RAMP}	Voltage ramp rate on core and I/O supplies	0.2	50	V/ms	Voltage ramp must be monotonic
V_N	Noise level permitted on V_{DD} and I/O supplies	–	100	mV	Max p-p noise level permitted on all supplies except A_{VDD}
V_{N_AVDD}	Noise level permitted on A_{VDD} supply	–	20	mV	Max p-p noise level permitted on A_{VDD}

Figure 13. GPIF II Timing in Asynchronous Mode



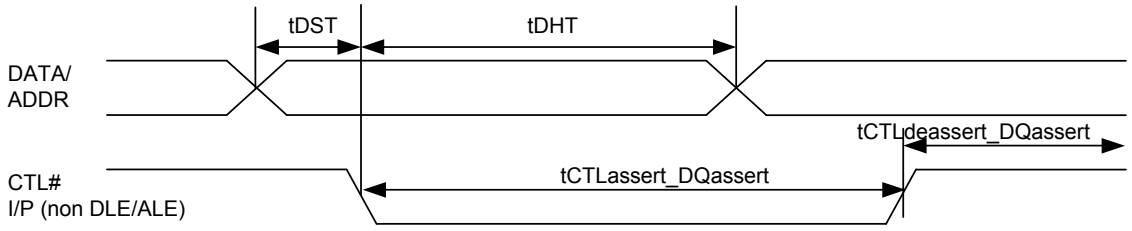
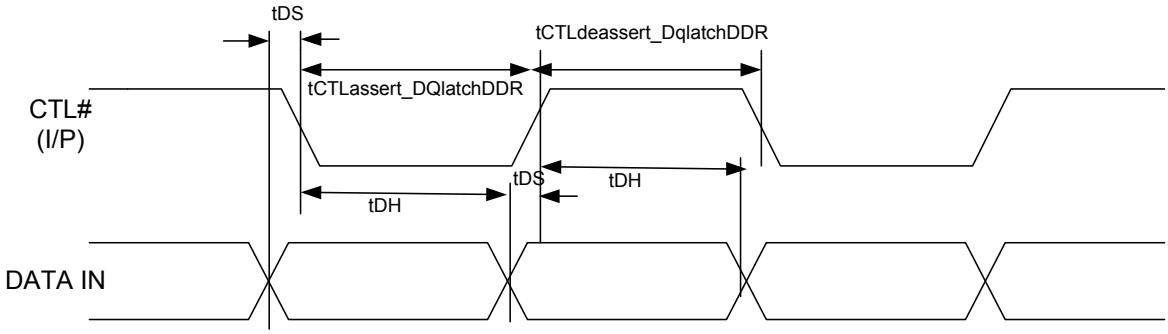


Figure 14. GPIF II Timing in Asynchronous DDR Mode



Asynchronous SRAM Timing

Figure 15. Non-multiplexed Asynchronous SRAM Read Timing

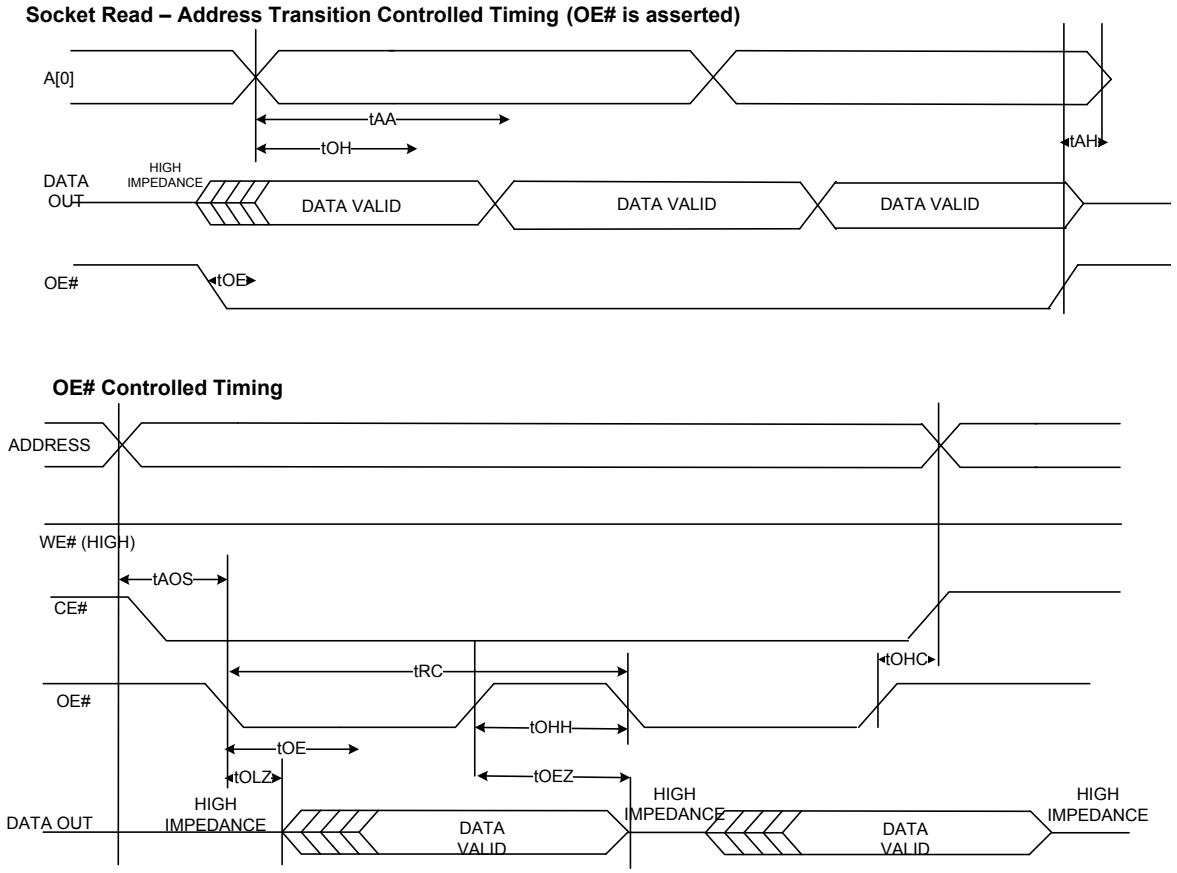
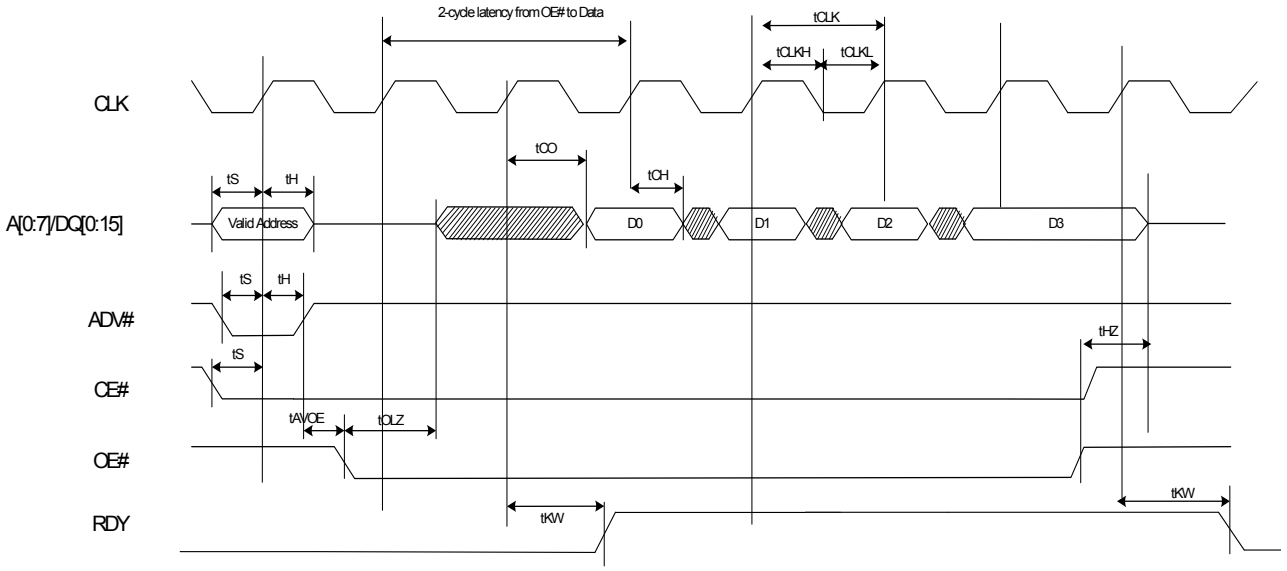


Table 9. Asynchronous SRAM Timing Parameters[5]

Parameter	Description	Min	Max	Units
–	SRAM interface bandwidth	–	61.5	MBps
tRC	Read cycle time	32.5	–	ns
tAA	Address to data valid	–	30	ns
tAOS	Address to OE# LOW setup time	7	–	ns
tOH	Data output hold from address change	3	–	ns
tOHH	OE# HIGH hold time	7.5	–	ns
tOHC	OE# HIGH to CE# HIGH	2	–	ns
tOE	OE# LOW to data valid	–	25	ns
tOLZ	OE# LOW to LOW-Z	0	–	ns
tWC	Write cycle time	30	–	ns
tCW	CE# LOW to write end	30	–	ns
tAW	Address valid to write end	30	–	ns
tAS	Address setup to write start	7	–	ns
tAH	Address hold time from CE# or WE#	2	–	ns
tWP	WE# pulse width	20	–	ns
tWPH	WE# HIGH time	10	–	ns
tCPH	CE# HIGH time	10	–	ns
tDS	Data setup to write end	7	–	ns
tDH	Data hold to write end	2	–	ns
tWHZ	Write to DQ HIGH-Z output	–	22.5	ns
tOEZ	OE# HIGH to DQ HIGH-Z output	–	22.5	ns
tOW	End of write to LOW-Z output	0	–	ns

Note
5. All parameters guaranteed by design and validated through characterization.

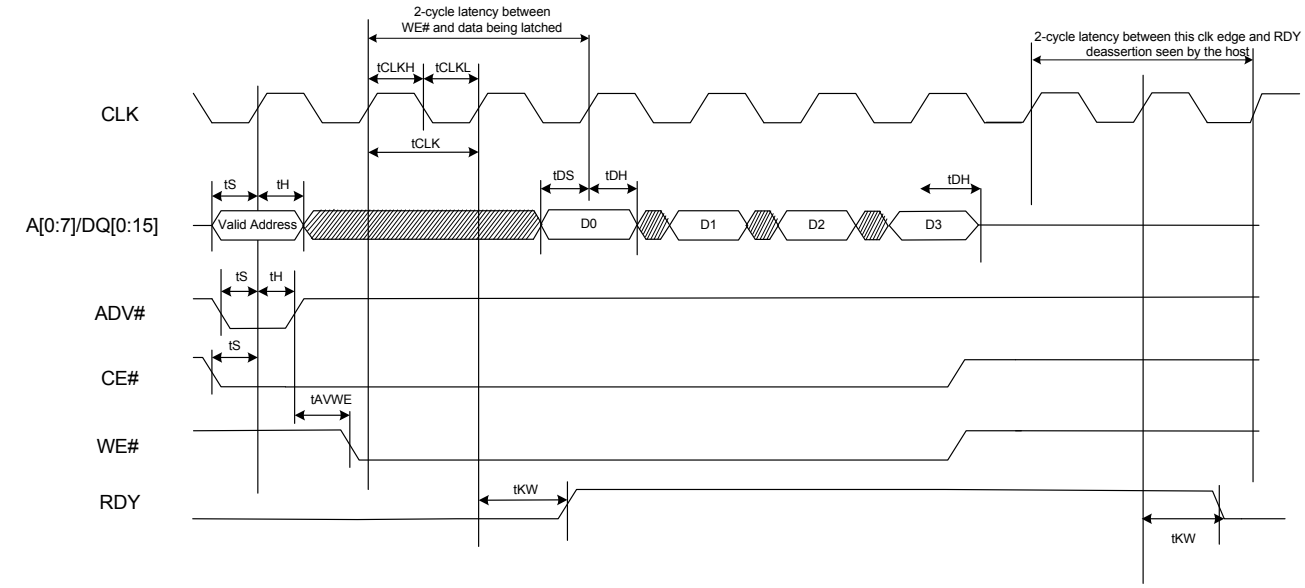
Figure 22. Synchronous ADMux Interface – Burst Read Timing



Note:

1) External P-Port processor and FX3S work operate on the same clock edge
2) External processor sees RDY assert 2 cycles after OE # asserts andand sees RDY deassert a cycle after the last burst data appears on the output
3) Valid output data appears 2 cycle after OE # asserted. The last burst data is held until OE # deasserts
4) Burst size of 4 is shown. Transfer size for the operation must be a multiple of burst size. Burst size is usually power of 2. RDY will not deassert in the middle of the burst.
5) External processor cannot deassert OE in the middle of a burst. If it does so, any bytes remaining in the burst packet could get lost.
6) Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

Figure 23. Sync ADMux Interface – Burst Write Timing



Note:

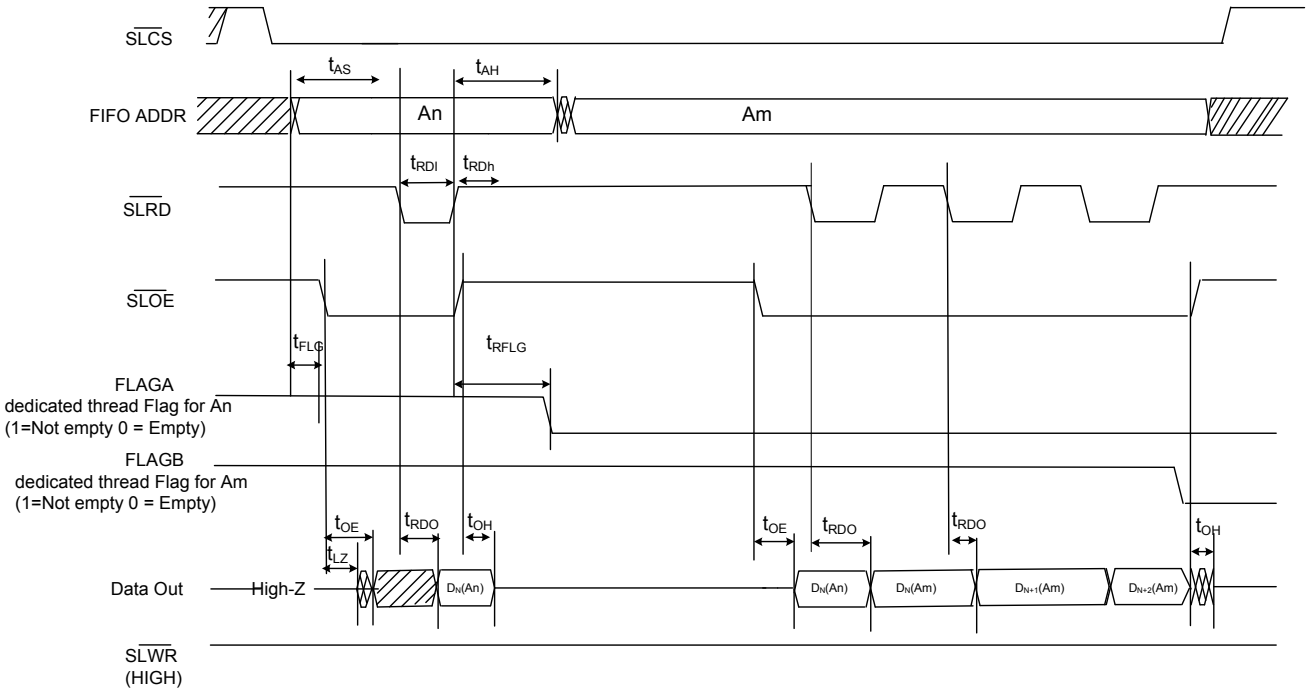
1) External P-Port processor and FX3S operate on the same clock edge
2) External processor sees RDY assert 2 cycles after WE # asserts and deasserts 3 cycles after the edge sampling the last burst data.
3) Transfer size for the operation must be a multiple of burst size. Burst size is usually power of 2. RDY will not deassert in the middle of the burst. Burst size of 4 is shown
4) External processor cannot deassert WE in the middle of a burst. If it does so, any bytes remaining in the burst packet could get lost.
5)Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

Table 11. Synchronous ADMux Timing Parameters[7]

Parameter	Description	Min	Max	Unit
FREQ	Interface clock frequency	–	100	MHz
tCLK	Clock period	10	–	ns
tCLKH	Clock HIGH time	4	–	ns
tCLKL	Clock LOW time	4	–	ns
tS	CE#/WE#/DQ setup time	2	–	ns
tH	CE#/WE#/DQ hold time	0.5	–	ns
tCH	Clock to data output hold time	0	–	ns
tDS	Data input setup time	2	–	ns
tDH	Clock to data input hold	0.5	–	ns
tAVDOE	ADV# HIGH to OE# LOW	0	–	ns
tAVDWE	ADV# HIGH to WE# LOW	0	–	ns
tHZ	CE# HIGH to Data HIGH-Z	–	8	ns
tOHZ	OE# HIGH to Data HIGH-Z	–	8	ns
tOLZ	OE# LOW to Data LOW-Z	0	–	ns
tKW	Clock to RDY valid	–	8	ns

Note
7. All parameters guaranteed by design and validated through characterization.

Figure 26. Asynchronous Slave FIFO Read Mode



Asynchronous Slave FIFO Write Sequence Description

- FIFO address is driven and SLCS# is asserted
- SLWR# is asserted. SLCS# must be asserted with SLWR# or before SLWR# is asserted
- Data must be present on the tWRS bus before the deasserting edge of SLWR#
- Deassertion of SLWR# causes the data to be written from the data bus to the FIFO, and then the FIFO pointer is incremented
- The FIFO flag is updated after the tWFLG from the deasserting edge of SLWR.

The same sequence of events is shown for a burst write.

Note that in the burst write mode, after SLWR# deassertion, the data is written to the FIFO, and then the FIFO pointer is incremented.

Short Packet: A short packet can be committed to the USB host by using the PKTEND#. The external device or processor should be designed to assert the PKTEND# along with the last word of data and SLWR# pulse corresponding to the last word. The FIFOADDR lines must be held constant during the PKTEND# assertion.

Zero-Length Packet: The external device or processor can signal a zero-length packet (ZLP) to FX3S simply by asserting PKTEND#, without asserting SLWR#. SLCS# and the address must be driven as shown in Figure 27 on page 39.

FLAG Usage: The FLAG signals are monitored by the external processor for flow control. FLAG signals are FX3S outputs that can be configured to show empty, full, and partial status for a dedicated address or the current address.

Table 13. Asynchronous Slave FIFO Parameters[9]

Parameter	Description	Min	Max	Units
tRDI	SLRD# low	20	–	ns
tRDh	SLRD# high	10	–	ns
tAS	Address to SLRD#/SLWR# setup time	7	–	ns
tAH	SLRD#/SLWR#/PKTEND to address hold time	2	–	ns
tRFLG	SLRD# to FLAGS output propagation delay	–	35	ns
tFLG	ADDR to FLAGS output propagation delay	–	22.5	
tRDO	SLRD# to data valid	–	25	ns
tOE	OE# low to data valid	–	25	ns
tLZ	OE# low to data low-Z	0	–	ns
tOH	SLOE# deassert data output hold	–	22.5	ns
tWRI	SLWR# low	20	–	ns
tWRh	SLWR# high	10	–	ns
tWRS	Data to SLWR# setup time	7	–	ns
tWRH	SLWR# to Data Hold time	2	–	ns
tWFLG	SLWR#/PKTEND to Flags output propagation delay	–	35	ns
tPEI	PKTEND low	20	–	ns
tPEh	PKTEND high	7.5	–	ns
tWRPE	SLWR# deassert to PKTEND deassert	2	–	ns

Note
9. All parameters guaranteed by design and validated through characterization.

Table 15. I²C Timing Parameters[11] (continued)

Parameter	Description	Min	Max	Units
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	50	–	ns
tr	Rise time of both SDA and SCL signals	–	120	ns
tf	Fall time of both SDA and SCL signals	–	120	ns
tSU:STO	Setup time for STOP condition	0.26	–	µs
tBUF	Bus-free time between a STOP and START condition	0.5	–	µs
tVD:DAT	Data valid time	–	0.45	µs
tVD:ACK	Data valid ACK	–	0.55	µs
tSP	Pulse width of spikes that must be suppressed by input filter	0	50	ns

I²S Timing Diagram

Figure 29. I²S Transmit Cycle

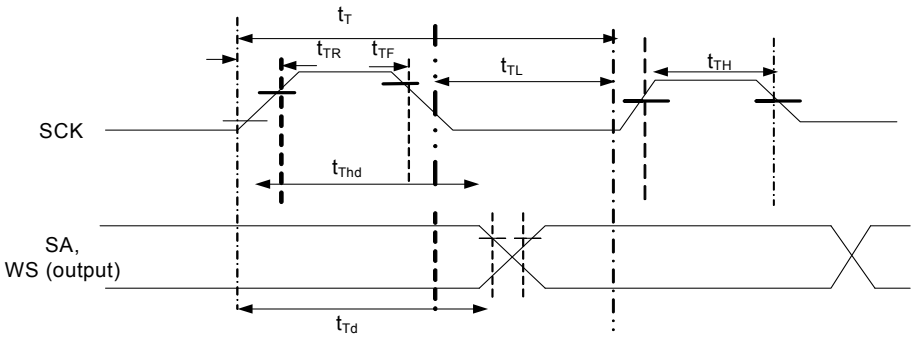


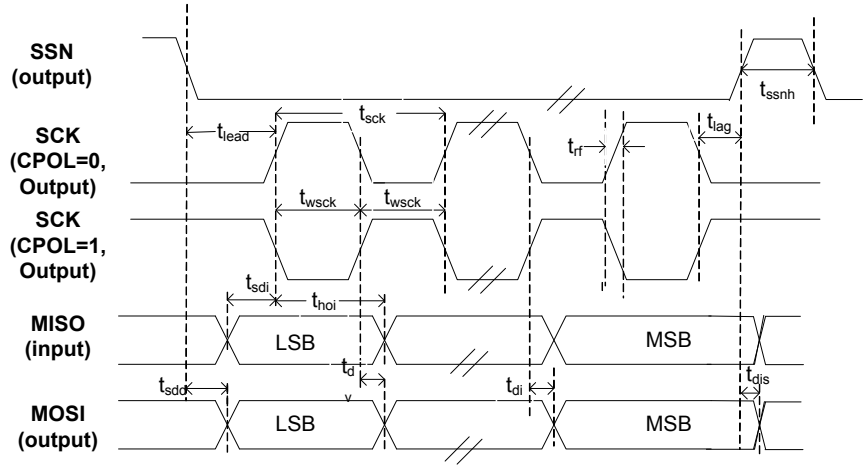
Table 16. I²S Timing Parameters[12]

Parameter	Description	Min	Max	Units
tT	I²S transmitter clock cycle	Ttr	–	ns
tTL	I²S transmitter cycle LOW period	0.35 Ttr	–	ns
tTH	I²S transmitter cycle HIGH period	0.35 Ttr	–	ns
tTR	I²S transmitter rise time	–	0.15 Ttr	ns
tTF	I²S transmitter fall time	–	0.15 Ttr	ns
tThd	I²S transmitter data hold time	0	–	ns
tTd	I²S transmitter delay time	–	0.8tT	ns
Note tT is selectable through clock gears. Max Ttr is designed for 96-kHz codec at 32 bits to be 326 ns (3.072 MHz).				

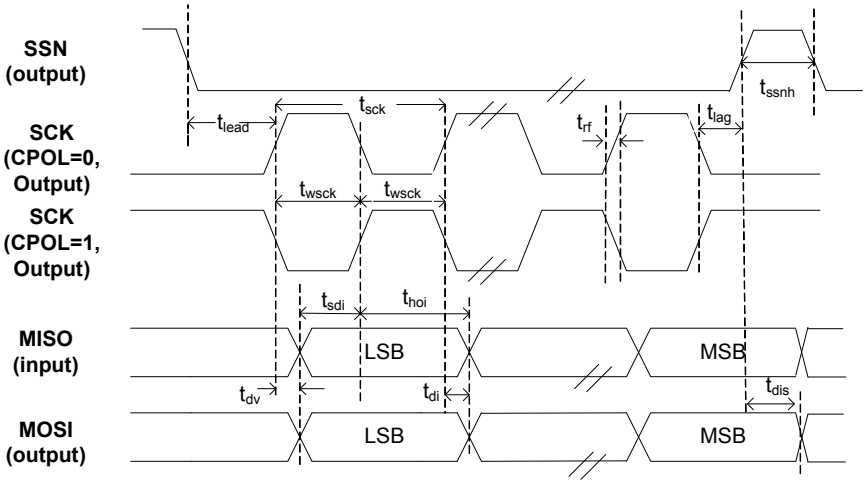
Note
12. All parameters guaranteed by design and validated through characterization.

SPI Timing Specification

Figure 30. SPI Timing



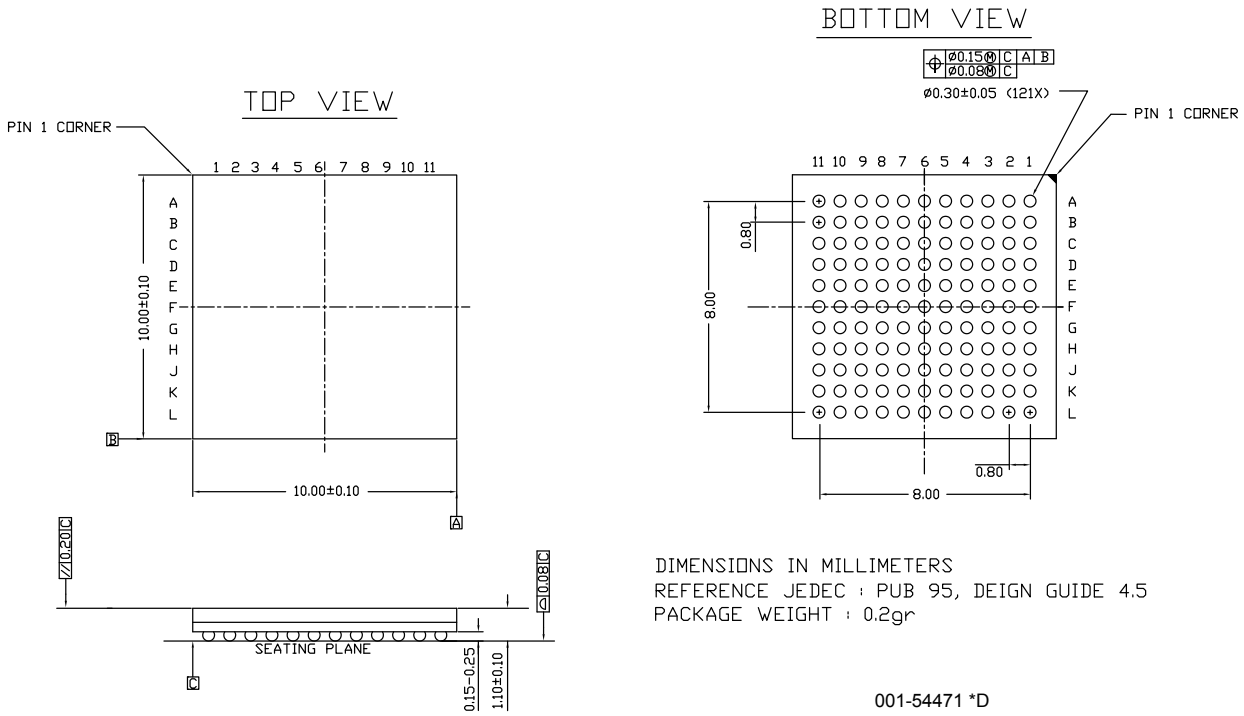
SPI Master Timing for CPHA = 0



SPI Master Timing for CPHA = 1

Package Diagram

Figure 32. 121-ball FBGA (10 × 10 × 1.2 mm (0.30 mm Ball Diameter)) Package Outline, 001-54471



Acronyms

Acronym	Description
DMA	Direct Memory Access
HNP	Host Negotiation Protocol
MMC	Multimedia Card
MTP	Media Transfer Protocol
PLL	Phase Locked Loop
PMIC	Power Management IC
SD	Secure Digital
SDIO	Secure Digital Input/Output
SLC	Single-Level Cell
SLCS	Slave Chip Select
SLOE	Slave Output Enable
SLRD	Slave Read
SLWR	Slave Write
SPI	Serial Peripheral Interface
SRP	Session Request Protocol
USB	Universal Serial Bus
WLCSP	Wafer Level Chip Scale Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Mbps	megabits per second
MBps	megabytes per second
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt

Document History Page

Document Title: CYUSB303X, EZ-USB® FX3S SuperSpeed USB Controller Document Number: 001-84160				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3786345	SAMT	12/06/2012	New data sheet.
*A	3900859	SAMT	02/11/2013	Updated Ordering Information (Updated part numbers).
*B	4027072	SAMT	06/20/2013	Updated Ordering Information (Updated part numbers). Updated in new template.
*C	4132176	GSZ	09/23/2013	Updated Features. Updated Applications. Updated Functional Overview. Updated Storage Port (S-Port). Replaced CYUSB3035 with CYUSB303X in all instances across the document.
*D	4616283	MDDD	01/07/2015	Added link to related resources on page 1. Added More Information section.
*E	4646195	RAJV	09/18/2015	Updated Slave FIFO Interface and Synchronous Slave FIFO Write Sequence Description. Updated Figure 24 and Figure 25. Updated Table 12.
*F	5085988	ANOP	01/14/2016	No technical updates. Completing Sunset Review.