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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78e054b40pl">https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78e054b40pl</a>

9.3.1	Clock Input Waveform .....	16
9.3.2	Program Fetch Cycle.....	16
9.3.3	Data Read Cycle .....	17
9.3.4	Data Write Cycle.....	17
9.3.5	Port Access Cycle .....	17
9.3.6	Program Operation .....	17
10.	TIMING WAVEFORMS .....	18
10.1	Program Fetch Cycle .....	18
10.2	Data Read Cycle.....	19
10.3	Data Write Cycle .....	19
10.4	Port Access Cycle.....	20
10.5	Program Operation .....	20
11.	TYPICAL APPLICATION CIRCUITS .....	21
11.1	Expanded External Program Memory and Crystal .....	21
11.2	Expanded External Data Memory and Oscillator .....	22
12.	PACKAGE DIMENSIONS .....	23
12.1	40-pin DIP .....	23
12.2	44-pin PLCC .....	23
12.3	44-pin PQFP .....	24
13.	REVISION HISTORY .....	25



## 1. GENERAL DESCRIPTION

The W78E54B is an 8-bit microcontroller which can accommodate a wider frequency range with low power consumption. The instruction set for the W78E54B is fully compatible with the standard 8051. The W78E54B contains an 16K bytes Flash EPROM; a 256 bytes RAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 4-bit I/O port P4; three 16-bit timer/counters; a hardware watchdog timer and a serial port. These peripherals are supported by eight sources two-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78E54B allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

The W78E54B microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

## 2. FEATURES

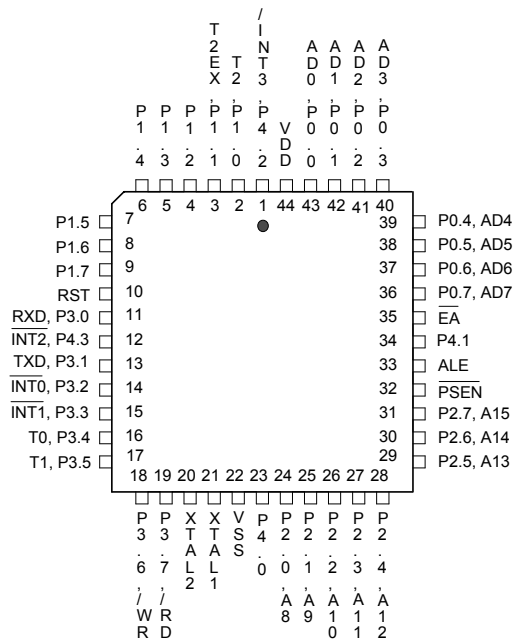
- Fully static design 8-bit CMOS microcontroller
- Wide supply voltage of 4.5V to 5.5V
- 256 bytes of on-chip scratchpad RAM
- 16 KB electrically erasable/programmable Flash EPROM
- 64 KB program memory address space
- 64 KB data memory address space
- Four 8-bit bi-directional ports
- One extra 4-bit bit-addressable I/O port, additional  $\overline{\text{INT2}}$  /  $\overline{\text{INT3}}$   
(available on 44-pin PLCC/QFP package)
- Three 16-bit timer/counters
- One full duplex serial port(UART)
- Watchdog Timer
- Eight sources, two-level interrupt capability
- EMI reduction mode
- Built-in power management
- Code protection mechanism
- Packages:
  - DIP 40: W78E54B-40
  - PLCC 44: W78E54BP-40
  - PQFP 44: W78E54BF-40
  - Lead Free (RoHS) DIP 40: W78E054B40DL
  - Lead Free (RoHS) PLCC 44: W78E054B40PL
  - Lead Free (RoHS) PQFP 44: W78E054B40FL

## 3. PIN CONFIGURATIONS

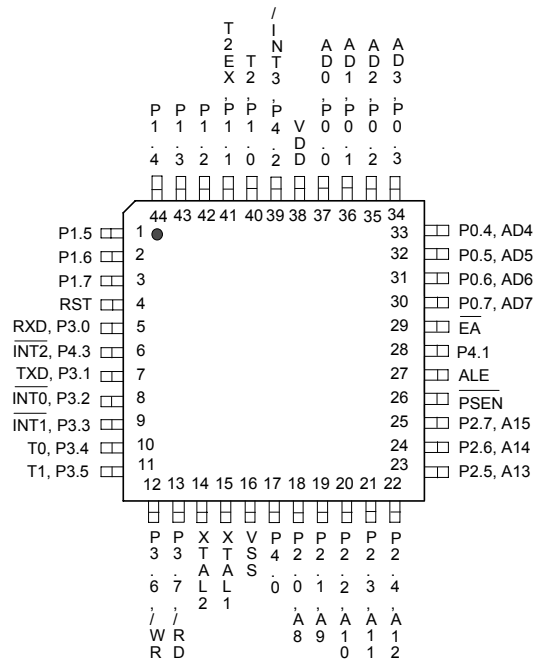
40-Pin DIP (W78E54B)

T2, P1.0	1	40	VDD
T2EX, P1.1	2	39	P0.0, AD0
P1.2	3	38	P0.1, AD1
P1.3	4	37	P0.2, AD2
P1.4	5	36	P0.3, AD3
P1.5	6	35	P0.4, AD4
P1.6	7	34	P0.5, AD5
P1.7	8	33	P0.6, AD6
RST	9	32	P0.7, AD7
RXD, P3.0	10	31	$\overline{EA}$
TXD, P3.1	11	30	ALE
$\overline{INT0}$ , P3.2	12	29	$\overline{PSEN}$
$\overline{INT1}$ , P3.3	13	28	P2.7, A15
T0, P3.4	14	27	P2.6, A14
T1, P3.5	15	26	P2.5, A13
$\overline{WR}$ , P3.6	16	25	P2.4, A12
$\overline{RD}$ , P3.7	17	24	P2.3, A11
XTAL2	18	23	P2.2, A10
XTAL1	19	22	P2.1, A9
VSS	20	21	P2.0, A8

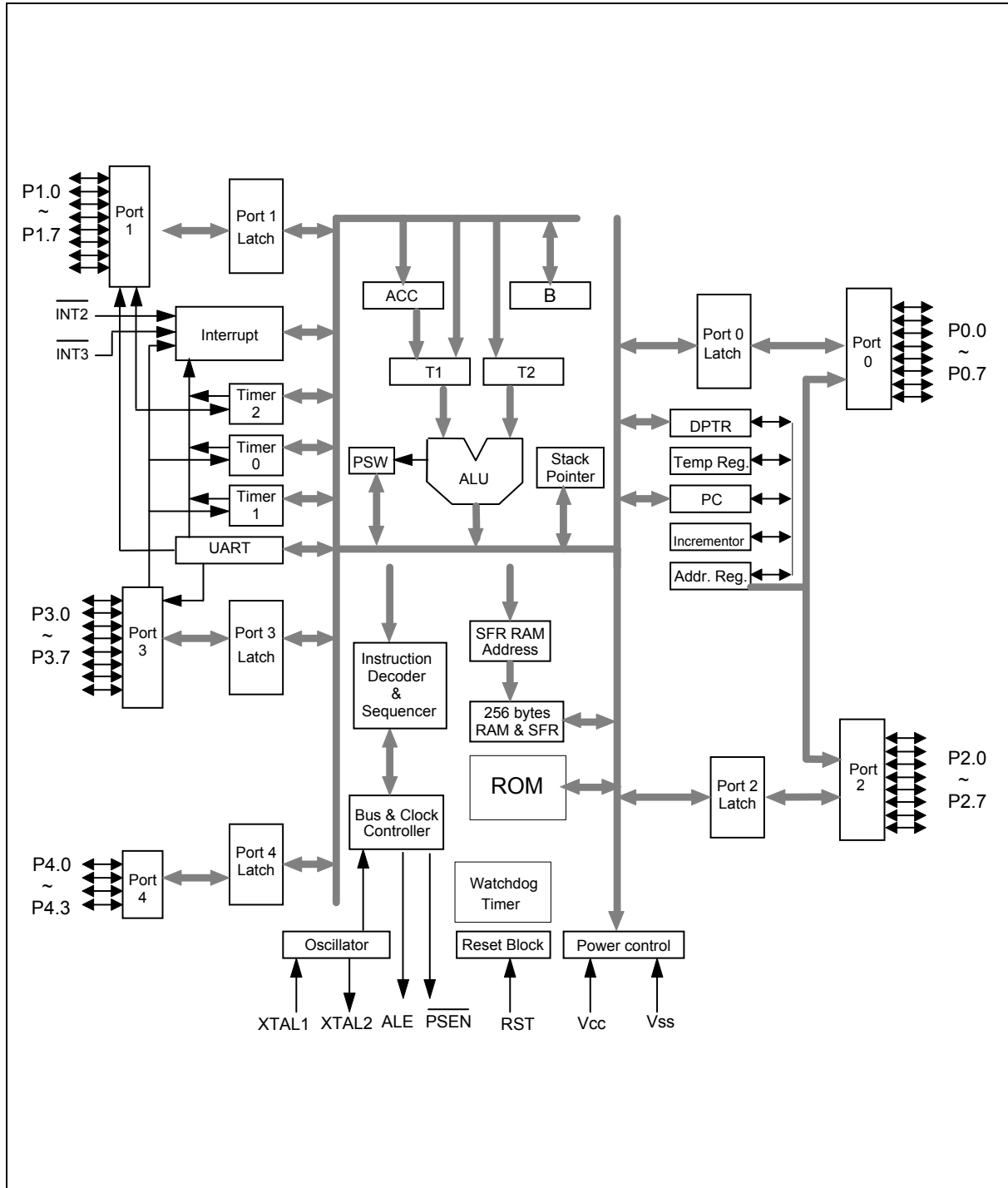
44-Pin PLCC (W78E54BP)



44-Pin QFP (W78E54BF)



## 5. BLOCK DIAGRAM





## 6. FUNCTIONAL DESCRIPTION

The W78E54B architecture consists of a core controller surrounded by various registers, five general purpose I/O ports, 256 bytes of RAM, three timer/counters, and a serial port. The processor supports 111 different opcodes and references both a 64K program address space and a 64K data storage space.

### 6.1 Timers 0, 1, and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0 and 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2.

The operations of Timer 0 and Timer 1 are the same as in the W78C51. Timer 2 is a special feature of the W78E54B: it is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

### 6.2 New Defined Peripheral

In order to be more suitable for I/O, an extra 4-bit bit-addressable port P4 and two external interrupt  $\overline{\text{INT2}}$ ,  $\overline{\text{INT3}}$  has been added to either the PLCC or QFP 44-pin package. And description follows:

#### 6.2.1 $\overline{\text{INT2}}$ / $\overline{\text{INT3}}$

Two additional external interrupts,  $\overline{\text{INT2}}$  and  $\overline{\text{INT3}}$ , whose functions are similar to those of external interrupt 0 and 1 in the standard 80C52. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 80C52. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB (/CLR) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON.

#### XICON - external interrupt control (C0H)

PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2
-----	-----	-----	-----	-----	-----	-----	-----

PX3: External interrupt 3 priority high if set

EX3: External interrupt 3 enable if set

IE3: If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced

IT3: External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software

PX2: External interrupt 2 priority high if set

EX2: External interrupt 2 enable if set

IE2: If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced

IT2: External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software



## \*\*\*AUXR - Auxiliary register (8EH)

-	-	-	-	-	-	-	AO
---	---	---	---	---	---	---	----

AO: Turn off ALE output.

## 6.3 Power-off Flag

### \*\*\*PCON - Power control (87H)

-	-	-	POF	GF1	GF0	PD	IDL
---	---	---	-----	-----	-----	----	-----

POF: Power off flag. Bit is set by hardware when power on reset. It can be cleared by software to determine chip reset is a warm boot or cold boot.

GF1, GF0: These two bits are general-purpose flag bits for the user.

PD: Power down mode bit. Set it to enter power down mode.

IDL: Idle mode bit. Set it to enter idle mode.

The power-off flag is located at PCON.4. This bit is set when VDD has been applied to the part. It can be used to determine if a reset is a warm boot or a cold boot if it is subsequently reset by software.

## 6.4 Watchdog Timer

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs, a system reset can also be caused if it is enabled. The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed. The Watchdog timer will be disabled on reset. In general, software should restart the Watchdog timer to put it into a known state. The control bits that support the Watchdog timer are discussed below.

### Watchdog Timer Control Register

Bit:	7	6	5	4	3	2	1	0
	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0

Mnemonic: WDTC

Address: 8FH

ENW : Enable watch-dog if set.

CLRW : Clear watch-dog timer and prescaler if set. This flag will be cleared automatically

WIDL : If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.

PS2, PS1, PS0: Watch-dog prescaler timer select. Prescaler is selected when set PS2~0 as follows:



## 6.5 Clock

The W78E54B is designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used. This makes the W78E54B relatively insensitive to duty cycle variations in the clock. The W78E54B incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground. An external clock source should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator.

## 6.6 Power Management

### Idle Mode

The idle mode is entered by setting the IDL bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

### Power-down Mode

When the PD bit of the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator. The only way to exit power-down mode is by a reset.

## 6.7 Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the W78E54B is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

## 7. ON-CHIP FLASH EPROM CHARACTERISTICS

The W78E54B has several modes to program the on-chip Flash EPROM. All these operations are configured by the pins RST, ALE, PSEN, A9CTRL(P3.0), A13CTRL(P3.1), A14CTRL(P3.2), OECTRL(P3.3), CE (P3.6), OE (P3.7), A0(P1.0) and VPP( $\overline{\text{EA}}$ ). Moreover, the A15–A0(P2.7–P2.0, P1.7–P1.0) and the D7–D0(P0.7–P0.0) serve as the address and data bus respectively for these operations.

### 7.1 Read Operation

This operation is supported for customer to read their code and the Security bits. The data will not be valid if the Lock bit is programmed to low.

### 7.2 Output Disable Condition

When the  $\overline{\text{OE}}$  is set to high, no data output appears on the D7..D0.

### 7.3 Program Operation





This operation is used to program the data to Flash EPROM and the security bits. Program operation is done when the Vpp is reach to Vcp (12.5V) level,  $\overline{CE}$  set to low, and  $\overline{OE}$  set to high.

## 7.4 Program Verify Operation

All the programming data must be checked after program operations. This operation should be performed after each byte is programmed; it will ensure a substantial program margin.

## 7.5 Erase Operation

An erase operation is the only way to change data from 0 to 1. This operation will erase all the Flash EPROM cells and the security bits from 0 to 1. This erase operation is done when the Vpp is reach to Vep level,  $\overline{CE}$  set to low, and  $\overline{OE}$  set to high.

## 7.6 Erase Verify Operation

After an erase operation, all of the bytes in the chip must be verified to check whether they have been successfully erased to 1 or not. The erase verify operation automatically ensures a substantial erase margin. This operation will be done after the erase operation if Vpp = Vep (14.5V),  $\overline{CE}$  is high and  $\overline{OE}$  is low.

## 7.7 Program/Erase Inhibit Operation

This operation allows parallel erasing or programming of multiple chips with different data. When P3.6( $\overline{CE}$ ) = VIH, P3.7( $\overline{OE}$ ) = VIH, erasing or programming of non-targeted chips is inhibited. So, except for the P3.6 and P3.7 pins, the individual chips may have common inputs.

OPERATIONS	P3.0 (A9 CTRL)	P3.1 (A13 CTRL)	P3.2 (A14 CTRL)	P3.3 (OE CTRL)	P3.6 ( $\overline{CE}$ )	P3.7 ( $\overline{OE}$ )	EA (VPP)	P2, P1 (A15..A0)	P0 (D7..D0)	NOTE
Read	0	0	0	0	0	0	1	Address	Data Out	
Output Disable	0	0	0	0	0	1	1	X	Hi-Z	
Program	0	0	0	0	0	1	VCP	Address	Data In	
Program Verify	0	0	0	0	1	0	VCP	Address	Data Out	@3
Erase	1	0	0	0	0	1	VEP	A0:0, others: X	Data In 0FFH	@4
Erase Verify	1	0	0	0	1	0	VEP	Address	Data Out	@5
Program/Erase Inhibit	X	0	0	0	1	1	VCP/ VEP	X	X	

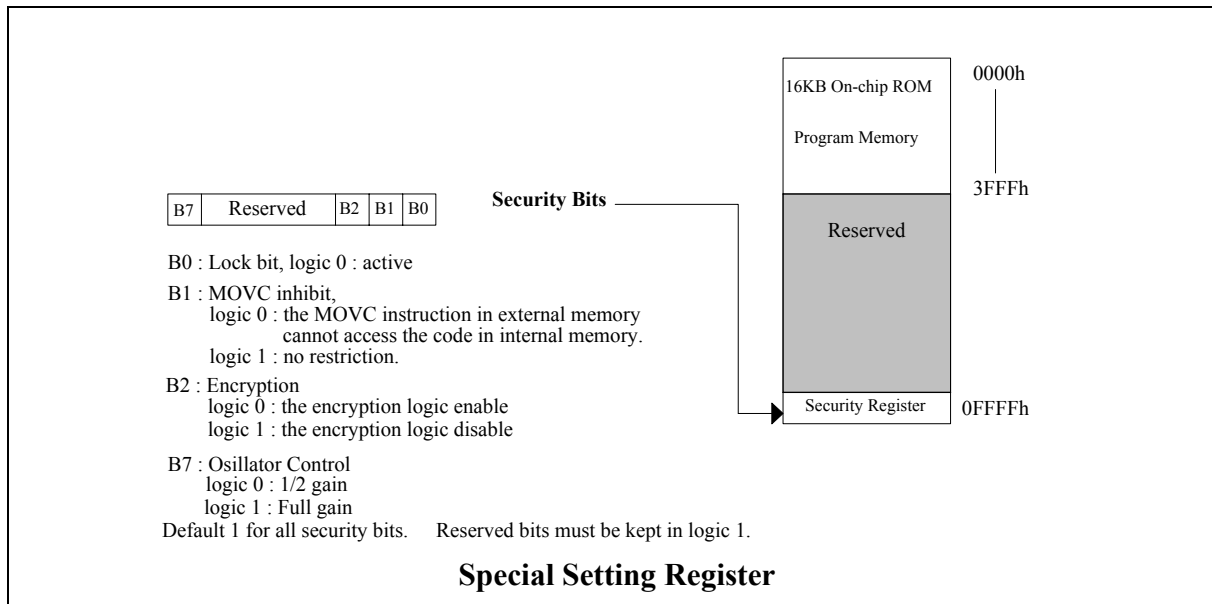
### Notes:

1. All these operations happen in RST = VIH, ALE = VIL and  $\overline{PSEN}$  = VIH.
2. VCP = 12.5V, VEP = 14.5V, VIH = VDD, VIL = Vss.
3. The program verify operation follows behind the program operation.
4. This erase operation will erase all the on-chip Flash EPROM cells and the Security bits.
5. The erase verify operation follows behind the erase operation.

## 8. SECURITY BITS

During the on-chip Flash EPROM operation mode, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of Flash EPROM and those operations on it are described below.

The W78E54B has a Security Register which can not be accessed in normal mode. These registers can only be accessed from the Flash EPROM operation mode. Those bits of the Security Register can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The Security Register is addressed in the Flash EPROM operation mode by address #0FFFFh.



### 8.1 Lock Bit

This bit is used to protect the customer's program code in the W78E54B. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and Special Setting Register can not be accessed again.

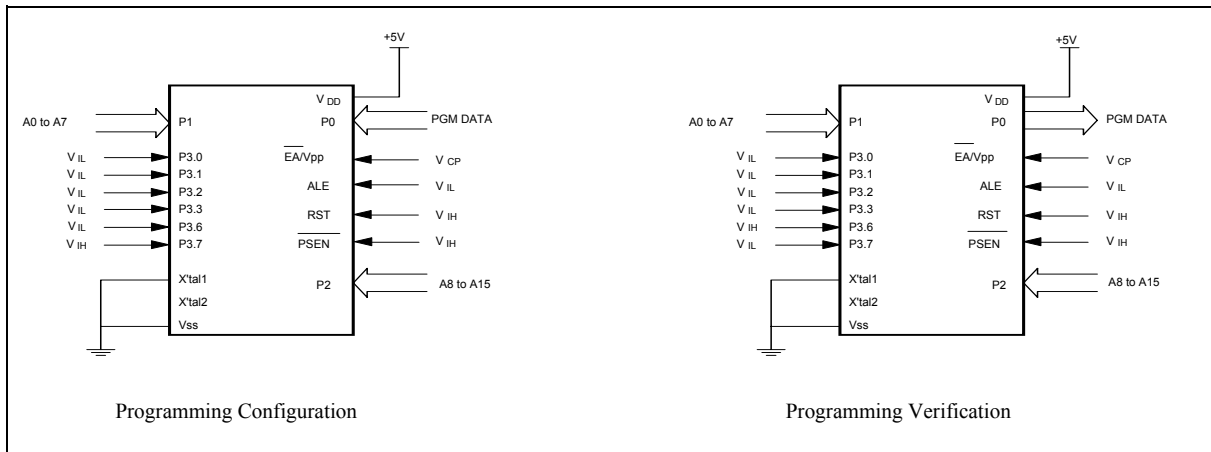
### 8.2 MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

### 8.3 Encryption

This bit is used to enable/disable the encryption logic for code protection. Once encryption feature is enabled, the data presented on port 0 will be encoded via encryption logic. Only whole chip erase will reset this bit.

# W78E54B/W78E054B



## 9. ELECTRICAL CHARACTERISTICS

### 9.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	V <sub>DD</sub> -V <sub>SS</sub>	-0.3	+7.0	V
Input Voltage	V <sub>IN</sub>	V <sub>SS</sub> -0.3	V <sub>DD</sub> +0.3	V
Operating Temperature	T <sub>A</sub>	0	70	°C
Storage Temperature	T <sub>ST</sub>	-55	+150	°C

**Note:** Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

### 9.2 D.C. Characteristics

(V<sub>CC</sub>-V<sub>SS</sub> = 5V ±10%, T<sub>A</sub> = 25° C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	PECIFICATION		UNIT
			MIN.	MAX.	
Operating Voltage	V <sub>DD</sub>	-	4.5	5.5	V
Operating Current	I <sub>DD</sub>	No load, V <sub>DD</sub> = 5.5V, RST = 1	-	20	mA
Idle Current	I <sub>IDLE</sub>	Idle mode V <sub>DD</sub> = 5.5V	-	6	mA
Power Down Current	I <sub>PWDN</sub>	Power-down mode V <sub>DD</sub> = 5.5V	-	50	μA
Input Current P1, P2, P3, P4	I <sub>IN1</sub>	V <sub>DD</sub> = 5.5V V <sub>IN</sub> = 0V or V <sub>DD</sub>	-50	+10	μA
Logical 1-to-0 Transition Current P1, P2, P3 <sup>(*1)</sup> , P4	I <sub>TL</sub>	V <sub>DD</sub> = 5.5V V <sub>IN</sub> = 2.0V <sup>(*1)</sup>	-550	-	μA

# W78E54B/W78E054B



DC Characteristics, continued

PARAMETER	SYMBOL	TEST CONDITIONS	SPECIFICATION		UNIT
			MIN.	MAX.	
Input Current RST <sup>(*2)</sup>	IIN2	VDD = 5.5V VIN = VDD	-10	+300	μA
Input Leakage Current P0, EA	ILK	VDD = 5.5V 0V < VIN < VDD	-10	+10	μA
Output Low Voltage P1, P2, P3, P4	VOL1	VDD = 4.5V IOL1 = +2 mA	-	0.45	V
Output Low Voltage ALE, PSEN, P0 <sup>(*3)</sup>	VOL2	VDD = 4.5V IOL2 = +4 mA	-	0.45	V
Output High Voltage P1, P2, P3, P4	VOH1	VDD = 4.5V IOH1 = -100 μA	2.4	-	V
Output High Voltage ALE, PSEN, P0 <sup>(*3)</sup>	VOH2	VDD = 4.5V IOH2 = -400 μA	2.4	-	V
Input Low Voltage (Except RST)	VIL1	VDD = 4.5V	0	0.8	V
Input Low Voltage RST <sup>(*4)</sup>	VIL2	VDD = 4.5V	0	0.8	V
Input Low Voltage XTAL1 <sup>(*4)</sup>	VIL3	VDD = 4.5V	0	0.8	V
Input High Voltage (Except RST)	VIH1	VDD = 4.5V	2.4	VDD +0.2	V
Sink Current P1, P2, P3, P4	ISK1	VDD = 4.5V Vs = 0.45V	4	12	mA
Input High Voltage RST <sup>(*4)</sup>	VIH2	VDD = 4.5V	0.67 VDD	VDD +0.2	V
Input High Voltage XTAL1 <sup>(*4)</sup>	VIH3	VDD = 4.5V	0.67 VDD	VDD +0.2	V
Sink Current P0, ALE, PSEN <sup>(*3)</sup>	ISK2	VDD = 4.5V Vs = 0.45V	8	16	mA
Source Current P1, P2, P3, P4	ISR1	VDD = 4.5V Vs = 2.4V	-100	-250	uA
Source Current P0, ALE, PSEN <sup>(*3)</sup>	ISR2	VDD = 4.5V Vs = 2.4V	-8	-14	mA

**Notes:**

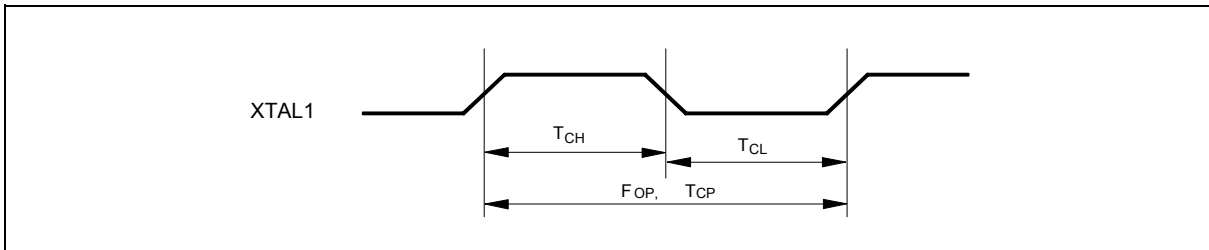
- \*1. Pins P1, P2 and P3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when VIN is approximately 2V.
- \*2. RST pin has an internal pull-down resistor.
- \*3. P0, ALE, PSEN are in the external access memory mode.
- \*4. XTAL1 is a CMOS input and RST is a Schmitt trigger input.



### 9.3 A.C. Characteristics

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a  $\pm 20$  nS variation. The numbers below represent the performance expected from a 0.6micron CMOS process when using 2 and 4 mA output buffers.

#### 9.3.1 Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	FOP	0	-	40	MHz	1
Clock Period	TCP	25	-	-	nS	2
Clock High	TCH	10	-	-	nS	3
Clock Low	TCL	10	-	-	nS	3

**Notes:**

1. The clock may be stopped indefinitely in either state.
2. The TCP specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

#### 9.3.2 Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	TAAS	1 TCP - $\Delta$	-	-	nS	4
Address Hold from ALE Low	TAAH	1 TCP - $\Delta$	-	-	nS	1, 4
ALE Low to $\overline{\text{PSEN}}$ Low	TAPL	1 TCP - $\Delta$	-	-	nS	4
$\overline{\text{PSEN}}$ Low to Data Valid	TPDA	-	-	2 TCP	nS	2
Data Hold after $\overline{\text{PSEN}}$ High	TPDH	0	-	1 TCP	nS	3
Data Float after $\overline{\text{PSEN}}$ High	TPDZ	0	-	1 TCP	nS	
ALE Pulse Width	TALW	2 TCP - $\Delta$	2 TCP	-	nS	4
$\overline{\text{PSEN}}$ Pulse Width	TPSW	3 TCP - $\Delta$	3 TCP	-	nS	4

**Notes:**

1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 TCP.
3. Data have been latched internally prior to  $\overline{\text{PSEN}}$  going high.
4. " $\Delta$ " (due to buffer driving delay and wire loading) is 20 nS.

### 9.3.3 Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{\text{RD}}$ Low	T <sub>DAR</sub>	3 T <sub>CP</sub> - $\Delta$	-	3 T <sub>CP</sub> + $\Delta$	nS	1, 2
$\overline{\text{RD}}$ Low to Data Valid	T <sub>DDA</sub>	-	-	4 T <sub>CP</sub>	nS	1
Data Hold from $\overline{\text{RD}}$ High	T <sub>DDH</sub>	0	-	2 T <sub>CP</sub>	nS	
Data Float from $\overline{\text{RD}}$ High	T <sub>DDZ</sub>	0	-	2 T <sub>CP</sub>	nS	
$\overline{\text{RD}}$ Pulse Width	T <sub>DRD</sub>	6 T <sub>CP</sub> - $\Delta$	6 T <sub>CP</sub>	-	nS	2

**Notes:**

1. Data memory access time is 8 T<sub>CP</sub>.
2. " $\Delta$ " (due to buffer driving delay and wire loading) is 20 nS.

### 9.3.4 Data Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{\text{WR}}$ Low	T <sub>DAW</sub>	3 T <sub>CP</sub> - $\Delta$	-	3 T <sub>CP</sub> + $\Delta$	nS
Data Valid to $\overline{\text{WR}}$ Low	T <sub>DAD</sub>	1 T <sub>CP</sub> - $\Delta$	-	-	nS
Data Hold from $\overline{\text{WR}}$ High	T <sub>DWD</sub>	1 T <sub>CP</sub> - $\Delta$	-	-	nS
$\overline{\text{WR}}$ Pulse Width	T <sub>DWR</sub>	6 T <sub>CP</sub> - $\Delta$	6 T <sub>CP</sub>	-	nS

**Note:** " $\Delta$ " (due to buffer driving delay and wire loading) is 20 nS.

### 9.3.5 Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	T <sub>PDS</sub>	1 T <sub>CP</sub>	-	-	nS
Port Input Hold from ALE Low	T <sub>PDH</sub>	0	-	-	nS
Port Output to ALE	T <sub>PDA</sub>	1 T <sub>CP</sub>	-	-	nS

**Note:** Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

### 9.3.6 Program Operation

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
VPP Setup Time	T <sub>VPS</sub>	2.0	-	-	$\mu\text{S}$
Data Setup Time	T <sub>DS</sub>	2.0	-	-	$\mu\text{S}$
Data Hold Time	T <sub>DH</sub>	2.0	-	-	$\mu\text{S}$
Address Setup Time	T <sub>AS</sub>	2.0	-	-	$\mu\text{S}$
Address Hold Time	T <sub>AH</sub>	0	-	-	$\mu\text{S}$

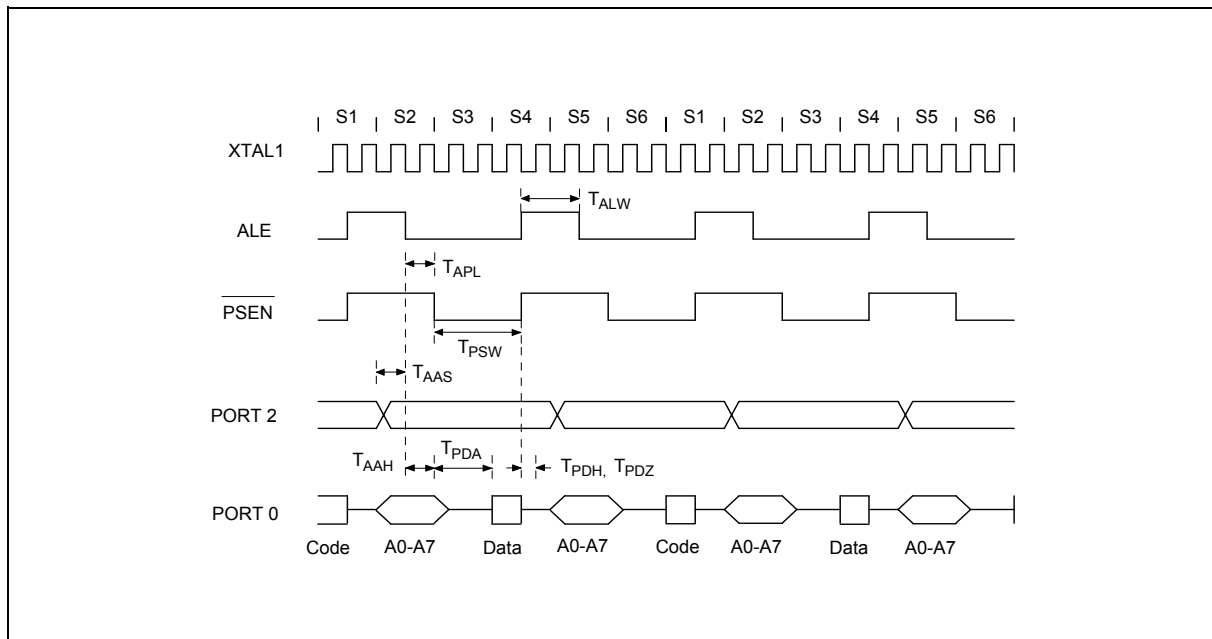
Program Operation, continued

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
$\overline{\text{CE}}$ Program Pulse Width for Program Operation	TPWP	290	300	310	$\mu\text{S}$
OCTRL Setup Time	TOCS	2.0	-	-	$\mu\text{S}$
OCTRL Hold Time	TOCH	2.0	-	-	$\mu\text{S}$
$\overline{\text{OE}}$ Setup Time	TOES	2.0	-	-	$\mu\text{S}$
$\overline{\text{OE}}$ High to Output Float	TDFP	0	-	130	nS
Data Valid from $\overline{\text{OE}}$	TOEV	-	-	150	nS

**Note:** Flash data can be accessed only in flash mode. The RST pin must pull in  $V_{\text{IH}}$  status, the ALE pin must pull in  $V_{\text{IL}}$  status, and the  $\overline{\text{PSEN}}$  pin must pull in  $V_{\text{IH}}$  status.

## 10. TIMING WAVEFORMS

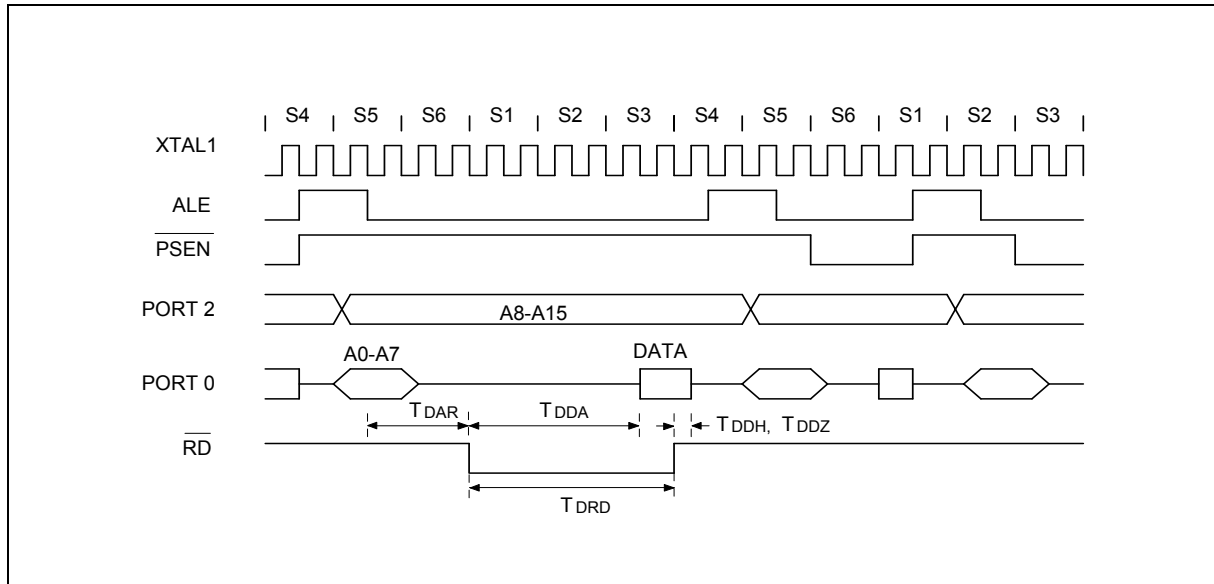
### 10.1 Program Fetch Cycle



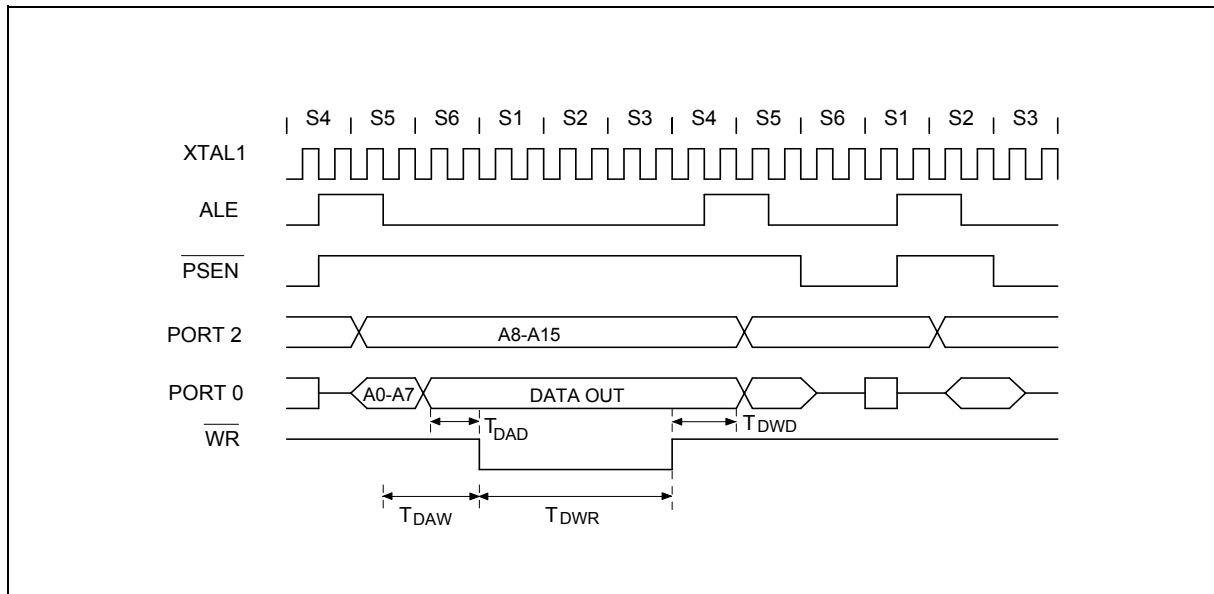


Timing Waveforms, continued

## 10.2 Data Read Cycle



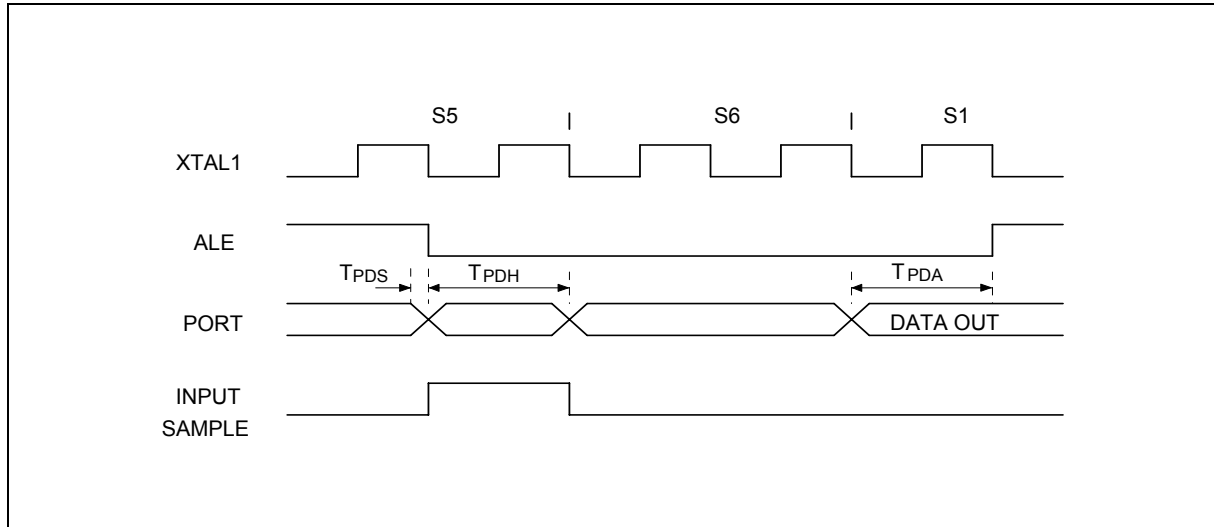
## 10.3 Data Write Cycle



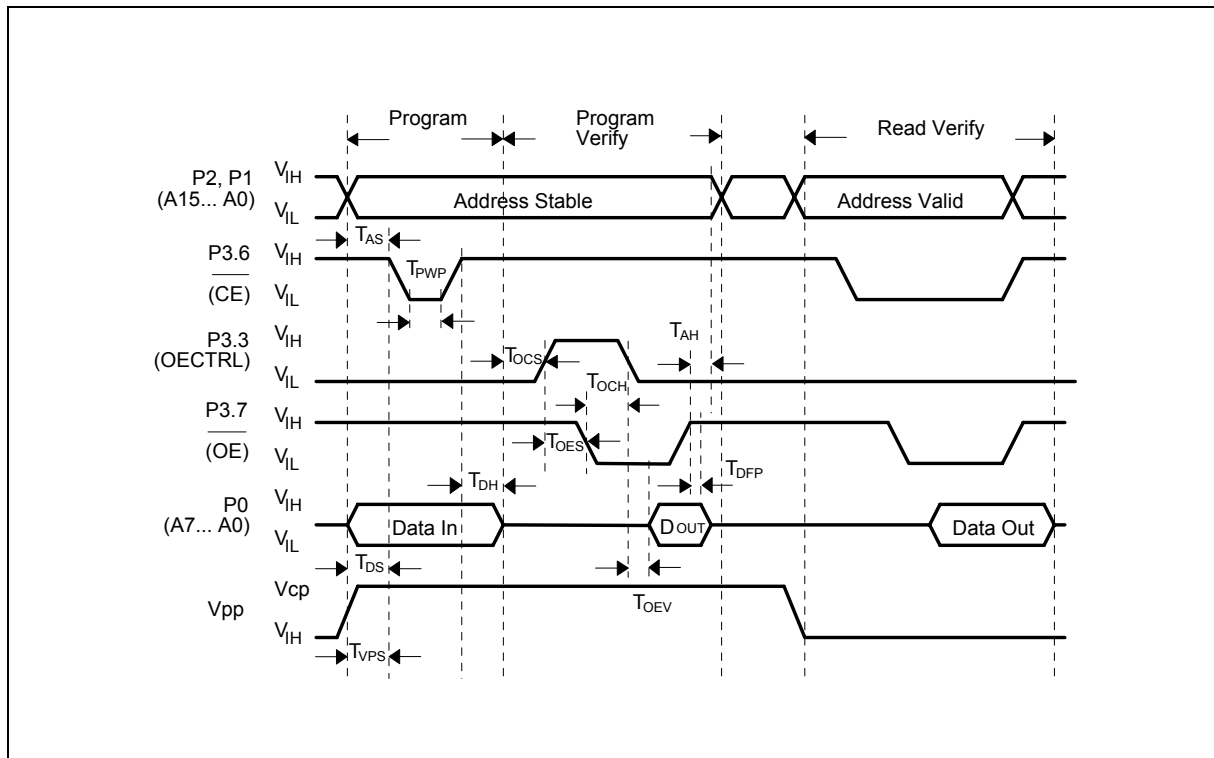


Timing Waveforms, continued

## 10.4 Port Access Cycle



## 10.5 Program Operation



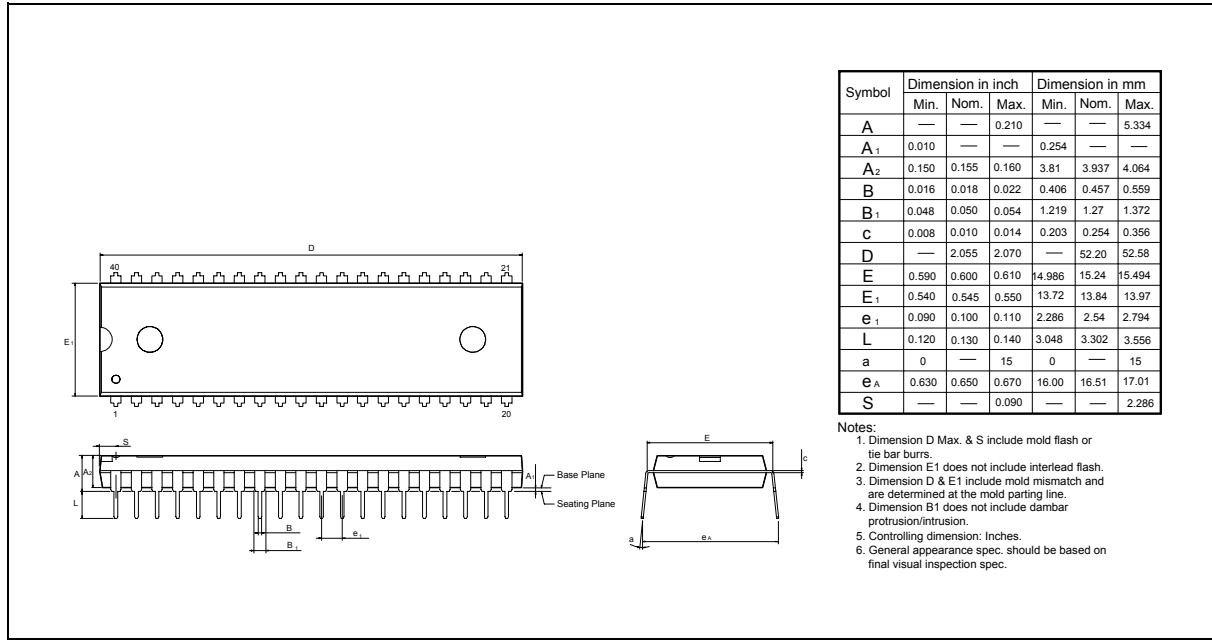


## 11.2 Expanded External Data Memory and Oscillator

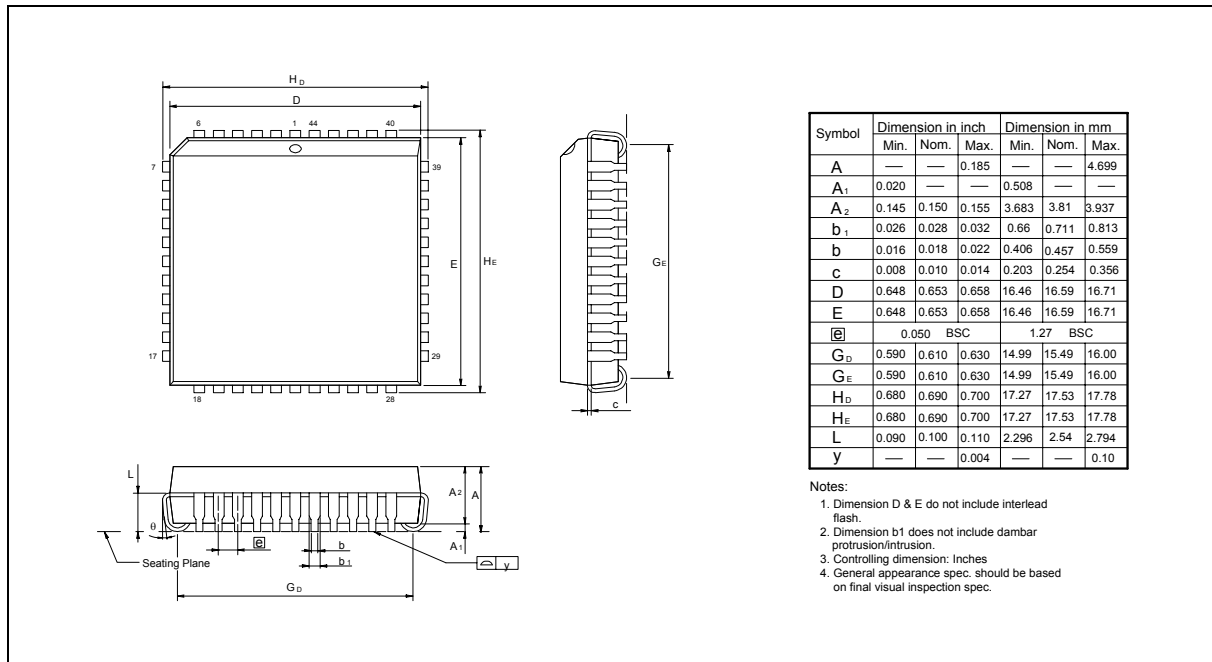


## 12. PACKAGE DIMENSIONS

### 12.1 40-pin DIP



### 12.2 44-pin PLCC



Package Dimensions, continued

## 12.3 44-pin PQFP

