What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

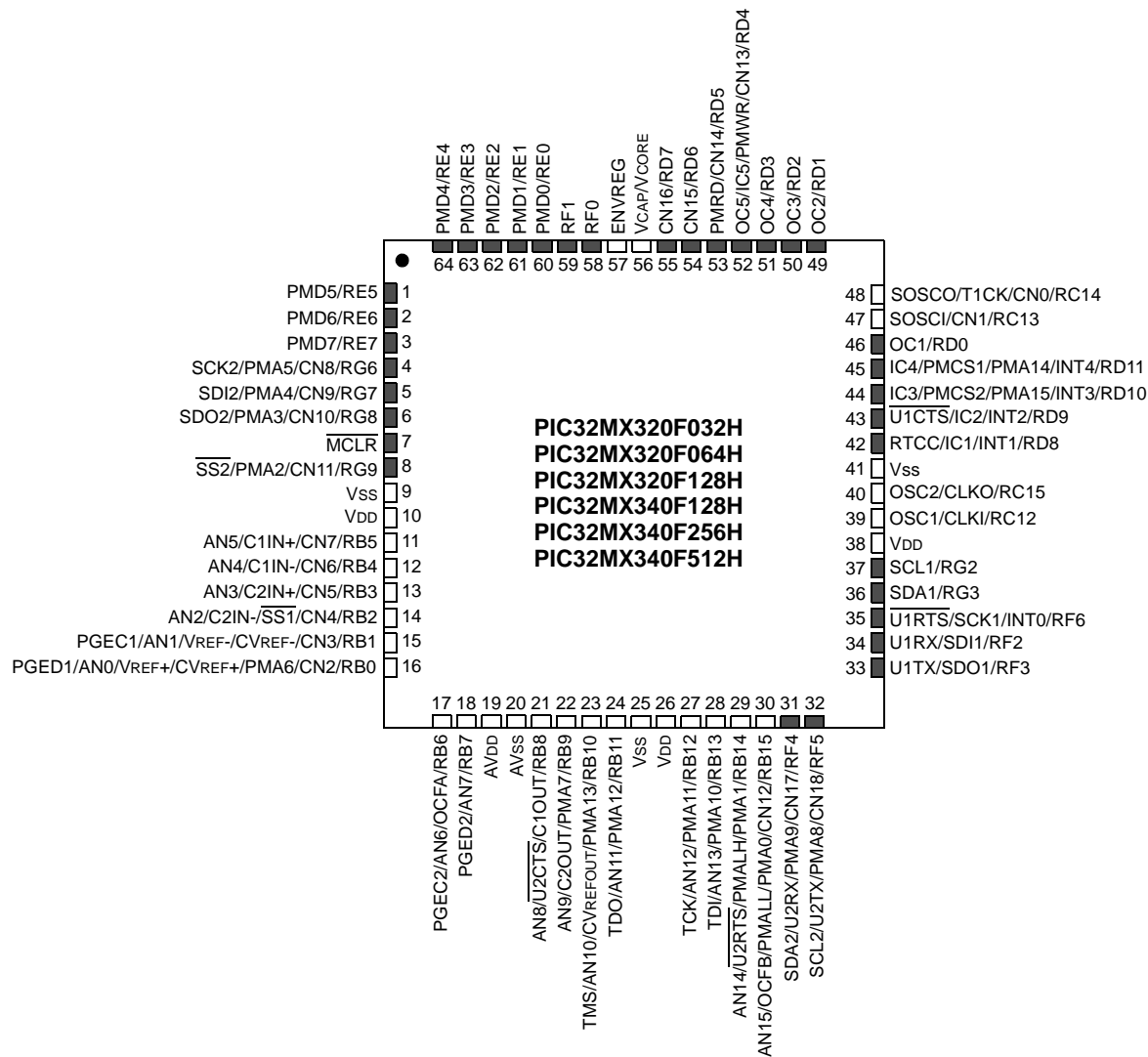## Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	53
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx320f032h-40i-mr

PIC32MX3XX/4XX

Pin Diagrams

64-Pin QFN (General Purpose)

■ = Pins are up to 5V tolerant

Top pins (64 → 49):
- 64 PMD4/RE4
- 63 PMD3/RE3
- 62 PMD2/RE2
- 61 PMD1/RE1
- 60 PMD0/RE0
- 59 RF1
- 58 RF0
- 57 ENVREG
- 56 VCAP/VCORE
- 55 CN16/RD7
- 54 CN15/RD6
- 53 PMRD/CN14/RD5
- 52 OC5/IC5/PMWR/CN13/RD4
- 51 OC4/RD3
- 50 OC3/RD2
- 49 OC2/RD1

Left pins (1 → 16):
- 1 PMD5/RE5
- 2 PMD6/RE6
- 3 PMD7/RE7
- 4 SCK2/PMA5/CN8/RG6
- 5 SDI2/PMA4/CN9/RG7
- 6 SDO2/PMA3/CN10/RG8
- 7 MCLR
- 8 SS2/PMA2/CN11/RG9
- 9 VSS
- 10 VDD
- 11 AN5/C1IN+/CN7/RB5
- 12 AN4/C1IN-/CN6/RB4
- 13 AN3/C2IN+/CN5/RB3
- 14 AN2/C2IN-/SS1/CN4/RB2
- 15 PGEC1/AN1/VREF-/CVREF-/CN3/RB1
- 16 PGED1/AN0/VREF+/CVREF+/PMA6/CN2/RB0

Device labels:
PIC32MX320F032H
PIC32MX320F064H
PIC32MX320F128H
PIC32MX340F128H
PIC32MX340F256H
PIC32MX340F512H

Right pins (48 → 33):
- 48 SOSCO/T1CK/CN0/RC14
- 47 SOSCI/CN1/RC13
- 46 OC1/RD0
- 45 IC4/PMCS1/PMA14/INT4/RD11
- 44 IC3/PMCS2/PMA15/INT3/RD10
- 43 U1CTS/IC2/INT2/RD9
- 42 RTCC/IC1/INT1/RD8
- 41 VSS
- 40 OSC2/CLKO/RC15
- 39 OSC1/CLKI/RC12
- 38 VDD
- 37 SCL1/RG2
- 36 SDA1/RG3
- 35 U1RTS/SCK1/INT0/RF6
- 34 U1RX/SDI1/RF2
- 33 U1TX/SDO1/RF3

Bottom pins (17 → 32):
- 17 PGEC2/AN6/OCFA/RB6
- 18 PGED2/AN7/RB7
- 19 AVDD
- 20 AVSS
- 21 AN8/U2CTS/C1OUT/RB8
- 22 AN9/C2OUT/PMA7/RB9
- 23 TMS/AN10/CVREFOUT/PMA13/RB10
- 24 TDO/AN11/PMA12/RB11
- 25 VSS
- 26 VDD
- 27 TCK/AN12/PMA11/RB12
- 28 TDI/AN13/PMA10/RB13
- 29 AN14/U2RTS/PMALH/PMA1/RB14
- 30 AN15/OCFB/PMALL/PMA0/CN12/RB15
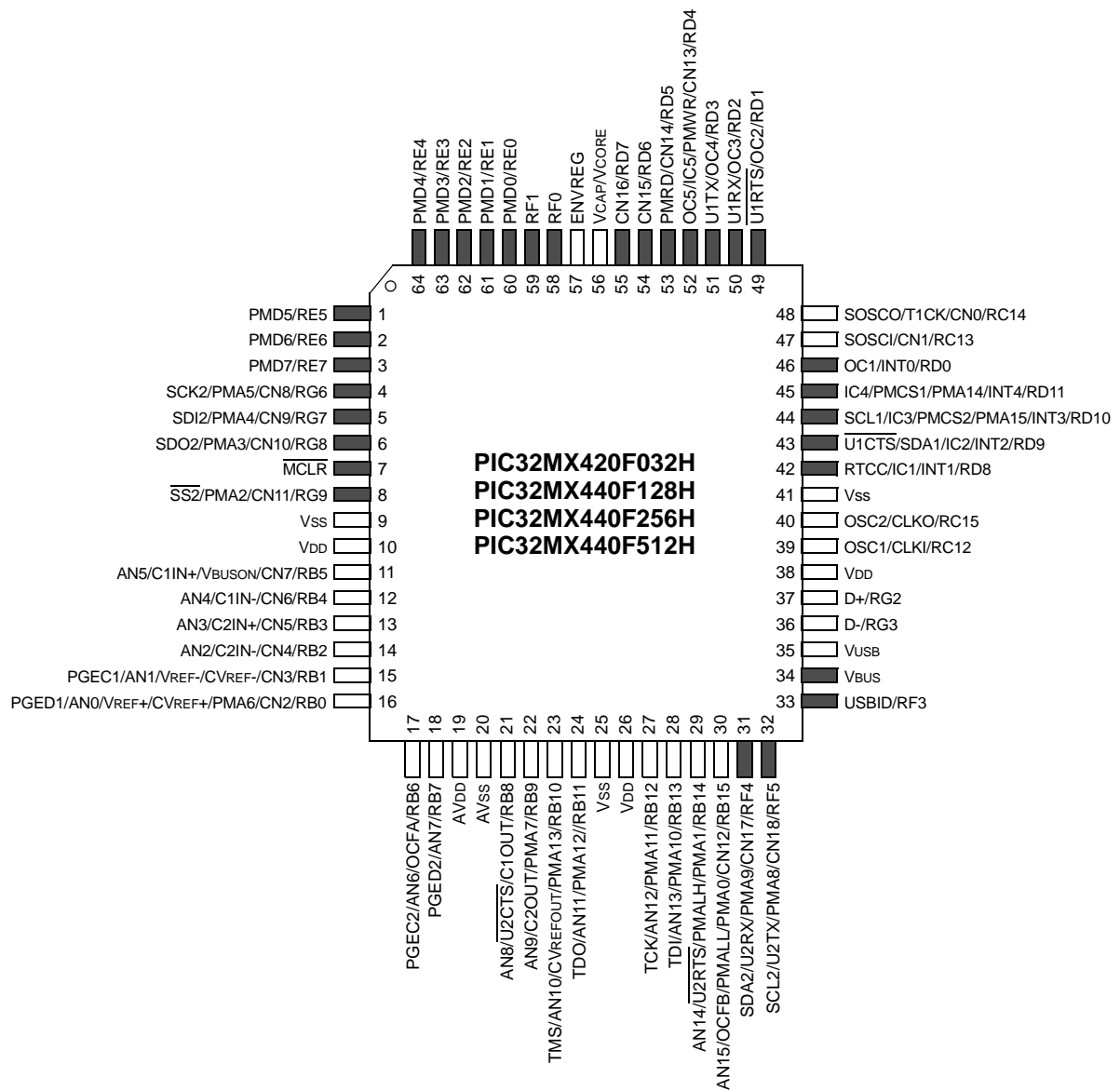- 31 SDA2/U2RX/PMA9/CN17/RF4
- 32 SCL2/U2TX/PMA8/CN18/RF5

Note: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Pin Diagrams (Continued)

64-Pin TQFP (USB)

■ = Pins are up to 5V tolerant

Top pins (left to right, 64 → 49):
64 PMD4/RE4
63 PMD3/RE3
62 PMD2/RE2
61 PMD1/RE1
60 PMD0/RE0
59 RF1
58 RF0
57 ENVREG
56 VCAP/VCORE
55 CN16/RD7
54 CN15/RD6
53 PMRD/CN14/RD5
52 OC5/IC5/PMWR/CN13/RD4
51 U1TX/OC4/RD3
50 U1RX/OC3/RD2
49 U1RTS/OC2/RD1

Left pins (1 → 16):
1 PMD5/RE5
2 PMD6/RE6
3 PMD7/RE7
4 SCK2/PMA5/CN8/RG6
5 SDI2/PMA4/CN9/RG7
6 SDO2/PMA3/CN10/RG8
7 MCLR
8 SS2/PMA2/CN11/RG9
9 Vss
10 VDD
11 AN5/C1IN+/VBUSON/CN7/RB5
12 AN4/C1IN-/CN6/RB4
13 AN3/C2IN+/CN5/RB3
14 AN2/C2IN-/CN4/RB2
15 PGEC1/AN1/VREF-/CVREF-/CN3/RB1
16 PGED1/AN0/VREF+/CVREF+/PMA6/CN2/RB0

Center labels:
PIC32MX420F032H
PIC32MX440F128H
PIC32MX440F256H
PIC32MX440F512H

Right pins (48 → 33):
48 SOSCO/T1CK/CN0/RC14
47 SOSCI/CN1/RC13
46 OC1/INT0/RD0
45 IC4/PMCS1/PMA14/INT4/RD11
44 SCL1/IC3/PMCS2/PMA15/INT3/RD10
43 U1CTS/SDA1/IC2/INT2/RD9
42 RTCC/IC1/INT1/RD8
41 Vss
40 OSC2/CLKO/RC15
39 OSC1/CLKI/RC12
38 VDD
37 D+/RG2
36 D-/RG3
35 VUSB
34 VBUS
33 USBID/RF3

Bottom pins (17 → 32):
17 PGEC2/AN6/OCFA/RB6
18 PGED2/AN7/RB7
19 AVDD
20 AVss
21 AN8/U2CTS/C1OUT/RB8
22 AN9/C2OUT/PMA7/RB9
23 TMS/AN10/CVREFOUT/PMA13/RB10
24 TDO/AN11/PMA12//RB11
25 Vss
26 VDD
27 TCK/AN12/PMA11/RB12
28 TDI/AN13/PMA10/RB13
29 AN14/U2RTS/PMALH/PMA1/RB14
30 AN15/OCFB/PMALL/PMA0/CN12/RB15
31 SDA2/U2RX/PMA9/CN17/RF4
32 SCL2/U2TX/PMA8/CN18/RF5

2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternately, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 2, MPLAB ICD 3 or MPLAB REAL ICE™.

For more information on ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- *"MPLAB® ICD 2 In-Circuit Debugger User's Guide"* DS51331
- *"Using MPLAB® ICD 2"* (poster) DS51265
- *"MPLAB® ICD 2 Design Advisory"* DS51566
- *"Using MPLAB® ICD 3"* (poster) DS51765
- *"MPLAB® ICD 3 Design Advisory"* DS51764
- *"MPLAB® REAL ICE™ In-Circuit Debugger User's Guide"* DS51616
- *"Using MPLAB® REAL ICE™"* (poster) DS51749

2.6 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternately, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

2.7 Trace

The trace pins can be connected to a hardware-trace-enabled programmer to provide a compress real time instruction trace. When used for trace the TRD3, TRD2, TRD1, TRD0 and TRCLK pins should be dedicated for this use. The trace hardware requires a 22 Ohm series resistor between the trace pins and the trace connector.

2.8 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT

PIC32MX3XX/4XX
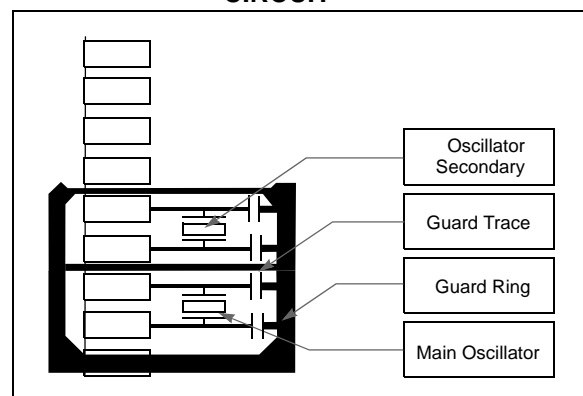
3.2 Architecture Overview

The MIPS32® M4K® Processor Core contains several logic blocks working together in parallel, providing an efficient high performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e Support
- Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The MIPS32® M4K® Processor Core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit general purpose registers used for integer operations and address calculation. One additional register file shadow set (containing thirty-two registers) is added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid stalls when executing instructions streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the CLZ and CLO instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- Shifter and Store Aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The MIPS32® M4K® Processor Core includes a multiply/divide unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the integer unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32MX core only checks the value of the latter (*rt)* operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If rs is 8 bits wide, 23 iterations are skipped. For a 16-bit-wide rs, 15 iterations are skipped, and for a 24-bit-wide rs, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32MX core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 4-13: ADC REGISTERS MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
9110	ADC1BUFA	31:16								ADC Result Word A (ADC1BUFA<31:0>)									0000
		15:0																	0000
9120	ADC1BUFB	31:16								ADC Result Word B (ADC1BUFB<31:0>)									0000
		15:0																	0000
9130	ADC1BUFC	31:16								ADC Result Word C (ADC1BUFC<31:0>)									0000
		15:0																	0000
9140	ADC1BUFD	31:16								ADC Result Word D (ADC1BUFD<31:0>)									0000
		15:0																	0000
9150	ADC1BUFE	31:16								ADC Result Word E (ADC1BUFE<31:0>)									0000
		15:0																	0000
9160	ADC1BUFF	31:16								ADC Result Word F (ADC1BUFF<31:0>)									0000
		15:0																	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

PIC32MX3XX/4XX

TABLE 4-43: USB REGISTERS MAP[1]

Virtual Address (BF88_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
5040	U1OTGIR[2]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF	0000
5050	U1OTGIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE	0000
5060	U1OTGSTAT[3]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD	0000
5070	U1OTGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
5080	U1PWRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UACTPND[4]	—	—	USLPGRD	—	—	USUSPEND	USBPWR	0000
5200	U1IR[2]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF	0000
																		DETACHIF	0000
5210	U1IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE	0000
																		DETACHIE	0000
5220	U1EIR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF	PIDEF	0000
																	EOFEF		0000
5230	U1EIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE	PIDEE	0000
																	EOFEE		0000
5240	U1STAT[3]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ENDPT<3:0>[4]				DIR	PPBI	—	—	0000
5250	U1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	JSTATE[4]	SE0[4]	PKTDIS	USBRST	HOSTEN	RESUME	PPBRST	USBEN	0000
													TOKBUSY					SOFEN	0000
5260	U1ADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPDEN	DEVADDR<6:0>							0000
5270	U1BDTP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRL<7:1>							—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: This register does not have associated CLR, SET, and INV registers.

3: All bits in this register are read-only; therefore, CLR, SET, and INV registers are not supported.

4: The reset value for this bit is undefined.

5.0 FLASH PROGRAM MEMORY

> **Note 1:** This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. "Flash Program Memory"** (DS61121) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

PIC32MX3XX/4XX devices contain an internal program Flash memory for executing user code. There are three methods by which the user can program this memory:

- Run-Time Self Programming (RTSP)
- In-Circuit Serial Programming™ (ICSP™)
- EJTAG Programming

RTSP is performed by software executing from either Flash or RAM memory. EJTAG is performed using the EJTAG port of the device and a EJTAG capable programmer. ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP. RTSP techniques are described in this chapter. The ICSP and EJTAG methods are described in the "*PIC32MX Flash Programming Specification*" (DS61145), which can be downloaded from the Microchip web site.

> **Note:** Flash LVD Delay (LVDstartup) must be taken into account between setting up and executing any Flash command operation. See Example 5-1 for a code example to set up and execute a Flash command operation.

EXAMPLE 5-1:

```
NVMCON = 0x4004;         // Enable and configure for erase operation
Wait(delay);             // Delay for 6 µs for LVDstartup

NVMKEY = 0xAA996655;
NVMKEY = 0x556699AA;
NVMCONSET = 0x8000;      // Initiate operation

while(NVMCONbits.WR==1); // Wait for current operation to complete
```

NOTES:

7.0   INTERRUPT CONTROLLER

> **Note 1:** This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupt Controller"** (DS61108) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

PIC32MX3XX/4XX devices generate interrupt requests in response to interrupt events from peripheral modules. The Interrupt Control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

The PIC32MX3XX/4XX interrupts module includes the following features:

- Up to 96 interrupt sources
- Up to 64 interrupt vectors
- Single and Multi-Vector mode operations
- Five external interrupts with edge polarity control
- Interrupt proximity timer
- Module Freeze in Debug mode
- Seven user-selectable priority levels for each vector
- Four user-selectable subpriority levels within each priority
- Dedicated shadow set for highest priority level
- Software can generate any interrupt
- User-configurable interrupt vector table location
- User-configurable interrupt vector spacing

FIGURE 7-1:   INTERRUPT CONTROLLER MODULE
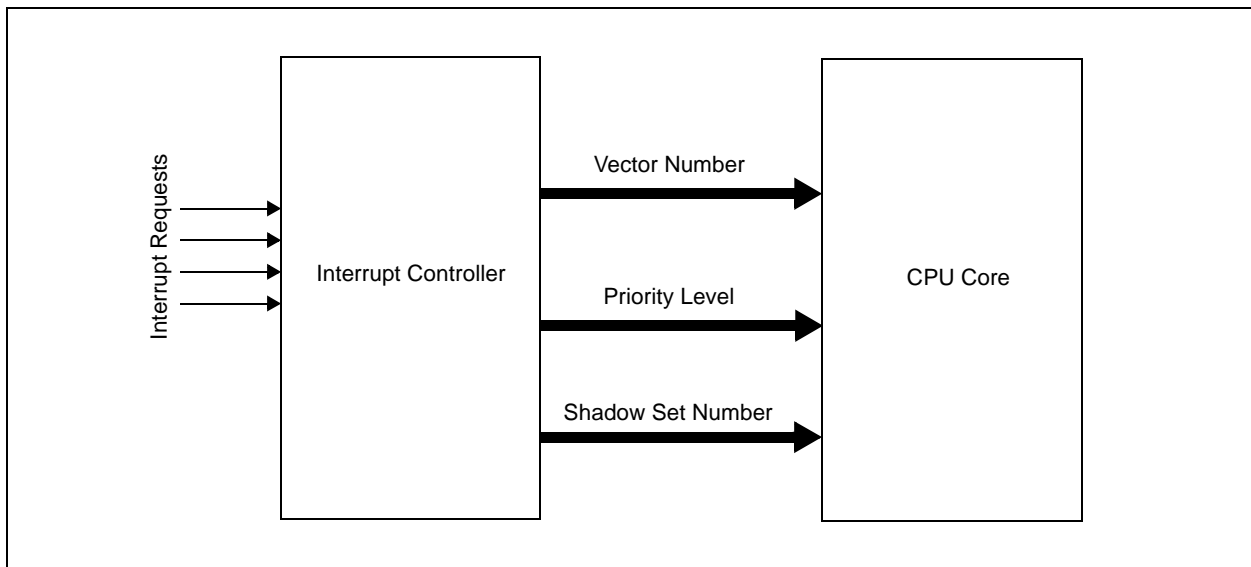
> **Note:** Several of the registers cited in this section are not in the interrupt controller module. These registers (and bits) are associated with the CPU. Details about them are available in **Section 3.0 "CPU"**.
>
> To avoid confusion, a typographic distinction is made for registers in the CPU. The register names in this section, and all other sections of this manual, are signified by uppercase letters only. The CPU register names are signified by upper and lowercase letters. For example, INTSTAT is an Interrupts register; whereas, IntCtl is a CPU register.

NOTES:

15.0   INPUT CAPTURE

> **Note 1:** This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS61122) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement. The PIC32MX3XX/4XX devices support up to five input capture channels.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The events that cause a capture event are listed below in three categories:

1. Simple Capture Event modes
   - Capture timer value on every falling edge of input at ICx pin
   - Capture timer value on every rising edge of input at ICx pin

2. Capture timer value on every edge (rising and falling)

3. Capture timer value on every edge (rising and falling), specified edge first.

4. Prescaler Capture Event modes
   - Capture timer value on every 4th rising edge of input at ICx pin
   - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

• Device wake-up from capture pin during CPU Sleep and Idle modes
• Interrupt on input capture event
• 4-word FIFO buffer for capture values
   - Interrupt optionally generated after 1, 2, 3 or 4 buffer locations are filled
• Input capture can also be used to provide additional sources of external interrupts

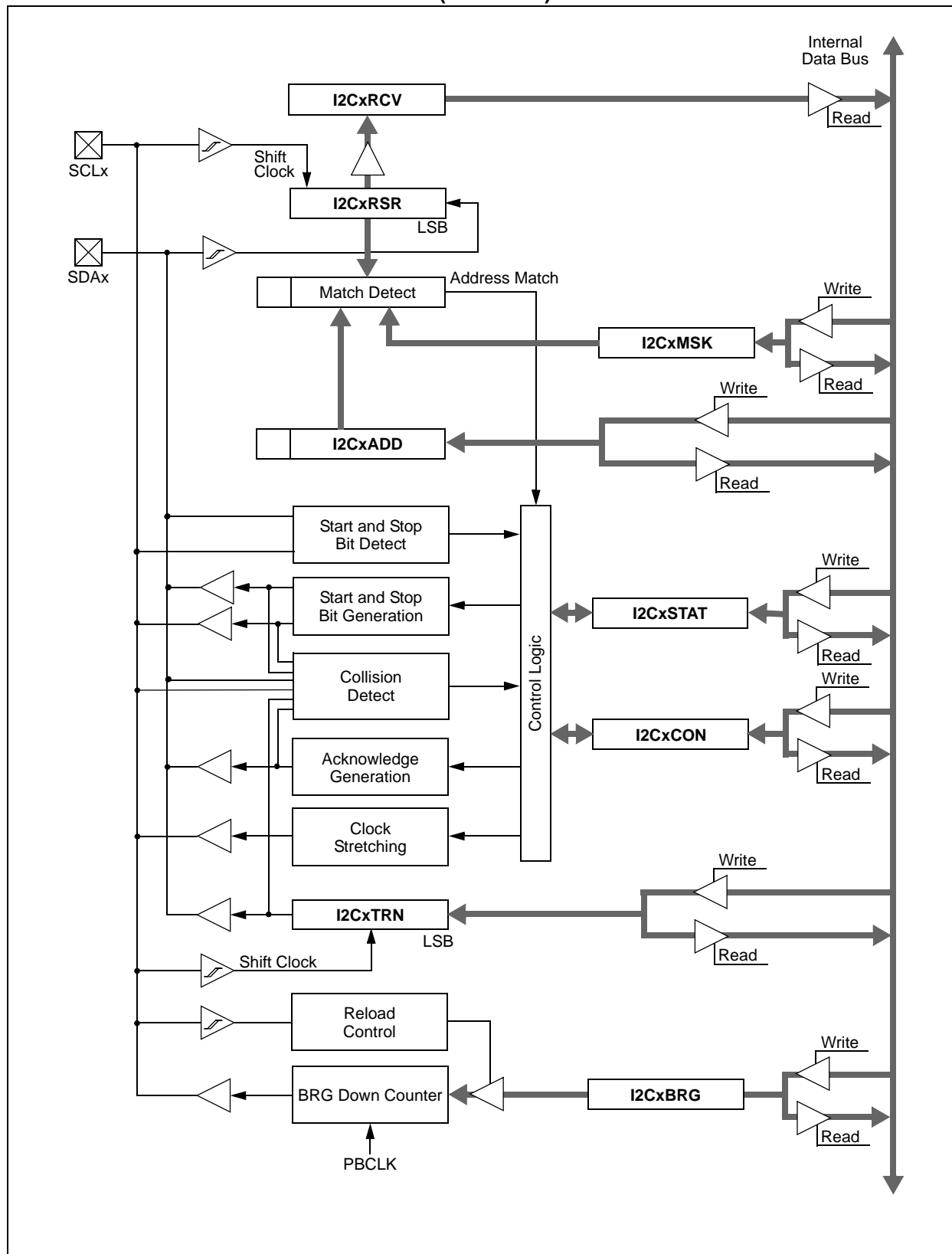**FIGURE 15-1:   INPUT CAPTURE BLOCK DIAGRAM**
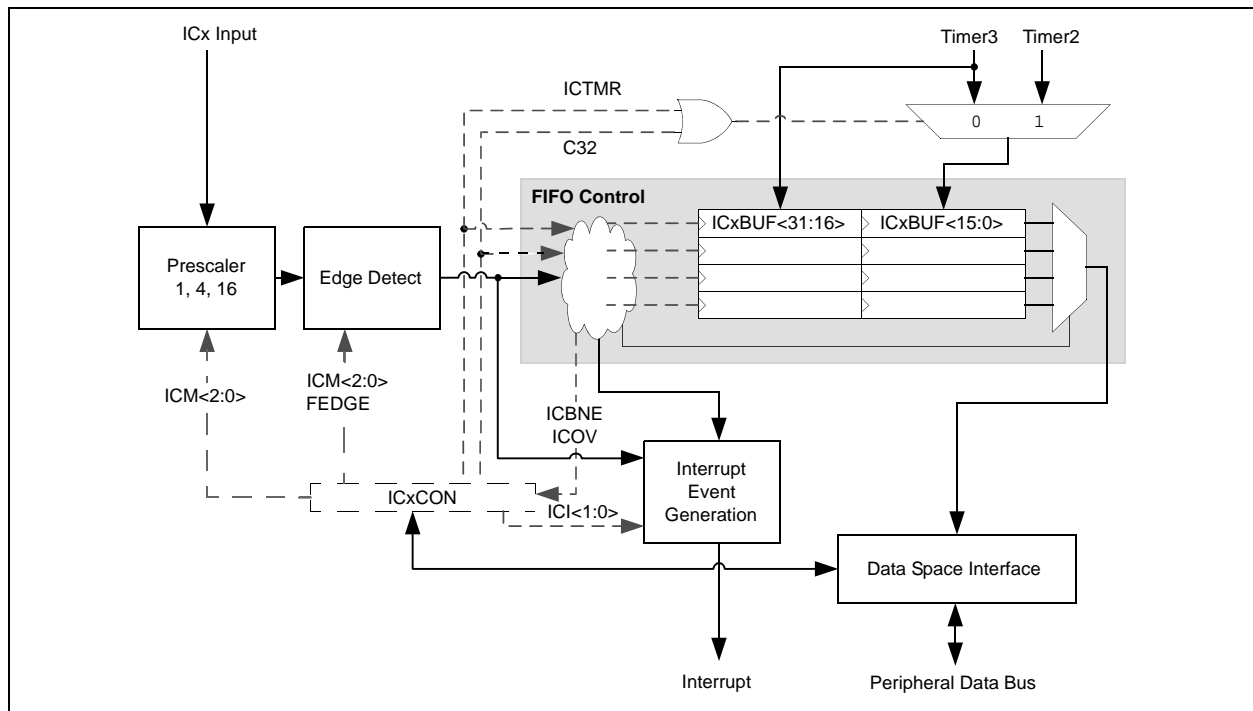
NOTES:

PIC32MX3XX/4XX

FIGURE 18-1: I²C™ BLOCK DIAGRAM (x = 1 OR 2)

REGISTER 26-2:   DEVCFG1: DEVICE CONFIGURATION WORD 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	R/P	r-1	r-1	R/P	R/P	R/P	R/P	R/P
	FWDTEN	—	—	WDTPS<4:0>				
15:8	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P
	IESO	—	FSOSCEN	—	—	FNOSC<2:0>		

Legend:

R = Readable bit   W = Writable bit   P = Programmable bit   r = Reserved bit

U = Unimplemented bit   -n = Bit Value at POR: ('0', '1', x = Unknown)

bit 31-24   **Reserved:** Write '1'

bit 23   **FWDTEN:** Watchdog Timer Enable bit

1 = The WDT is enabled and cannot be disabled by software
0 = The WDT is not enabled; it can be enabled in software

bit 22-21   **Reserved:** Write '1'

bit 20-16   **WDTPS<4:0>:** Watchdog Timer Postscale Select bits

10100 = 1:1048576
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1
All other combinations not shown result in operation = '10100'

bit 15-14   **FCKSM<1:0>:** Clock Switching and Monitor Selection Configuration bits

1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

Note 1:   Do not disable POSC (POSCMOD = 00) when using this oscillator source.

PIC32MX3XX/4XX

28.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

28.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

28.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

28.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

28.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

28.7   MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

28.8   MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

28.9   MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

28.10   PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC® and dsPIC® Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming™.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

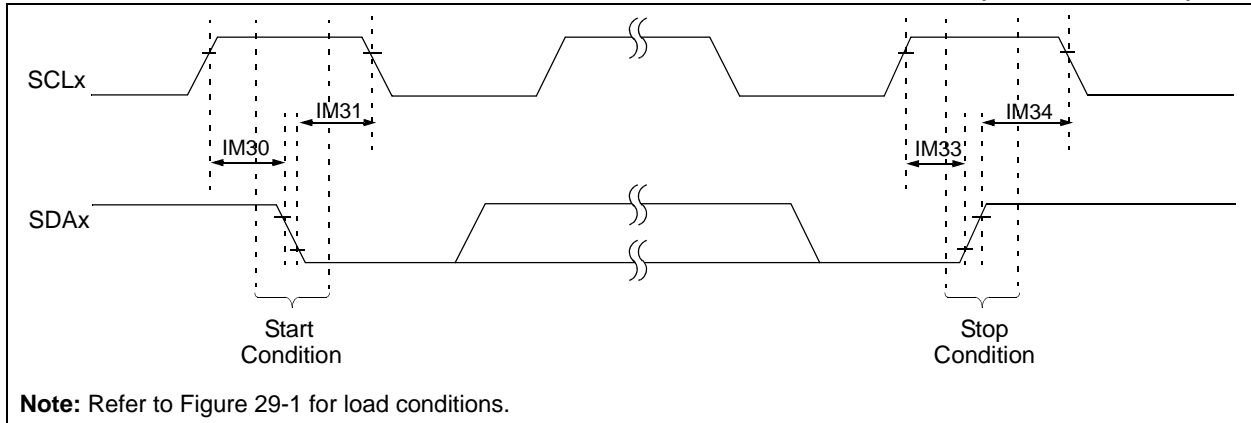**FIGURE 29-14:** **I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)**
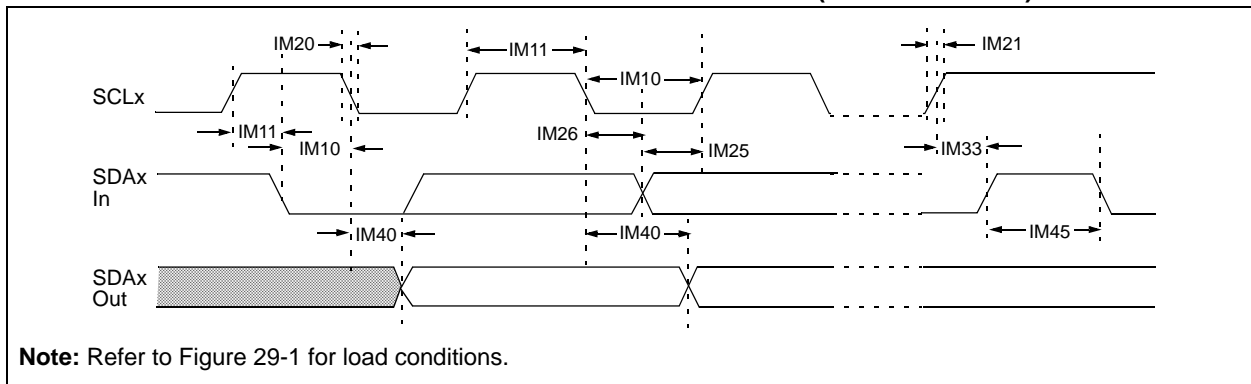

Note: Refer to Figure 29-1 for load conditions.

FIGURE 29-15: **I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)**

Note: Refer to Figure 29-1 for load conditions.

TABLE 29-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp			
Param. No.	Symbol	Characteristics		Min.[1]	Max.	Units	Conditions
IM10	$T_{LO:SCL}$	Clock Low Time	100 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	
			400 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	—
			1 MHz mode[2]	$T_{PB} * (BRG + 2)$	—	μs	
IM11	$T_{HI:SCL}$	Clock High Time	100 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	
			400 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	—
			1 MHz mode[2]	$T_{PB} * (BRG + 2)$	—	μs	
IM20	$T_{F:SCL}$	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF.
			400 kHz mode	$20 + 0.1 C_B$	300	ns	
			1 MHz mode[2]	—	100	ns	
IM21	$T_{R:SCL}$	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF.
			400 kHz mode	$20 + 0.1 C_B$	300	ns	
			1 MHz mode[2]	—	300	ns	
IM25	$T_{SU:DAT}$	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	—
			1 MHz mode[2]	100	—	ns	
IM26	$T_{HD:DAT}$	Data Input Hold Time	100 kHz mode	0	—	μs	
			400 kHz mode	0	0.9	μs	—
			1 MHz mode[2]	0	0.3	μs	
IM30	$T_{SU:STA}$	Start Condition Setup Time	100 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	Only relevant for Repeated Start condition.
			400 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	
			1 MHz mode[2]	$T_{PB} * (BRG + 2)$	—	μs	
IM31	$T_{HD:STA}$	Start Condition Hold Time	100 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	After this period, the first clock pulse is generated.
			400 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	
			1 MHz mode[2]	$T_{PB} * (BRG + 2)$	—	μs	
IM33	$T_{SU:STO}$	Stop Condition Setup Time	100 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	
			400 kHz mode	$T_{PB} * (BRG + 2)$	—	μs	—
			1 MHz mode[2]	$T_{PB} * (BRG + 2)$	—	μs	
IM34	$T_{HD:STO}$	Stop Condition Hold Time	100 kHz mode	$T_{PB} * (BRG + 2)$	—	ns	
			400 kHz mode	$T_{PB} * (BRG + 2)$	—	ns	—
			1 MHz mode[2]	$T_{PB} * (BRG + 2)$	—	ns	
IM40	$T_{AA:SCL}$	Output Valid from Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	—
			1 MHz mode[2]	—	350	ns	
IM45	$T_{BF:SDA}$	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus must be free before a new transmission can start.
			400 kHz mode	1.3	—	μs	
			1 MHz mode[2]	0.5	—	μs	
IM50	C_B	Bus Capacitive Loading		—	400	pF	—
IM51	T_{PGD}	Pulse Gobbler Delay[3]		52	312	ns	—

Note 1: BRG is the value of the I2C™ Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

TABLE 29-35: 10-BIT ADC CONVERSION RATE PARAMETERS[2]

Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +105°C for V-Temp					
ADC Speed	**T_{AD} Minimum**	**Sampling Time Min**	**Rs Max**	**V_{DD}**	**ADC Channels Configuration**
1 MIPS to 400 ksps[1]	65 ns	132 ns	500Ω	3.0V to 3.6V	ANx, SHA, CHx, ADC; VREF-, VREF+
Up to 400 ksps	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	ANx, ANx or VREF-, SHA, CHx, ADC; VREF- or AVSS, VREF+ or AVDD
Up to 300 ksps	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	ANx, ANx or VREF-, SHA, CHx, ADC; VREF- or AVSS, VREF+ or AVDD

Note 1: External VREF- and VREF+ pins must be used for correct operation.
2: These parameters are characterized, but not tested in manufacturing.

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
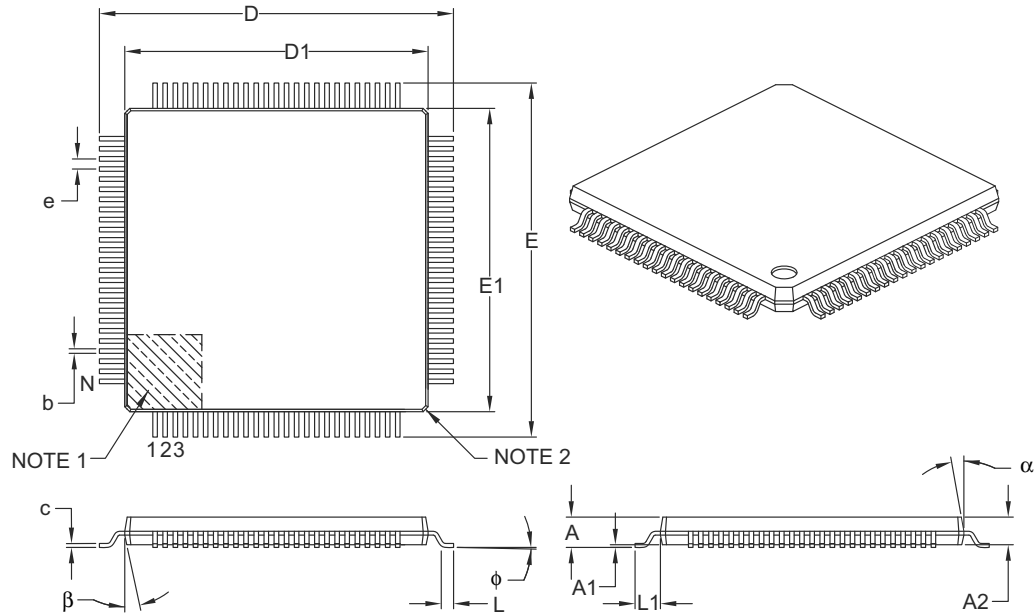
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		100	
Lead Pitch	e		0.40 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.13	0.18	0.23
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B