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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	53
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx320f032h-40v-mr

PIC32MX3XX/4XX

TABLE 1: PIC32MX GENERAL PURPOSE – FEATURES

GENERAL PURPOSE														
Device	Pins	Packages ⁽²⁾	MHz	Program Memory (KB)	Data Memory (KB)	Timers/Capture/Compare	Programmable DMA Channels	VREG	Trace	EUART/SPI/I ² C™	10-bit ADC (ch)	Comparators	PMP/PSP	JTAG
PIC32MX320F032H	64	PT, MR	40	32 + 12 ⁽¹⁾	8	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX320F064H	64	PT, MR	80	64 + 12 ⁽¹⁾	16	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX320F128H	64	PT, MR	80	128 + 12 ⁽¹⁾	16	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX340F128H	64	PT, MR	80	128 + 12 ⁽¹⁾	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX340F256H	64	PT, MR	80	256 + 12 ⁽¹⁾	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX340F512H	64	PT, MR	80	512 + 12 ⁽¹⁾	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX320F128L	100	PT	80	128 + 12 ⁽¹⁾	16	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes
	121	BG												
PIC32MX340F128L	100	PT	80	128 + 12 ⁽¹⁾	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes
	121	BG												
PIC32MX360F256L	100	PT	80	256 + 12 ⁽¹⁾	32	5/5/5	4	Yes	Yes	2/2/2	16	2	Yes	Yes
	121	BG												
PIC32MX360F512L	100	PT	80	512 + 12 ⁽¹⁾	32	5/5/5	4	Yes	Yes	2/2/2	16	2	Yes	Yes
	121	BG												

Legend: PT = TQFP MR = QFN BG = XBGA

Note 1: This device features 12 KB Boot Flash memory.

Note 2: See Legend for an explanation of the acronyms. See **Section 30.0 “Packaging Information”** for details.

Pin Diagrams (Continued)

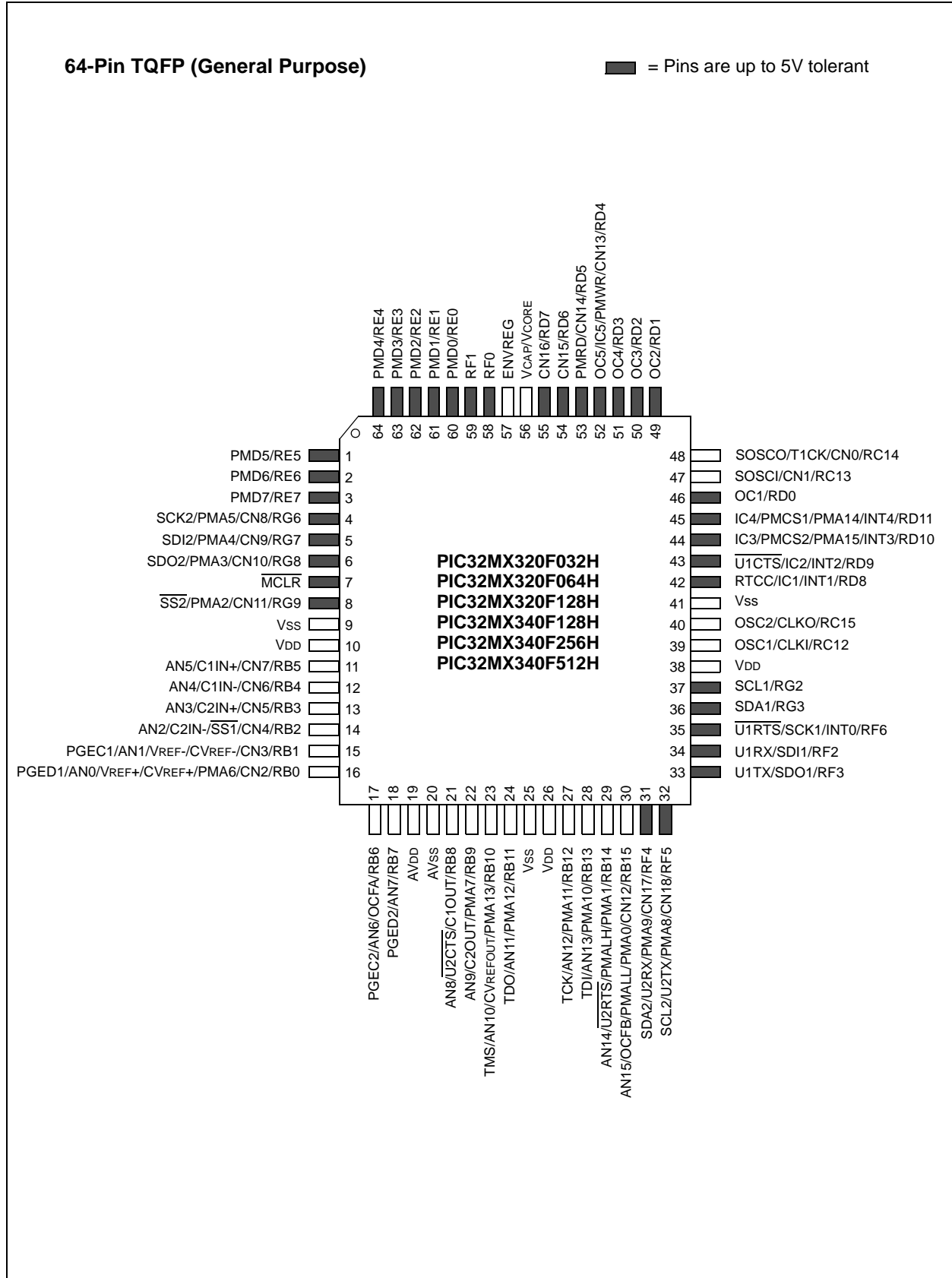


TABLE 4: PIN NAMES: PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES (CONTINUED)

Pin Number	Full Pin Name
K4	AN8/C1OUT/RB8
K5	No Connect (NC)
K6	$\overline{U2CTS}$ /RF12
K7	AN14/PMALH/PMA1/RB14
K8	VDD
K9	$\overline{U1RTS}$ /CN21/RD15
K10	USBID/RF3
K11	U1RX/RF2
L1	PGEC2/AN6/OCFA/RB6
L2	VREF-/CVREF-/PMA7/RA9

Pin Number	Full Pin Name
L3	AVSS
L4	AN9/C2OUT/RB9
L5	AN10/CVREFOUT/PMA13/RB10
L6	$\overline{U2RTS}$ /RF13
L7	AN13/PMA10/RB13
L8	AN15/OCFB/PMALL/PMA0/CN12/RB15
L9	$\overline{U1CTS}$ /CN20/RD14
L10	U2RX/PMA9/CN17/RF4
L11	U2TX/PMA8/CN18/RF5

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An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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TABLE 4-4: INTERRUPT REGISTERS MAP FOR PIC32MX320F032H, PIC32MX320F064H, PIC32MX320F128H AND PIC32MX320F128L DEVICES ONLY⁽¹⁾

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000
		15:0	—	—	—	MVEC	—	—	—	—	—	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP
1010	INTSTAT ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	SPI1RXIF	SPI1TXIF	SPI1EIF	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	—	—	—	—	—	—	—	FCEIF	—	—	—	—	—	—	—	—	0000
		15:0	RTCCIF	FSCMIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF	SPI2RXIF	SPI2TXIF	SPI2EIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	SPI1RXIE	SPI1TXIE	SPI1EIE	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	—	—	—	—	—	—	—	FCEIE	—	—	—	—	—	—	—	—	0000
		15:0	RTCCIE	FSCMIE	I2C2MIE	—	—	—	—	—	SPI2RXIE	SPI2TXIE	SPI2EIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000
1090	IPC0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
10A0	IPC1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
10B0	IPC2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
10C0	IPC3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
10D0	IPC4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
10E0	IPC5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
10F0	IPC6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
1100	IPC7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
1110	IPC8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
1140	IPC11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 “CLR, SET and INV Registers” for more information.

2: This register does not have associated CLR, SET, and INV registers.

TABLE 4-23: PORTC REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L, PIC32MX360F512L, PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY⁽¹⁾

Virtual Address (BF88_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
6080	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	TRISC4	TRISC3	TRISC2	TRISC1	—	F01E
6090	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	RC4	RC3	RC2	RC1	—	xxxxx
60A0	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	LATC4	LATC3	LATC2	LATC1	—	xxxxx
60B0	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	ODCC4	ODCC3	ODCC2	ODCC1	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 “CLR, SET and INV Registers” for more information.

TABLE 4-24: PORTC REGISTERS MAP FOR PIC32MX320F032H, PIC32MX320F064H, PIC32MX320F128H, PIC32MX340F128H, PIC32MX340F256H, PIC32MX340F512H, PIC32MX420F032H, PIC32MX440F128H, PIC32MX440F256H AND PIC32MX440F512H DEVICES ONLY⁽¹⁾

Virtual Address (BF88_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
6080	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	—	—	—	—	—	F000
6090	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxxx
60A0	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxxx
60B0	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 “CLR, SET and INV Registers” for more information.

TABLE 4-40: RTCC REGISTERS MAP⁽¹⁾

Virtual Address (BF80_#)	Register Name	Bit Range	Bits														All Resets		
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2		17/1	16/0
0200	RTCCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	ON	—	SIDL	—	—	—	—	—	RTSECSEL	RTCCLKON	—	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	0000
0210	RTCALRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	ALRMEN	CHIME	PIV	ALRMSYNC	AMASK<3:0>				ARPT<7:0>							0000	
0220	RTCTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0230	RTCDATE	31:16	YEAR10<3:0>				YEAR01<3:0>				MONTH10<3:0>				MONTH01<3:0>				xxxx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx0x
0240	ALRMTIME	31:16	MIN10<3:0>				MIN01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0250	ALRMDATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	00xx	
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx0x

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-41: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits														All Resets		
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2		17/1	16/0
2FF0	DEVCFG3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx	
		15:0	USERID15	USERID14	USERID13	USERID12	USERID11	USERID10	USERID9	USERID8	USERID7	USERID6	USERID5	USERID4	USERID3	USERID2	USERID1	USERID0	xxxx
2FF4	DEVCFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	FPLL0DIV<2:0>			xxxx	
		15:0	UPLLEN ⁽¹⁾	—	—	—	—	UPLLDIV<2:0> ⁽¹⁾				—	FPLLMUL<2:0>			—	FPLLDIV<2:0>		xxxx
2FF8	DEVCFG1	31:16	—	—	—	—	—	—	—	—	FWDTEN	—	—	WDTPS<4:0>				xxxx	
		15:0	FCKSM<1:0>			FPBDIV<1:0>		—	OSCI0FNC	POSCMOD<1:0>		IESO	—	FSOSCEN	—	—	FNOSC<2:0>		
2FFC	DEVCFG0	31:16	—	—	—	CP	—	—	—	BWP	—	—	—	—	PWP19	PWP18	PWP17	PWP16	xxxx
		15:0	PWP15	PWP14	PWP13	PWP12	—	—	—	—	—	—	—	—	—	—	—	—	—

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These bits are only available on PIC32MX4XX devices.

10.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. “Direct Memory Access (DMA) Controller”** (DS61117) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The PIC32MX Direct Memory Access (DMA) controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the PIC32MX (such as Peripheral Bus (PBUS) devices: SPI, UART, PMP, and so on) or memory itself.

Following are some of the key features of the DMA controller module:

- Four Identical Channels, each featuring:
 - Auto-Increment Source and Destination Address Registers
 - Source and Destination Pointers
 - Memory to Memory and Memory to Peripheral Transfers

- Automatic Word-Size Detection:
 - Transfer Granularity, down to byte level
 - Bytes need not be word-aligned at source and destination
- Fixed Priority Channel Arbitration
- Flexible DMA Channel Operating Modes:
 - Manual (software) or automatic (interrupt) DMA requests
 - One-Shot or Auto-Repeat Block Transfer modes
 - Channel-to-channel chaining
- Flexible DMA Requests:
 - A DMA request can be selected from any of the peripheral interrupt sources
 - Each channel can select any (appropriate) observable interrupt as its DMA request source
 - A DMA transfer abort can be selected from any of the peripheral interrupt sources
 - Pattern (data) match transfer termination
- Multiple DMA Channel Status Interrupts:
 - DMA channel block transfer complete
 - Source empty or half empty
 - Destination full or half-full
 - DMA transfer aborted due to an external event
 - Invalid DMA address generated
- DMA Debug Support Features:
 - Most recent address accessed by a DMA channel
 - Most recent DMA channel to transfer data
- CRC Generation Module:
 - CRC module can be assigned to any of the available channels
 - CRC module is highly configurable

FIGURE 10-1: DMA BLOCK DIAGRAM



PIC32MX3XX/4XX

NOTES:

PIC32MX3XX/4XX

NOTES:

REGISTER 26-3: DEVCFG2: DEVICE CONFIGURATION WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —
23:16	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	R/P FPLLLODIV<2:0>	R/P FPLLLODIV<2:0>	R/P FPLLLODIV<2:0>
15:8	R/P UPLLEN	r-1 —	r-1 —	r-1 —	r-1 —	R/P UPLLDIV<2:0>	R/P UPLLDIV<2:0>	R/P UPLLDIV<2:0>
7:0	r-1 —	R/P FPLLMUL<2:0>	R/P FPLLMUL<2:0>	R/P FPLLMUL<2:0>	r-1 —	R/P FPLLIDIV<2:0>	R/P FPLLIDIV<2:0>	R/P FPLLIDIV<2:0>

Legend:

R = Readable bit W = Writable bit P = Programmable bit r = Reserved bit
 U = Unimplemented bit -n = Bit Value at POR: ('0', '1', x = Unknown)

bit 31-19 **Reserved:** Write '1'

bit 18-16 **FPLLLODIV<2:0>:** Default Postscaler for PLL bits

- 111 = PLL output divided by 256
- 110 = PLL output divided by 64
- 101 = PLL output divided by 32
- 100 = PLL output divided by 16
- 011 = PLL output divided by 8
- 010 = PLL output divided by 4
- 001 = PLL output divided by 2
- 000 = PLL output divided by 1

bit 15 **UPLLEN:** USB PLL Enable bit
 1 = Disable and bypass USB PLL
 0 = Enable USB PLL

bit 14-11 **Reserved:** Write '1'

bit 10-8 **UPLLDIV<2:0>:** PLL Input Divider bits

- 111 = 12x divider
- 110 = 10x divider
- 101 = 6x divider
- 100 = 5x divider
- 011 = 4x divider
- 010 = 3x divider
- 010 = 3x divider
- 001 = 2x divider
- 000 = 1x divider

bit 7 **Reserved:** Write '1'

bit 6-4 **FPLLMUL<2:0>:** PLL Multiplier bits

- 111 = 24x multiplier
- 110 = 21x multiplier
- 101 = 20x multiplier
- 100 = 19x multiplier
- 011 = 18x multiplier
- 010 = 17x multiplier
- 001 = 16x multiplier
- 000 = 15x multiplier

bit 3 **Reserved:** Write '1'

bit 2-0 **FPLLIDIV<2:0>:** PLL Input Divider bits

- 111 = 12x divider
- 110 = 10x divider
- 101 = 6x divider
- 100 = 5x divider
- 011 = 4x divider
- 010 = 3x divider
- 001 = 2x divider
- 000 = 1x divider

28.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB C Compiler for Various Device Families
 - HI-TECH C for Various Device Families
 - MPASM™ Assembler
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
 - MPLAB ICD 3
 - PICKit™ 3 Debug Express
- Device Programmers
 - PICKit™ 2 Programmer
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

28.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
 - Simulator
 - Programmer (sold separately)
 - In-Circuit Emulator (sold separately)
 - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
 - Source files (C or assembly)
 - Mixed C and assembly
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

PIC32MX3XX/4XX

29.1 DC Characteristics

TABLE 29-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)	Temp. Range (in °C)	Max. Frequency
			PIC32MX3XX/4XX
DC5	2.3V-3.6V	-40°C to +85°C	80 MHz (Note 1)
DC5b	2.3V-3.6V	-40°C to +105°C	80 MHz (Note 1)

Note 1: 40 MHz maximum for PIC32MX320F032H and PIC32MX420F032H devices.

TABLE 29-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typical	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
V-Temp Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+105	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – S IOH) I/O Pin Power Dissipation: I/O = S ((VDD – VOH) x IOH) + S (VOL x IOL)	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 29-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typical	Max.	Unit	Notes
Package Thermal Resistance, 121-Pin XBGA (10x10x1.1 mm)	θJA	40	—	°C/W	1
Package Thermal Resistance, 100-Pin TQFP (12x12x1 mm)	θJA	43	—	°C/W	1
Package Thermal Resistance, 64-Pin TQFP (10x10x1 mm)	θJA	47	—	°C/W	1
Package Thermal Resistance, 64-Pin QFN (9x9x0.9 mm)	θJA	28	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

TABLE 29-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp					
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Operating Voltage							
DC10	VDD	Supply Voltage	2.3	—	3.6	V	—
DC12	VDR	RAM Data Retention Voltage (Note 1)	1.75	—	—	V	—
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	1.75	—	1.95	V	—
DC17	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.05	—	—	V/ms	—

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

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TABLE 29-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp			
Parameter No.	Typical ⁽²⁾	Max.	Units	Conditions		
Module Differential Current (Continued)						
DC43	—	1100	μA	-40°C	2.5V	ADC: ΔI _{ADC} (Notes 3, 4, 6)
DC43a	—	1100	μA	+25°C		
DC43b	—	1000	μA	+85°C		
DC43h	—	1200	μA	+105°C		
DC43c	880	—	μA	—	—	ADC: ΔI _{ADC} (Notes 3, 4)
DC43e	—	1100	μA	-40°C	3.6V	ADC: ΔI _{ADC} (Notes 3, 4)
DC43f	—	1100	μA	+25°C		
DC43g	—	1000	μA	+85°C		
DC43i	—	1200	μA	+105°C		

- Note 1:** Base IPD is measured with all digital peripheral modules disabled. All I/Os are configured as inputs and pulled low. WDT and FSCM are disabled.
- 2:** Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.
- 4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.
- 5:** Data is characterized at +70°C and not tested. Parameter is for design guidance only.
- 6:** This parameter is characterized, but not tested in manufacturing.

TABLE 29-34: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.5	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module Vss Supply	Vss	—	Vss + 0.3	V	—
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 2.0	—	AVDD	V	(Note 1)
AD05a			2.5	—	3.6	V	VREFH = AVDD (Note 3)
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 2.0	V	(Note 1)
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	2.0	—	AVDD	V	(Note 3)
AD08	IREF	Current Drain	—	250 —	400 3	μA μA	ADC operating ADC off
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	—
AD13	VINL	Absolute VINL Input Voltage	AVSS – 0.3	—	AVDD/2	V	—
AD14	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	—
AD15	—	Leakage Current	—	± 0.001	± 0.610	μA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V Source Impedance = 10K Ω
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	5K	Ω	(Note 1)
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	10 data bits			bits	—
AD21c	INL	Integral Nonlinearity	—	—	$< \pm 1$	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD22c	DNL	Differential Nonlinearity	—	—	$< \pm 1$	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V (Note 2)
AD23c	GERR	Gain Error	—	—	$< \pm 1$	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD24n	E _{OFF}	Offset Error	—	—	$< \pm 1$	LSb	VINL = AVSS = 0V, AVDD = 3.3V
AD25c	—	Monotonicity	—	—	—	—	Guaranteed

Note 1: These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

3: These parameters are characterized, but not tested in manufacturing.

4: Characterized with 1 kHz sine wave.

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NOTES:

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64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.15 x 7.15 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-149C Sheet 1 of 2

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TABLE A-3: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 29.0 “Electrical Characteristics”	<p>Added the new V-Temp temperature range (-40°C to +105°C) to the heading of all specification tables.</p> <p>Updated the Ambient temperature under bias, updated the Voltage on any 5V tolerant pin with respect to V_{SS} when V_{DD} < 2.3V, and added Voltage on V_{BUS} with respect to V_{SS} in Absolute Maximum Ratings.</p> <p>Added the characteristic, DC5a to Operating MIPS vs. Voltage (see Table 29-1).</p> <p>Updated or added the following parameters to the Operating Current (I_{DD}) DC Characteristics: DC20, DC23, DC24c, DC25d, DC26c (see Table 29-5).</p> <p>Added the following parameters to the Idle Current (I_{IDLE}) DC Characteristics: DC30c, DC31c, DC32c, DS33c, DC34c, DC35c, and DC36c (see Table 29-6).</p> <p>Added the following parameters to the Power-down Current (I_{PD}) DC Characteristics: DC40g, DC40h, DC40i, DC41g, DC41h, DC42g, DC42h, DC42i, DC43h, and DC43i (see Table 29-7).</p> <p>Added the Brown-out Reset (BOR) Electrical Characteristics (see Table 29-10).</p> <p>Removed all Conditions from the Program Memory DC Characteristics (see Table 29-11).</p> <p>Removed the AC Characteristics voltage reference table (Table 29-15).</p> <p>Added Note 2 to the PLL Clock Timing Specifications (see Table 29-18).</p> <p>Updated the OC/PWM Module Timing Characteristics (see Figure 29-9).</p> <p>Added parameter IM51 and Note 3 to the I²Cx Bus Data Timing Requirements (Master Mode) (see Table 29-32).</p> <p>Added parameter numbers (AD13, AD14, and AD15) to the ADC Module Specifications (see Table 29-34).</p> <p>Updated the 10-bit ADC Conversion Rate Parameters (see Table 29-35).</p> <p>Updated parameter AD57 (TSAMP) in the Analog-to-Digital Conversion Timing Requirements (see Table 29-36).</p> <p>Updated the Conditions for parameters USB313, USB318, and USB319 in the OTG Electrical Specifications (see Table 29-40).</p>
Section 30.0 “Packaging Information”	<p>Updated the 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] packing diagram.</p>
Product Identification System	<p>Added the new V-Temp (V) temperature information.</p>

Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

	PIC32 MX 3XX F 512 H T - 80 I / PT - XXX	
Microchip Brand _____		Examples: PIC32MX320F032H-40I/PT: General purpose PIC32MX, 32 KB program memory, 64-pin, Industrial temperature, TQFP package. PIC32MX360F256L-80I/PT: General purpose PIC32MX, 256 KB program memory, 100-pin, Industrial temperature, TQFP package.
Architecture _____		
Product Groups _____		
Flash Memory Family _____		
Program Memory Size (KB) _____		
Pin Count _____		
Tape and Reel Flag (if applicable) _____		
Speed _____		
Temperature Range _____		
Package _____		
Pattern _____		

Flash Memory Family	
Architecture	MX = 32-bit RISC MCU core
Product Groups	3XX = General purpose microcontroller family 4XX = USB
Flash Memory Family	F = Flash program memory
Program Memory Size	32 = 32K 64 = 64K 128 = 128K 256 = 256K 512 = 512K
Speed	40 = 40 MHz 80 = 80 MHz
Pin Count	H = 64-pin L = 100-pin
Temperature Range	I = -40°C to +85°C (Industrial) V = -40°C to +105°C (V-Temp)
Package	PT = 64-Lead (10x10x1 mm) TQFP (Thin Quad Flatpack) PT = 100-Lead (12x12x1 mm) TQFP (Thin Quad Flatpack) MR = 64-Lead (9x9x0.9 mm) QFN (Plastic Quad Flat) BG = 121-Lead (10x10x1.1 mm) XBGA (Plastic Thin Profile Ball Grid Array)
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES = Engineering Sample

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