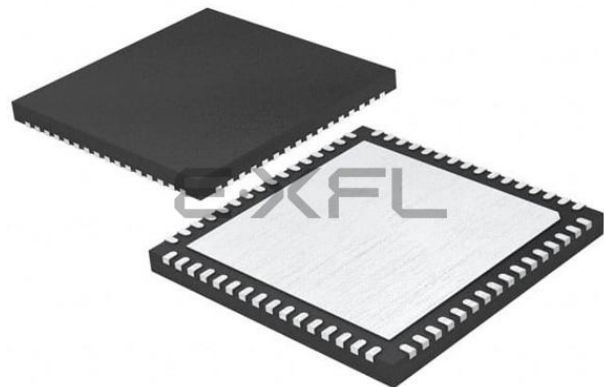




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

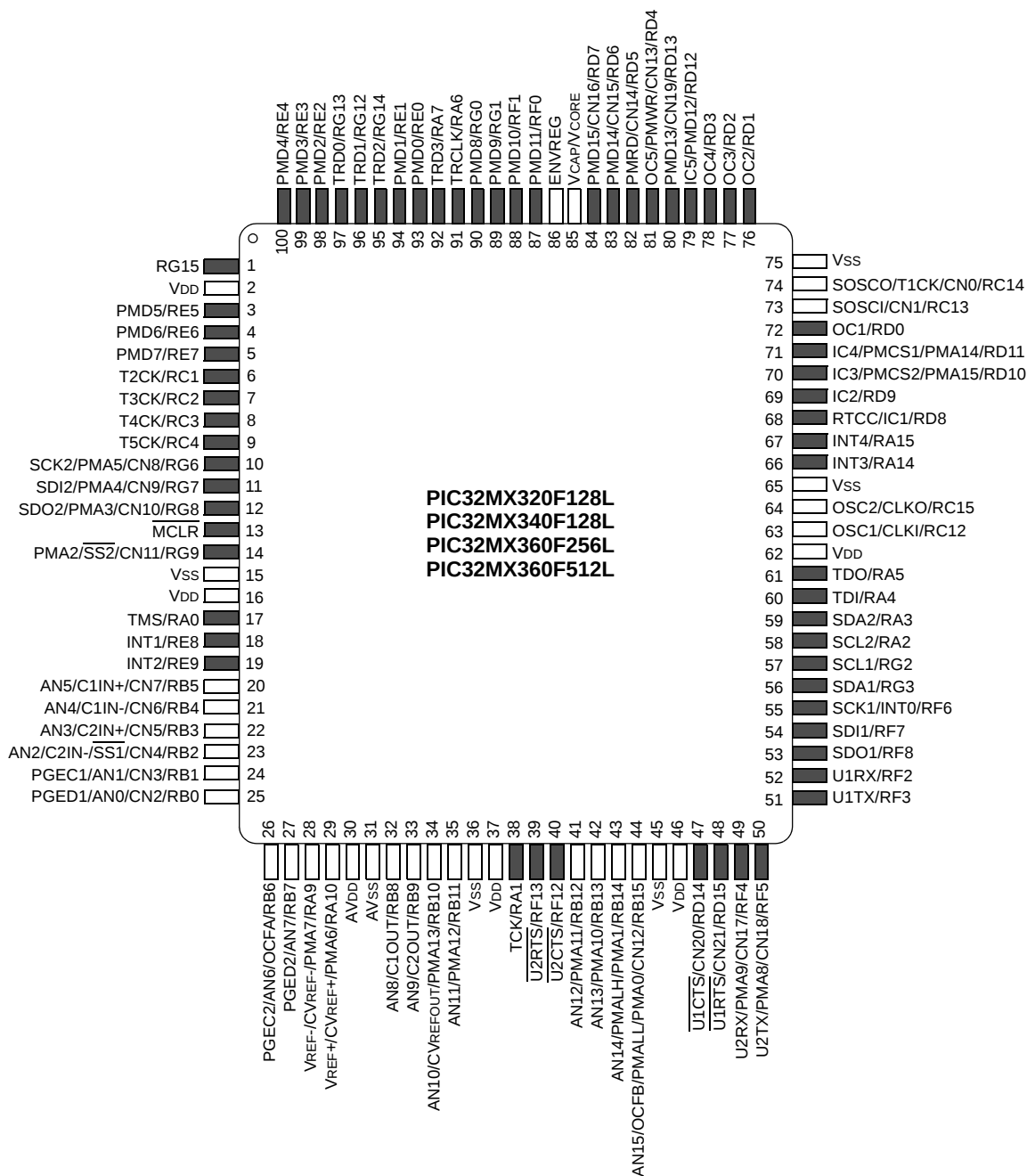
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	53
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx320f032ht-40i-mr

PIC32MX3XX/4XX

Pin Diagrams (Continued)

100-Pin TQFP (General Purpose)

■ = Pins are up to 5V tolerant

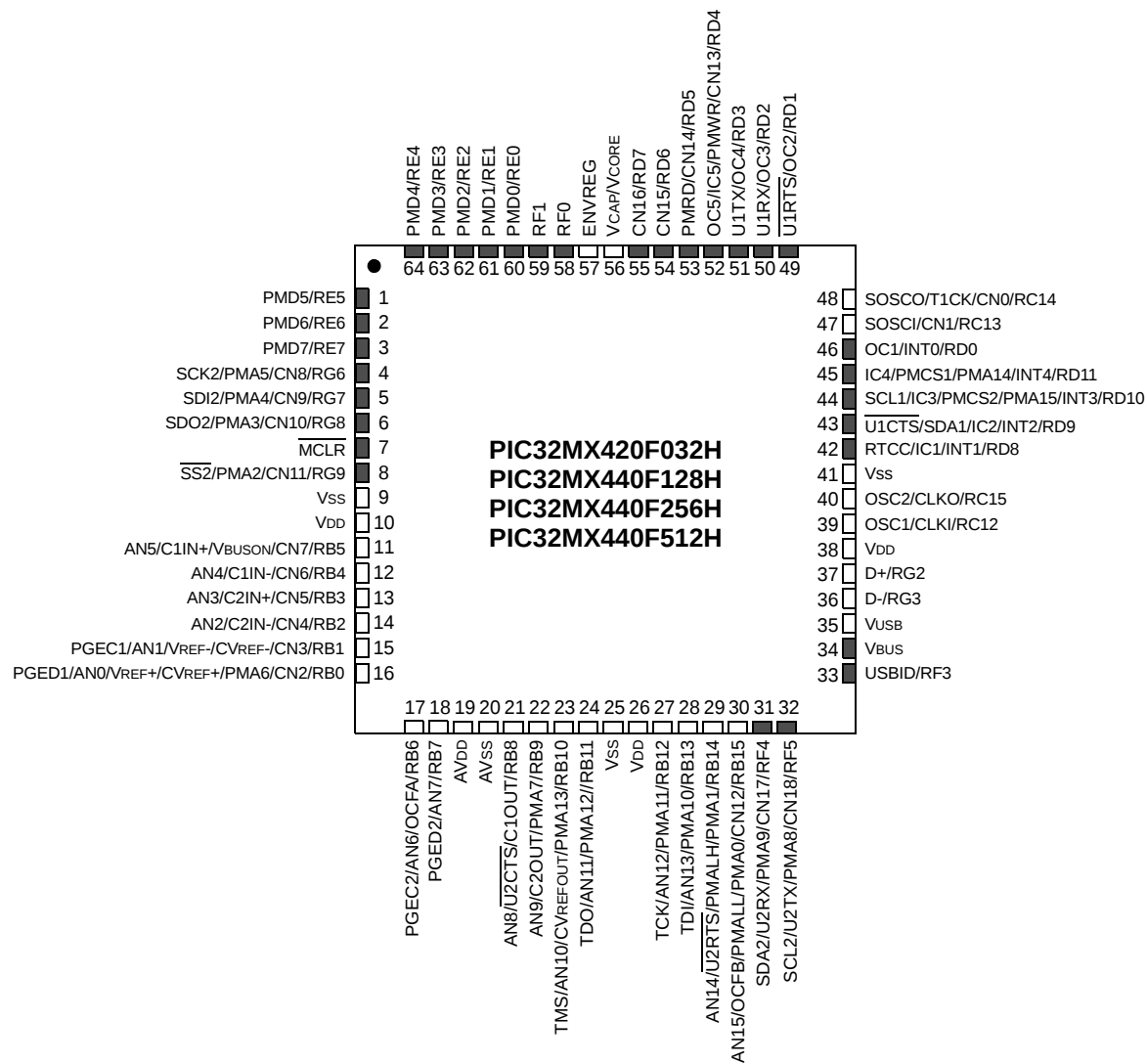


PIC32MX3XX/4XX

Pin Diagrams (Continued)

64-Pin QFN (USB)

■ = Pins are up to 5V tolerant



Note: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to V_{SS} externally.

PIC32MX3XX/4XX

TABLE 4: PIN NAMES: PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES

Pin Number	Full Pin Name
A1	PMD4/RE4
A2	PMD3/RE3
A3	TRD0/RG13
A4	PMD0/RE0
A5	PMD8/RG0
A6	PMD10/RF1
A7	ENVREG
A8	Vss
A9	IC5/PMD12/RD12
A10	OC3/RD2
A11	OC2/RD1
B1	No Connect (NC)
B2	RG15
B3	PMD2/RE2
B4	PMD1/RE1
B5	TRD3/RA7
B6	PMD11/RF0
B7	VCAP/VCORE
B8	PMRD/CN14/RD5
B9	OC4/RD3
B10	Vss
B11	SOSCO/T1CK/CN0/RC14
C1	PMD6/RE6
C2	VDD
C3	TRD1/RG12
C4	TRD2/RG14
C5	TRCLK/RA6
C6	No Connect (NC)
C7	PMD15/CN16/RD7
C8	OC5/PMWR/CN13/RD4
C9	VDD
C10	SOSCI/CN1/RC13
C11	IC4/PMCS1/PMA14/RD11
D1	T2CK/RC1
D2	PMD7/RE7
D3	PMD5/RE5
D4	Vss
D5	Vss
D6	No Connect (NC)
D7	PMD14/CN15/RD6
D8	CN19/PMD13/RD13
D9	SDO1/OC1/INT0/RD0
D10	No Connect (NC)
D11	SCK1/IC3/PMCS2/PMA15/RD10
E1	T5CK/SDI1/RC4
E2	T4CK/RC3
E3	SCK2/PMA5/CN8/RG6
E4	T3CK/RC2
E5	VDD
E6	PMD9/RG1
E7	Vss

Pin Number	Full Pin Name
E8	SDA1/INT4/RA15
E9	RTCC/IC1/RD8
E10	SS1/IC2/RD9
E11	SCL1/INT3/RA14
F1	MCLR
F2	SDO2/PMA3/CN10/RG8
F3	SS2/PMA2/CN11/RG9
F4	SDI2/PMA4/CN9/RG7
F5	Vss
F6	No Connect (NC)
F7	No Connect (NC)
F8	Vdd
F9	OSC1/CLKI/RC12
F10	Vss
F11	OSC2/CLKO/RC15
G1	INT1/RE8
G2	INT2/RE9
G3	TMS/RA0
G4	No Connect (NC)
G5	VDD
G6	Vss
G7	Vss
G8	No Connect (NC)
G9	TDO/RA5
G10	SDA2/RA3
G11	TDI/RA4
H1	AN5/C1IN+/VBUSON/CN7/RB5
H2	AN4/C1IN-/CN6/RB4
H3	Vss
H4	VDD
H5	No Connect (NC)
H6	VDD
H7	No Connect (NC)
H8	VBUS
H9	VUSB
H10	D+/RG2
H11	SCL2/RA2
J1	AN3/C2IN+/CN5/RB3
J2	AN2/C2IN-/CN4/RB2
J3	PGED2/AN7/RB7
J4	AVDD
J5	AN11/PMA12/RB11
J6	TCK/RA1
J7	AN12/PMA11/RB12
J8	No Connect (NC)
J9	No Connect (NC)
J10	U1TX/RF8
J11	D-/RG3
K1	PGEC1/AN1/CN3/RB1
K2	PGED1/AN0/CN2/RB0
K3	VREF+/CVREF+/PMA6/RA10

PIC32MX3XX/4XX

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PIC32MX3XX/4XX

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number ⁽¹⁾			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
PMD0	60	93	A4	I/O	TTL/ST	Parallel Master Port Data (De-multiplexed Master mode) or Address/Data (Multiplexed Master modes).
PMD1	61	94	B4	I/O	TTL/ST	
PMD2	62	98	B3	I/O	TTL/ST	
PMD3	63	99	A2	I/O	TTL/ST	
PMD4	64	100	A1	I/O	TTL/ST	
PMD5	1	3	D3	I/O	TTL/ST	
PMD6	2	4	C1	I/O	TTL/ST	
PMD7	3	5	D2	I/O	TTL/ST	
PMD8	—	90	A5	I/O	TTL/ST	
PMD9	—	89	E6	I/O	TTL/ST	
PMD10	—	88	A6	I/O	TTL/ST	
PMD11	—	87	B6	I/O	TTL/ST	
PMD12	—	79	A9	I/O	TTL/ST	
PMD13	—	80	D8	I/O	TTL/ST	
PMD14	—	83	D7	I/O	TTL/ST	
PMD15	—	84	C7	I/O	TTL/ST	
PMRD	53	82	B8	O	—	Parallel Master Port Read Strobe.
PMWR	52	81	C8	O	—	Parallel Master Port Write Strobe.
PMALL	30	44	L8	O	—	Parallel Master Port Address Latch Enable low-byte (Multiplexed Master modes).
PMALH	29	43	K7	O	—	Parallel Master Port Address Latch Enable high-byte (Multiplexed Master modes).
VBUS	34	54	H8	I	Analog	USB Bus Power Monitor.
VUSB	35	55	H9	P	—	USB Internal Transceiver Supply. If the USB module is <i>not</i> used, this pin must be connected to VDD.
VBUSON	11	20	H1	O	—	USB Host and OTG Bus Power Control Output.
D+	37	57	H10	I/O	Analog	USB D+.
D-	36	56	J11	I/O	Analog	USB D-.
USBID	33	51	K10	I	ST	USB OTG ID Detect.
ENVREG	57	86	A7	I	ST	Enable for On-Chip Voltage Regulator.
TRCLK	—	91	C5	O	—	Trace Clock.
TRD0	—	97	A3	O	—	Trace Data Bits 0-3.
TRD1	—	96	C3	O	—	
TRD2	—	95	C4	O	—	
TRD3	—	92	B5	O	—	
PGED1	16	25	K2	I/O	ST	Data I/O pin for programming/debugging communication channel 1.
PGEC1	15	24	K1	I	ST	Clock input pin for programming/debugging communication channel 1.

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer

Analog = Analog input
O = Output

P = Power
I = Input

Note 1: Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

3.2 Architecture Overview

The MIPS32[®] M4K[®] Processor Core contains several logic blocks working together in parallel, providing an efficient high performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CPO)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e Support
- Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The MIPS32[®] M4K[®] Processor Core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit general purpose registers used for integer operations and address calculation. One additional register file shadow set (containing thirty-two registers) is added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid stalls when executing instructions streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the CLZ and CLO instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- Shifter and Store Aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The MIPS32[®] M4K[®] Processor Core includes a multiply/divide unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the integer unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32MX core only checks the value of the latter (*rt*) operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit-wide *rs*, 15 iterations are skipped, and for a 24-bit-wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32MX core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

FIGURE 4-4: MEMORY MAP ON RESET FOR PIC32MX340F128H, PIC32MX340F128L, PIC32MX440F128H AND PIC32MX440F128L DEVICES⁽¹⁾

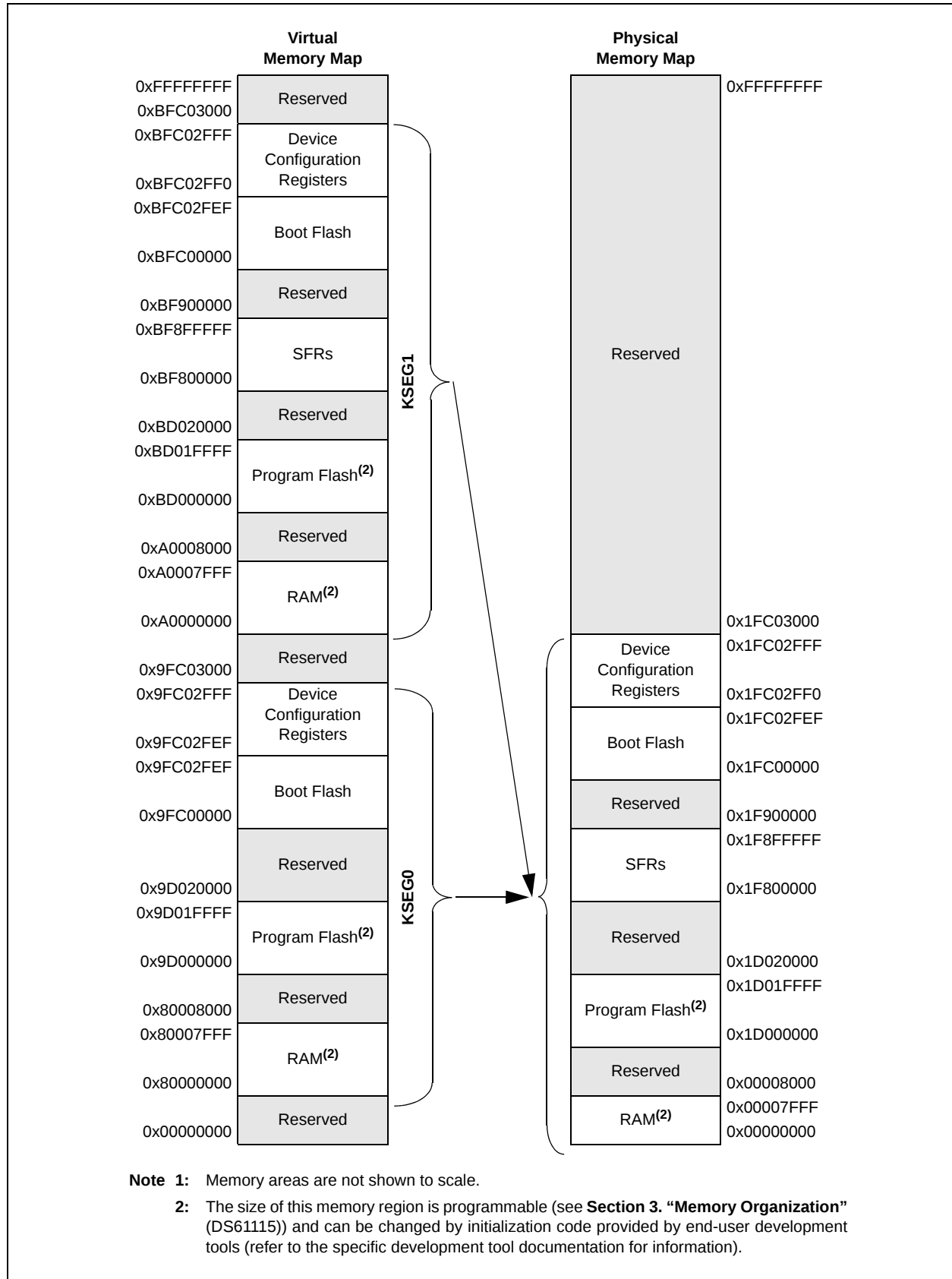


TABLE 4-7: TIMER1-5 REGISTERS MAP⁽¹⁾

Virtual Address (BF80-#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	T1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	TWDIS	TWIP	—	—	—	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—	0000
0610	TMR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR1<15:0>																0000
0620	PR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR1<15:0>																FFFF
0800	T2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>		—	T32	—	TCS ⁽²⁾	—	0000
0810	TMR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR2<15:0>																0000
0820	PR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR2<15:0>																FFFF
0A00	T3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>		—	—	—	TCS ⁽²⁾	—	0000
0A10	TMR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR3<15:0>																0000
0A20	PR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR3<15:0>																FFFF
0C00	T4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>		—	T32	—	TCS ⁽²⁾	—	0000
0C10	TMR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR4<15:0>																0000
0C20	PR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR4<15:0>																FFFF
0E00	T5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>		—	—	—	TCS ⁽²⁾	—	0000
0E10	TMR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR5<15:0>																0000
0E20	PR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR5<15:0>																FFFF

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
- 2:** This bit is not available on 64-pin devices.

TABLE 4-14: DMA GLOBAL REGISTERS MAP FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	DMACON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	SUSPEND	—	—	—	—	—	—	—	—	—	—	—	—	0000
3010	DMASTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RDWR	—	DMACH<1:0>	—	0000
3020	DMAADDR	31:16	DMAADDR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 4-15: DMA CRC REGISTERS MAP FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY⁽¹⁾

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3030	DCRCCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	PLEN<3:0>				CRCEN	CRCAPP	—	—	—	—	CRCCH<1:0>		0000
3040	DCRCDATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DCRCDATA<15:0>																0000
3050	DCRCXOR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DCRCXOR<15:0>																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 4-16: DMA CHANNELS 0-3 REGISTERS MAP FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY⁽¹⁾

Virtual Address (BF88-#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3060	DCH0CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	0000	
3070	DCH0ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>							00FF	
		15:0	CHSIRQ<7:0>							CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00	
3080	DCH0INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3090	DCH0SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
30A0	DCH0DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
30B0	DCH0SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHSSIZ<7:0>							0000	
30C0	DCH0DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHDSIZ<7:0>							0000	
30D0	DCH0SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHSTR<7:0>							0000	
30E0	DCH0DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHDPTR<7:0>							0000	
30F0	DCH0CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHCSIZ<7:0>							0000	
3100	DCH0CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHCPTR<7:0>							0000	
3110	DCH0DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>							0000	
3120	DCH1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	0000
3130	DCH1ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>							00FF	
		15:0	CHSIRQ<7:0>							CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00	
3140	DCH1INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3150	DCH1SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers except DCHxSPTR, DCHxDPTR and DCHxCPTR have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-23: PORTC REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L, PIC32MX360F512L, PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY⁽¹⁾

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6080	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	TRISC4	TRISC3	TRISC2	TRISC1	—	F01E
6090	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	RC4	RC3	RC2	RC1	—	xxxx
60A0	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	LATC4	LATC3	LATC2	LATC1	—	xxxx
60B0	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	ODCC4	ODCC3	ODCC2	ODCC1	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 4-24: PORTC REGISTERS MAP FOR PIC32MX320F032H, PIC32MX320F064H, PIC32MX320F128H, PIC32MX340F128H, PIC32MX340F256H, PIC32MX340F512H, PIC32MX420F032H, PIC32MX440F128H, PIC32MX440F256H AND PIC32MX440F512H DEVICES ONLY⁽¹⁾

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6080	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	—	—	—	—	—	F000
6090	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
60A0	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
60B0	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 4-43: USB REGISTERS MAP⁽¹⁾

Virtual Address (BF88-#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5040	U1OTG IR ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF	0000
5050	U1OTG IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE	0000
5060	U1OTG STAT ⁽³⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD	0000
5070	U1OTG CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
5080	U1PWRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UACTPND ⁽⁴⁾	—	—	USLPGRD	—	—	USUSPEND	USBPWR	0000
5200	U1IR ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF DETACHIF	0000 0000
5210	U1IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE DETACHIE	0000 0000
5220	U1EIR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF EOFEF	PIDEF	0000 0000
5230	U1EIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE EOFEE	PIDEE	0000 0000
5240	U1STAT ⁽³⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ENDPT<3:0> ⁽⁴⁾				DIR	PPBI	—	—	0000
5250	U1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	JSTATE ⁽⁴⁾	SE0 ⁽⁴⁾	PKTDIS TOKBUSY	USBRST	HOSTEN	RESUME	PPBRST	USBEN SOFEN	0000 0000
5260	U1ADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPDEN	DEVADDR<6:0>							0000
5270	U1BDTP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRL<7:1>							—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
- 2:** This register does not have associated CLR, SET, and INV registers.
- 3:** All bits in this register are read-only; therefore, CLR, SET, and INV registers are not supported.
- 4:** The reset value for this bit is undefined.

13.0 TIMER1

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. “Timers”** (DS61105) of the “*PIC32 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

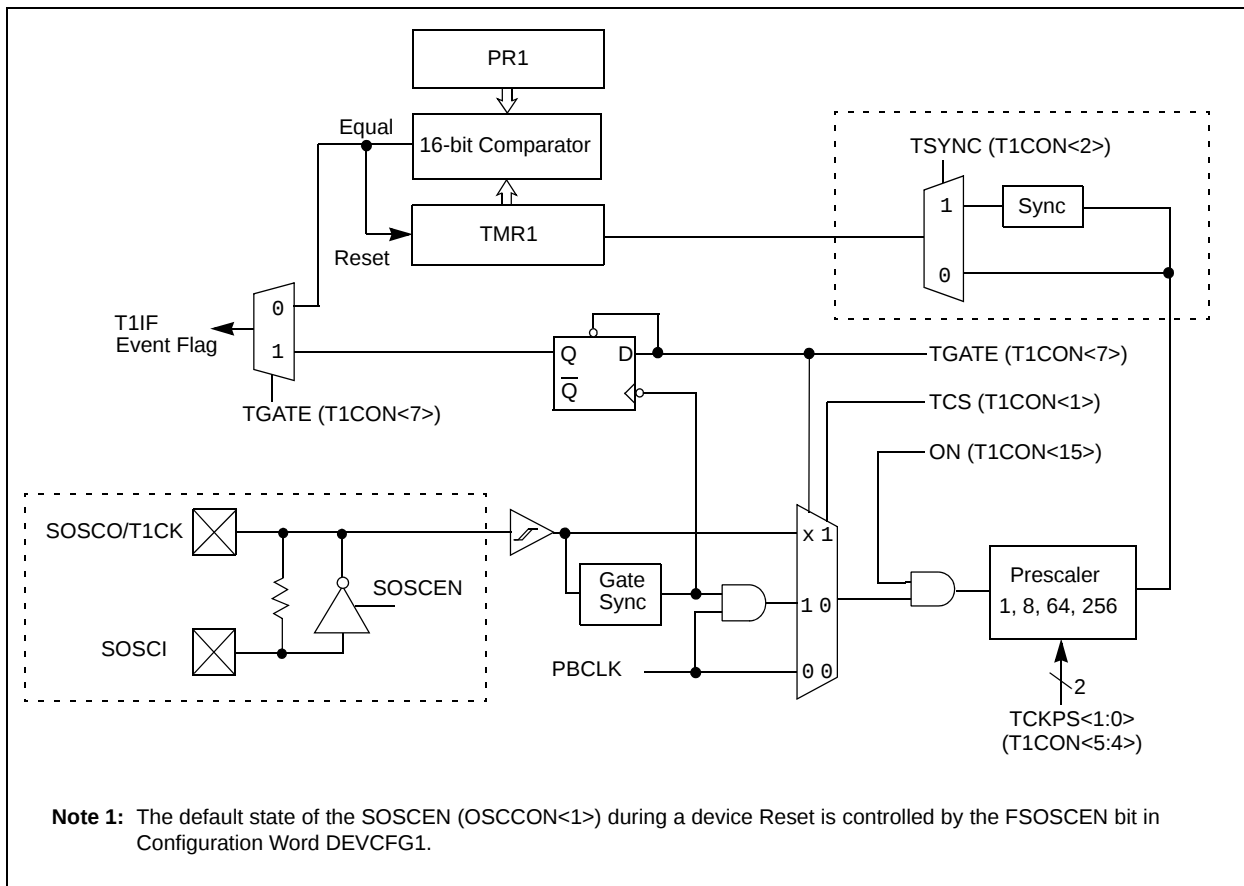
This family of PIC32MX devices features one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the Secondary Oscillator (Sosc) for real-time clock applications. The following modes are supported:

- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

13.1 Additional Supported Features

- Selectable clock prescaler
- Timer operation during CPU Idle and Sleep mode
- Fast bit manipulation using CLR, SET and INV registers
- Asynchronous mode can be used with the Sosc to function as a Real-Time Clock (RTC)

FIGURE 13-1: TIMER1 BLOCK DIAGRAM⁽¹⁾



15.0 INPUT CAPTURE

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. “Input Capture”** (DS61122) of the “*PIC32 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement. The PIC32MX3XX/4XX devices support up to five input capture channels.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The events that cause a capture event are listed below in three categories:

1. Simple Capture Event modes
 - Capture timer value on every falling edge of input at ICx pin
 - Capture timer value on every rising edge of input at ICx pin

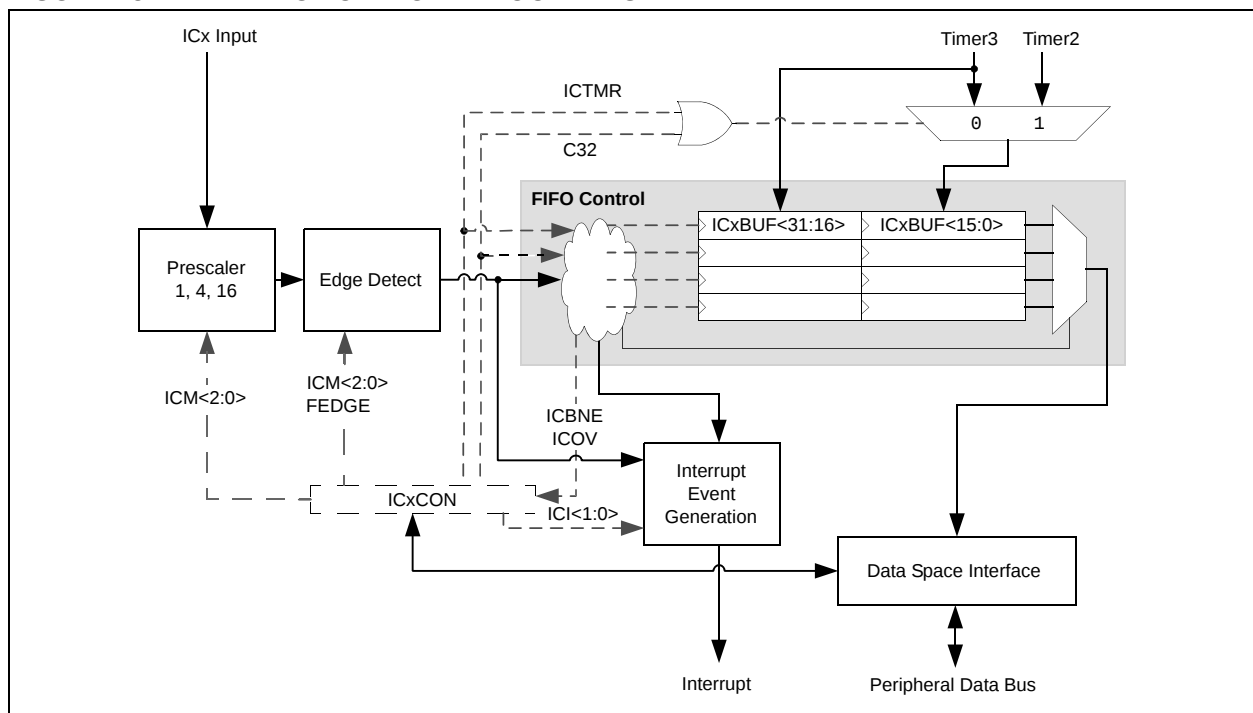
2. Capture timer value on every edge (rising and falling)
3. Capture timer value on every edge (rising and falling), specified edge first.
4. Prescaler Capture Event modes
 - Capture timer value on every 4th rising edge of input at ICx pin
 - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during CPU Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values
 - Interrupt optionally generated after 1, 2, 3 or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

FIGURE 15-1: INPUT CAPTURE BLOCK DIAGRAM



PIC32MX3XX/4XX

NOTES:

26.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. “Watchdog Timer and Power-up Timer”** (DS61114), **Section 32. “Configuration”** (DS61124) and **Section 33. “Programming and Diagnostics”** (DS61129) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX3XX/4XX devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. These are:

- Flexible Device Configuration
- Watchdog Timer
- JTAG Interface
- In-Circuit Serial Programming™ (ICSP™)

26.1 Configuration Bits

The Configuration bits can be programmed to select various device configurations.

REGISTER 26-1: DEVCFG0: DEVICE CONFIGURATION WORD 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-0	r-1	r-1	R/P	r-1	r-1	r-1	R/P
	—	—	—	CP	—	—	—	BWP
23:16	r-1	r-1	r-1	r-1	R/P	R/P	R/P	R/P
	—	—	—	—	PWP<7:4>			
15:8	R/P	R/P	R/P	R/P	r-1	r-1	r-1	r-1
	PWP<3:0>				—	—	—	—
7:0	r-1	r-1	r-1	r-1	R/P	r-1	R/P	R/P
	—	—	—	—	ICESEL	—	DEBUG<1:0>	

Legend:

R = Readable bit W = Writable bit P = Programmable bit r = Reserved bit
U = Unimplemented bit -n = Bit Value at POR: ('0', '1', x = Unknown)

bit 31 **Reserved:** Write '0'

bit 30-29 **Reserved:** Write '1'

bit 28 **CP:** Code-Protect bit

Prevents boot and program Flash memory from being read or modified by an external programming device.

1 = Protection disabled

0 = Protection enabled

bit 27-25 **Reserved:** Write '1'

bit 24 **BWP:** Boot Flash Write-Protect bit

Prevents boot Flash memory from being modified during code execution.

1 = Boot Flash is writable

0 = Boot Flash is not writable

bit 23-20 **Reserved:** Write '1'

PIC32MX3XX/4XX

TABLE 29-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD}) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp			
Parameter No.	Typical ⁽²⁾	Max.	Units	Conditions		
Module Differential Current (Continued)						
DC43	—	1100	μA	-40°C	2.5V	ADC: ΔIADC (Notes 3, 4, 6)
DC43a	—	1100	μA	+25°C		
DC43b	—	1000	μA	+85°C		
DC43h	—	1200	μA	+105°C		
DC43c	880	—	μA	—	—	ADC: ΔIADC (Notes 3, 4)
DC43e	—	1100	μA	-40°C	3.6V	ADC: ΔIADC (Notes 3, 4)
DC43f	—	1100	μA	+25°C		
DC43g	—	1000	μA	+85°C		
DC43i	—	1200	μA	+105°C		

- Note 1:** Base I_{PD} is measured with all digital peripheral modules disabled. All I/Os are configured as inputs and pulled low. WDT and FSCM are disabled.
- 2:** Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.
- 4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.
- 5:** Data is characterized at +70°C and not tested. Parameter is for design guidance only.
- 6:** This parameter is characterized, but not tested in manufacturing.

TABLE 29-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
DI10	V _{IL}	Input Low Voltage I/O pins: with TTL Buffer	V _{SS}	—	0.15 V _{DD}	V	(Note 4)
		with Schmitt Trigger Buffer	V _{SS}	—	0.2 V _{DD}	V	(Note 4)
DI15		$\overline{\text{MCLR}}$	V _{SS}	—	0.2 V _{DD}	V	(Note 4)
DI16		OSC1 (XT mode)	V _{SS}	—	0.2 V _{DD}	V	(Note 4)
DI17		OSC1 (HS mode)	V _{SS}	—	0.2 V _{DD}	V	(Note 4)
DI18		SDAx, SCLx	V _{SS}	—	0.3 V _{DD}	V	SMBus disabled (Note 4)
DI19		SDAx, SCLx	V _{SS}	—	0.8	V	SMBus enabled (Note 4)
DI20	V _{IH}	Input High Voltage I/O pins: with Analog Functions	0.8 V _{DD}	—	V _{DD}	V	(Note 4)
		Digital Only	0.8 V _{DD}	—		V	(Note 4)
		with TTL Buffer	0.25V _{DD} + 0.8V	—	5.5	V	(Note 4)
		with Schmitt Trigger Buffer	0.8 V _{DD}	—	5.5	V	(Note 4)
DI25		$\overline{\text{MCLR}}$	0.8 V _{DD}	—	V _{DD}	V	(Note 4)
DI26		OSC1 (XT mode)	0.7 V _{DD}	—	V _{DD}	V	(Note 4)
DI27		OSC1 (HS mode)	0.7 V _{DD}	—	V _{DD}	V	(Note 4)
DI28		SDAx, SCLx	0.7 V _{DD}	—	5.5	V	SMBus disabled (Note 4)
DI29		SDAx, SCLx	2.1	—	5.5	V	SMBus enabled, 2.3V $\leq$ V _{PIN} $\leq$ 5.5 (Note 4)
DI30	ICNPU	CNxx Pull up Current	50	250	400	μA	V _{DD} = 3.3V, V _{PIN} = V _{SS}
DI50	I _{IL}	Input Leakage Current I/O Ports	—	—	±1	μA	(Note 3) V _{SS} $\leq$ V _{PIN} $\leq$ V _{DD} , Pin at high-impedance
DI51		Analog Input Pins	—	—	±1	μA	V _{SS} $\leq$ V _{PIN} $\leq$ V _{DD} , Pin at high-impedance
DI55		$\overline{\text{MCLR}}$	—	—	±1	μA	V _{SS} $\leq$ V _{PIN} $\leq$ V _{DD}
DI56		OSC1	—	—	±1	μA	V _{SS} $\leq$ V _{PIN} $\leq$ V _{DD} , XT and HS modes

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: This parameter is characterized, but not tested in manufacturing.

FIGURE 29-6: TIMER1, 2, 3, 4, 5 EXTERNAL CLOCK TIMING CHARACTERISTICS

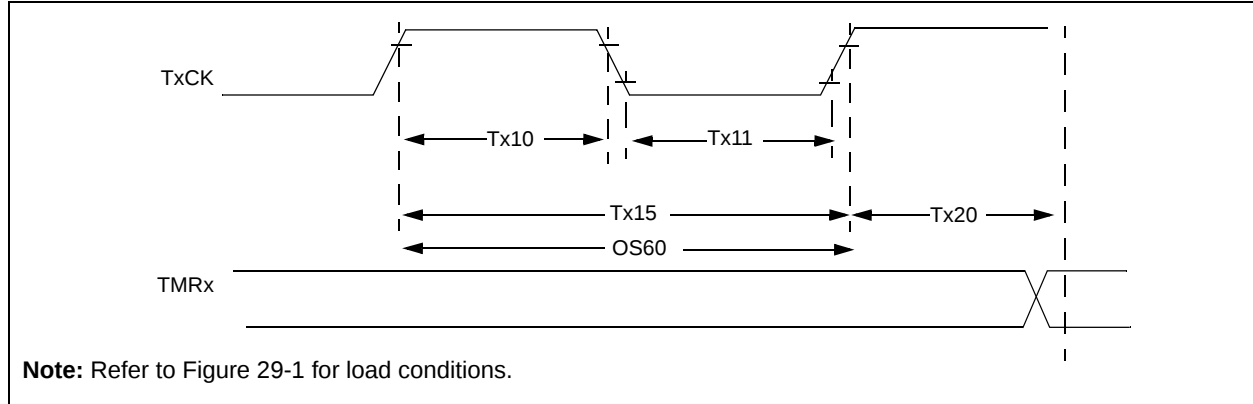


TABLE 29-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS⁽¹⁾

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	Symbol	Characteristics ⁽²⁾		Min.	Typical	Max.	Units	Conditions
TA10	TtxH	TxCK High Time	Synchronous, with prescaler	[(12.5 ns or 1TPB)/N] + 25 ns	—	—	ns	Must also meet parameter TA15.
			Asynchronous, with prescaler	10	—	—	ns	—
TA11	TtxL	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1TPB)/N] + 25 ns	—	—	ns	Must also meet parameter TA15.
			Asynchronous, with prescaler	10	—	—	ns	—
TA15	TtxP	TxCK Input Period	Synchronous, with prescaler	[(Greater of 25 ns or 2TPB)/N] + 30 ns	—	—	ns	VDD > 2.7V
				[(Greater of 25 ns or 2TPB)/N] + 50 ns	—	—	ns	VDD < 2.7V
			Asynchronous, with prescaler	20	—	—	ns	VDD > 2.7V (Note 3)
				50	—	—	ns	VDD < 2.7V (Note 3)
OS60	Ft1	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting TCS bit (T1CON<1>))		32	—	100	kHz	—
TA20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—		1	TPB	—

Note 1: Timer1 is a Type A.

2: This parameter is characterized, but not tested in manufacturing.

3: N = prescale value (1, 8, 64, 256)

PIC32MX3XX/4XX

FIGURE 29-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS

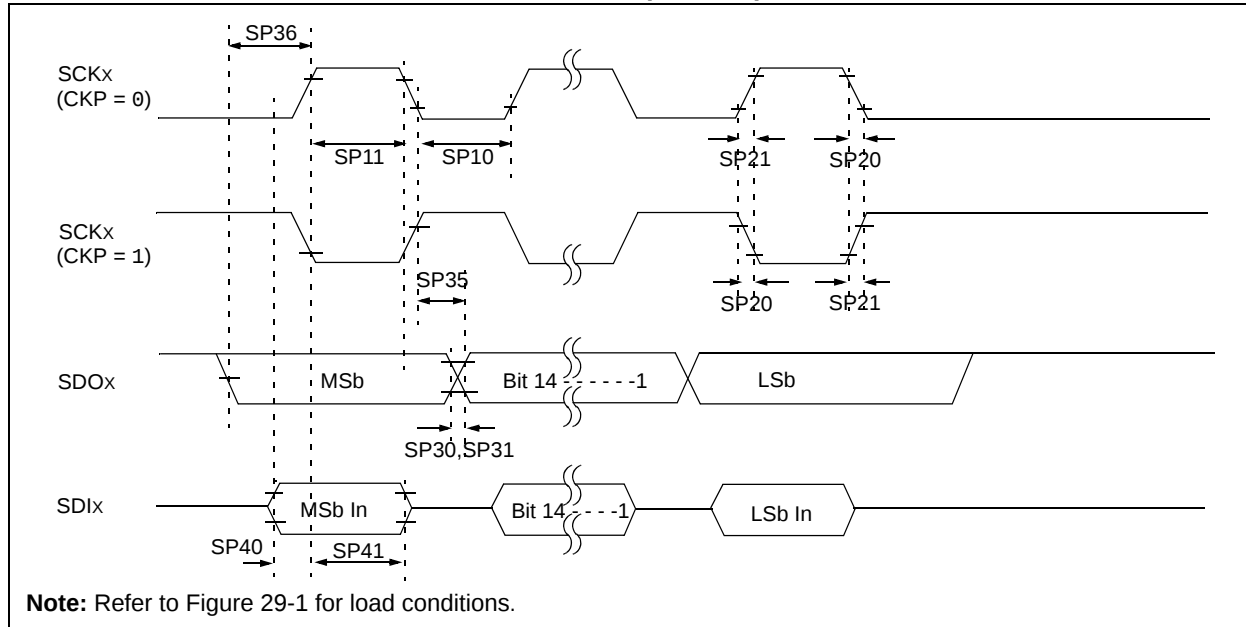


TABLE 29-29: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SP10	TsCL	SCKx Output Low Time ⁽³⁾	Tsck/2	—	—	ns	—
SP11	TsCH	SCKx Output High Time ⁽³⁾	Tsck/2	—	—	ns	—
SP20	TscF	SCKx Output Fall Time ⁽⁴⁾	—	—	—	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time ⁽⁴⁾	—	—	—	ns	See parameter DO31
SP30	TdOF	SDOx Data Output Fall Time ⁽⁴⁾	—	—	—	ns	See parameter DO32
SP31	TdOR	SDOx Data Output Rise Time ⁽⁴⁾	—	—	—	ns	See parameter DO31
SP35	TsCH2doV, TsCL2doV	SDOx Data Output Valid after SCKx Edge	—	—	15	ns	VDD > 2.7V
			—	—	20	ns	VDD < 2.7V
SP36	TdoV2sc, TdoV2sCL	SDOx Data Output Setup to First SCKx Edge	15	—	—	ns	—
SP40	TdiV2sCH, TdiV2sCL	Setup Time of SDIx Data Input to SCKx Edge	15	—	—	ns	VDD > 2.7V
			20	—	—	ns	VDD < 2.7V
SP41	TsCH2diL, TsCL2diL	Hold Time of SDIx Data Input to SCKx Edge	15	—	—	ns	VDD > 2.7V
			20	—	—	ns	VDD < 2.7V

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.