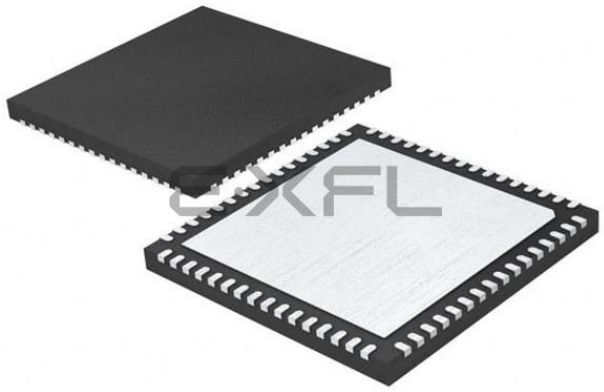
# Microchip Technology - PIC32MX320F064H-40V/MR Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 40MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 53 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-VQFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx320f064h-40v-mr |

# PIC32MX3XX/4XX

## High-Performance, General Purpose and USB 32-bit Flash Microcontrollers

### High-Performance 32-bit RISC CPU:

- MIPS32® M4K® 32-bit core with 5-stage pipeline
- 80 MHz maximum frequency
- 1.56 DMIPS/MHz (Dhrystone 2.1) performance at 0 wait state Flash access
- Single-cycle multiply and high-performance divide unit
- MIPS16e® mode for up to 40% smaller code size
- Two sets of 32 core register files (32-bit) to reduce interrupt latency
- Prefetch Cache module to speed execution from Flash

### Microcontroller Features:

- Operating temperature range of -40ºC to +105ºC
- Operating voltage range of 2.3V to 3.6V
- 32K to 512K Flash memory (plus an additional 12 KB of boot Flash)
- 8K to 32K SRAM memory
- Pin-compatible with most PIC24/dsPIC® DSC devices
- Multiple power management modes
- Multiple interrupt vectors with individually programmable priority
- Fail-Safe Clock Monitor Mode
- Configurable Watchdog Timer with on-chip Low-Power RC Oscillator for reliable operation

### Peripheral Features:

- Atomic SET, CLEAR and INVERT operation on select peripheral registers
- Up to 4-channel hardware DMA with automatic data size detection
- USB 2.0-compliant full-speed device and On-The-Go (OTG) controller
- USB has a dedicated DMA channel
- 3 MHz to 25 MHz crystal oscillator
- Internal 8 MHz and 32 kHz oscillators
- Separate PLLs for CPU and USB clocks
- Two $I^2C$™ modules
- Two UART modules with:
  - RS-232, RS-485 and LIN support
  - IrDA® with on-chip hardware encoder and decoder
- Up to two SPI modules
- Parallel Master and Slave Port (PMP/PSP) with 8-bit and 16-bit data and up to 16 address lines
- Hardware Real-Time Clock and Calendar (RTCC)
- Five 16-bit Timers/Counters (two 16-bit pairs combine to create two 32-bit timers)
- Five capture inputs
- Five compare/PWM outputs
- Five external interrupt pins
- High-Speed I/O pins capable of toggling at up to 80 MHz
- High-current sink/source (18 mA/18 mA) on all I/O pins
- Configurable open-drain output on digital I/O pins

### Debug Features:

- Two programming and debugging Interfaces:
  - 2-wire interface with unintrusive access and real-time data exchange with application
  - 4-wire MIPS® standard enhanced JTAG interface
- Unintrusive hardware-based instruction trace
- IEEE Standard 1149.2-compatible (JTAG) boundary scan

### Analog Features:

- Up to 16-channel 10-bit Analog-to-Digital Converter:
  - 1000 ksps conversion rate
  - Conversion available during Sleep, Idle
- Two Analog Comparators

**TABLE 1: PIC32MX GENERAL PURPOSE – FEATURES**

| General Purpose | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Device | Pins | Packages(2) | MHz | Program Memory (KB) | Data Memory (KB) | Timers/Capture/Compare | Programmable DMA Channels | VREG | Trace | EUART/SPI/I²C™ | 10-bit ADC (ch) | Comparators | PMP/PSP | JTAG |
| PIC32MX320F032H | 64 | PT, MR | 40 | 32 + 12(1) | 8 | 5/5/5 | 0 | Yes | No | 2/2/2 | 16 | 2 | Yes | Yes |
| PIC32MX320F064H | 64 | PT, MR | 80 | 64 + 12(1) | 16 | 5/5/5 | 0 | Yes | No | 2/2/2 | 16 | 2 | Yes | Yes |
| PIC32MX320F128H | 64 | PT, MR | 80 | 128 + 12(1) | 16 | 5/5/5 | 0 | Yes | No | 2/2/2 | 16 | 2 | Yes | Yes |
| PIC32MX340F128H | 64 | PT, MR | 80 | 128 + 12(1) | 32 | 5/5/5 | 4 | Yes | No | 2/2/2 | 16 | 2 | Yes | Yes |
| PIC32MX340F256H | 64 | PT, MR | 80 | 256 + 12(1) | 32 | 5/5/5 | 4 | Yes | No | 2/2/2 | 16 | 2 | Yes | Yes |
| PIC32MX340F512H | 64 | PT, MR | 80 | 512 + 12(1) | 32 | 5/5/5 | 4 | Yes | No | 2/2/2 | 16 | 2 | Yes | Yes |
| PIC32MX320F128L | 100 | PT | 80 | 128 + 12(1) | 16 | 5/5/5 | 0 | Yes | No | 2/2/2 | 16 | 2 | Yes | Yes |
| | 121 | BG | | | | | | | | | | | | |
| PIC32MX340F128L | 100 | PT | 80 | 128 + 12(1) | 32 | 5/5/5 | 4 | Yes | No | 2/2/2 | 16 | 2 | Yes | Yes |
| | 121 | BG | | | | | | | | | | | | |
| PIC32MX360F256L | 100 | PT | 80 | 256 + 12(1) | 32 | 5/5/5 | 4 | Yes | Yes | 2/2/2 | 16 | 2 | Yes | Yes |
| | 121 | BG | | | | | | | | | | | | |
| PIC32MX360F512L | 100 | PT | 80 | 512 + 12(1) | 32 | 5/5/5 | 4 | Yes | Yes | 2/2/2 | 16 | 2 | Yes | Yes |
| | 121 | BG | | | | | | | | | | | | |

**Legend:** PT = TQFP MR = QFN BG = XBGA

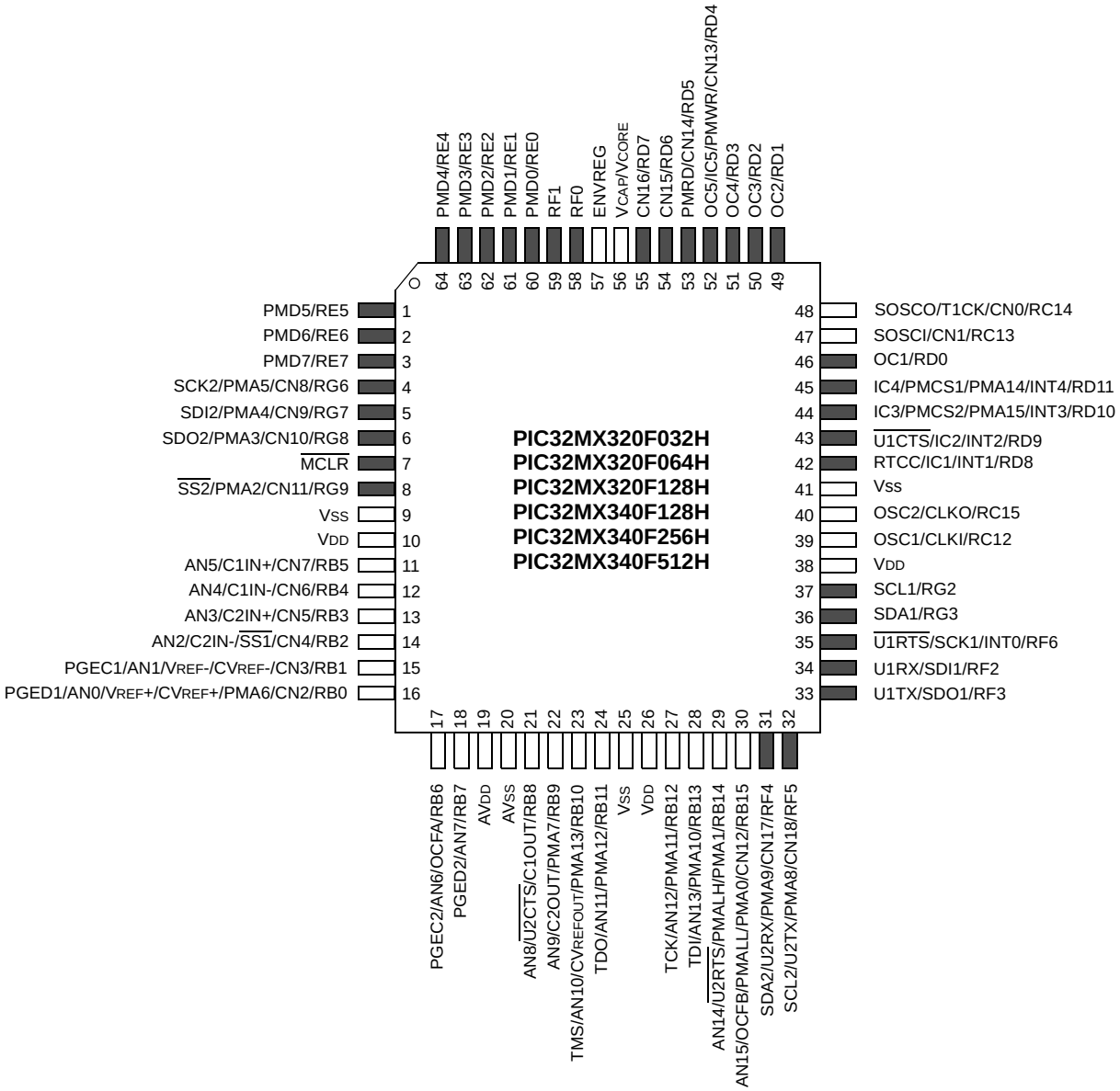
**Note 1:** This device features 12 KB Boot Flash memory.

**2:** See Legend for an explanation of the acronyms. See **Section 30.0 "Packaging Information"** for details.

## Pin Diagrams (Continued)

**64-Pin TQFP (General Purpose)**

= Pins are up to 5V tolerant



## Pin Diagrams (Continued)

**64-Pin TQFP (USB)**

= Pins are up to 5V tolerant

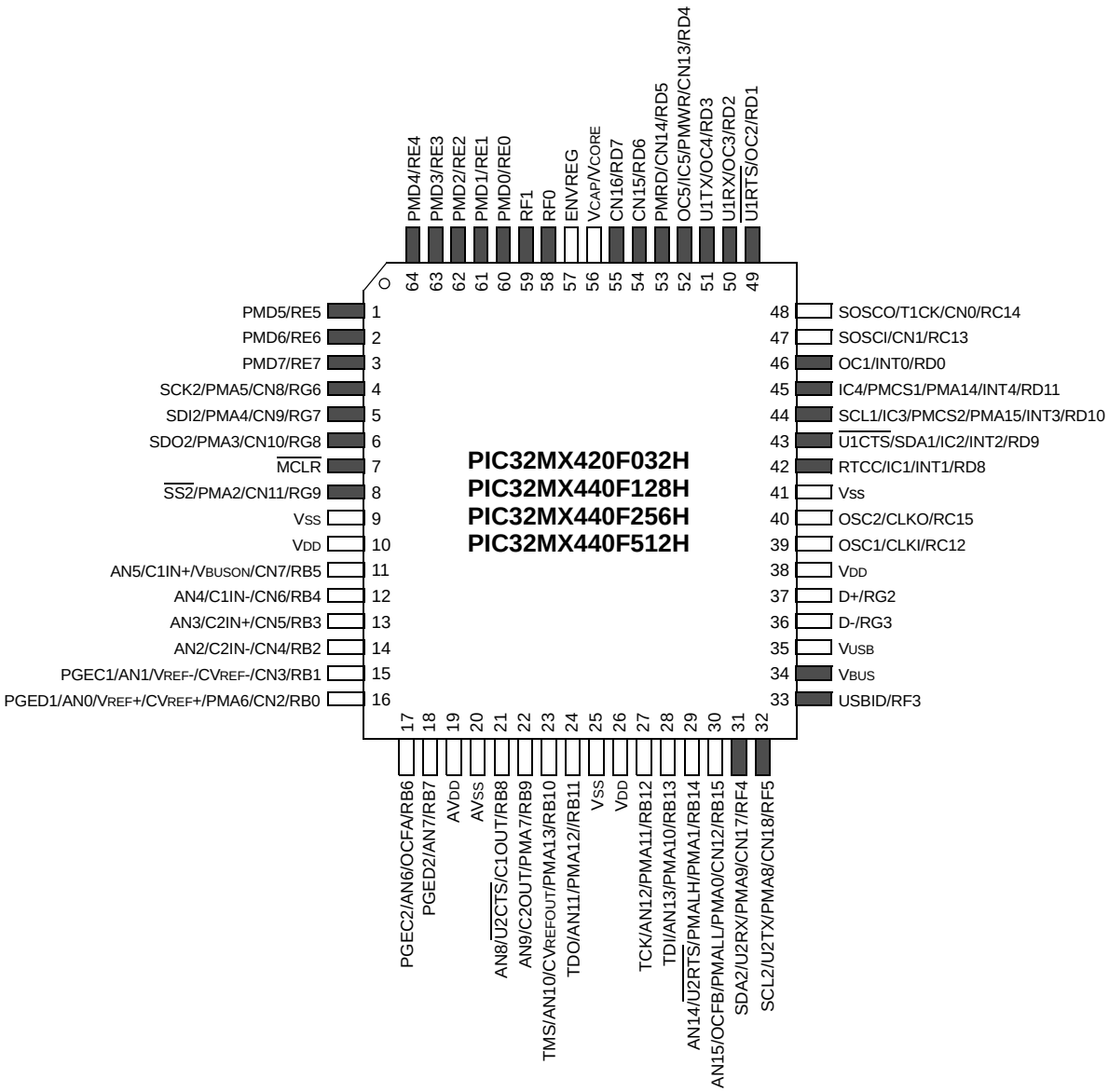
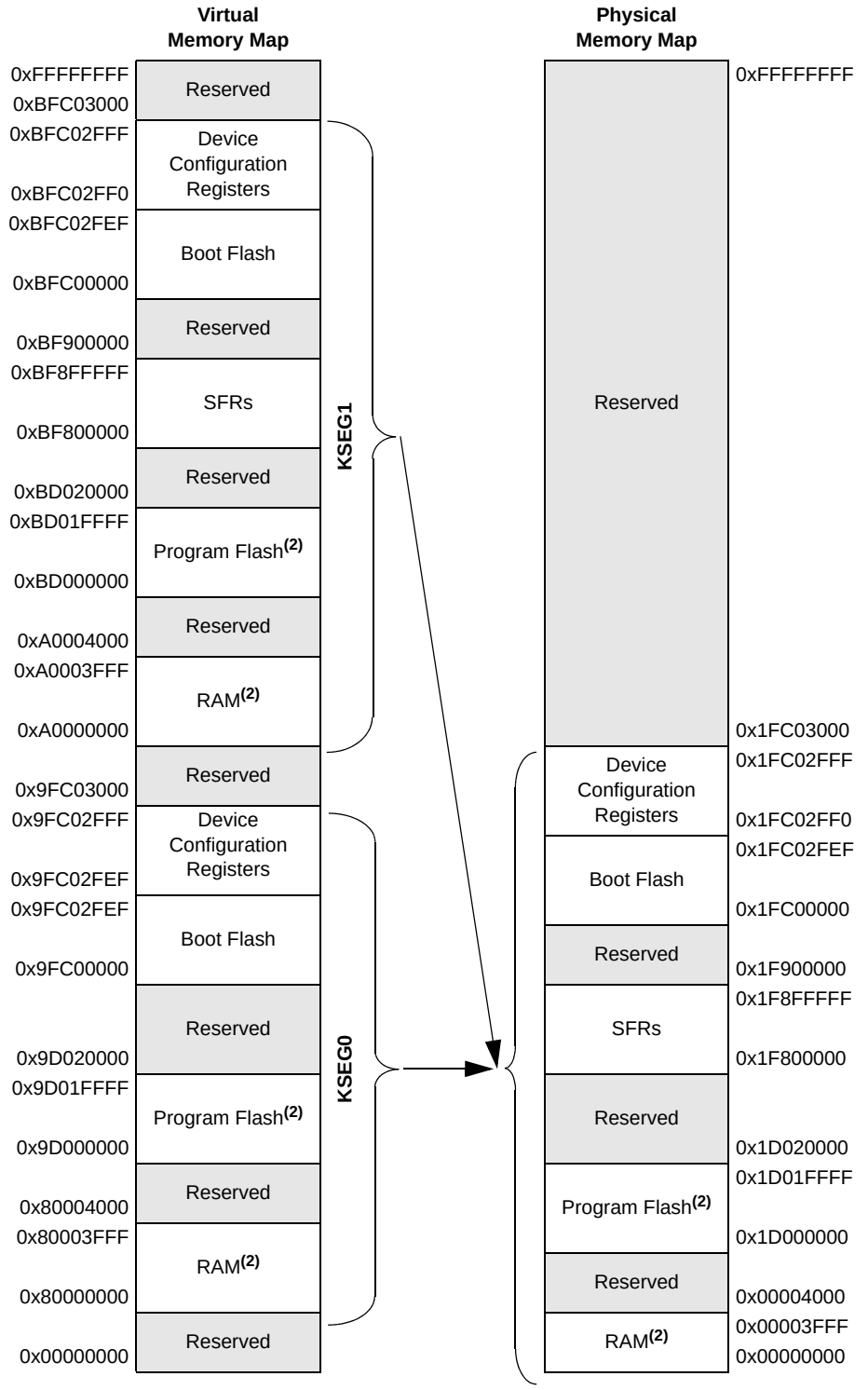


**FIGURE 4-3: MEMORY MAP ON RESET FOR PIC32MX320F128H AND PIC32MX320F128L DEVICES(1)**




**Note 1:** Memory areas are not shown to scale.

**2:** The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS61115)) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

**TABLE 4-3: INTERRUPT REGISTERS MAP FOR PIC32MX340F128H, PIC32MX340F256H, PIC32MX340F512H, PIC32MX340F128L, PIC32MX360F256L AND PIC32MX360F512L DEVICES ONLY(1)**

| Virtual Address (BF88_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 1000 | INTCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SS0 | 0000 |
| | | 15:0 | — | — | — | MVEC | — | TPC<2:0> | | | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 0000 |
| 1010 | INTSTAT(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | SRIPL<2:0> | | | — | — | VEC<5:0> | | | | | | 0000 |
| 1020 | IPTMR | 31:16 | IPTMR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 1030 | IFS0 | 31:16 | I2C1MIF | I2C1SIF | I2C1BIF | U1TXIF | U1RXIF | U1EIF | SPI1RXIF | SPI1TXIF | SPI1EIF | OC5IF | IC5IF | T5IF | INT4IF | OC4IF | IC4IF | T4IF | 0000 |
| | | 15:0 | INT3IF | OC3IF | IC3IF | T3IF | INT2IF | OC2IF | IC2IF | T2IF | INT1IF | OC1IF | IC1IF | T1IF | INT0IF | CS1IF | CS0IF | CTIF | 0000 |
| 1040 | IFS1 | 31:16 | — | — | — | — | — | — | — | FCEIF | — | — | — | — | DMA3IF | DMA2IF | DMA1IF | DMA0IF | 0000 |
| | | 15:0 | RTCCIF | FSCMIF | I2C2MIF | I2C2SIF | I2C2BIF | U2TXIF | U2RXIF | U2EIF | SPI2RXIF | SPI2TXIF | SPI2EIF | CMP2IF | CMP1IF | PMPIF | AD1IF | CNIF | 0000 |
| 1060 | IEC0 | 31:16 | I2C1MIE | I2C1SIE | I2C1BIE | U1TXIE | U1RXIE | U1EIE | SPI1RXIE | SPI1TXIE | SPI1EIE | OC5IE | IC5IE | T5IE | INT4IE | OC4IE | IC4IE | T4IE | 0000 |
| | | 15:0 | INT3IE | OC3IE | IC3IE | T3IE | INT2IE | OC2IE | IC2IE | T2IE | INT1IE | OC1IE | IC1IE | T1IE | INT0IE | CS1IE | CS0IE | CTIE | 0000 |
| 1070 | IEC1 | 31:16 | — | — | — | — | — | — | — | FCEIE | — | — | — | — | DMA3IE | DMA2IE | DMA1IE | DMA0IE | 0000 |
| | | 15:0 | RTCCIE | FSCMIE | I2C2MIE | — | — | — | — | — | SPI2RXIE | SPI2TXIE | SPI2EIE | CMP2IE | CMP1IE | PMPIE | AD1IE | CNIE | 0000 |
| 1090 | IPC0 | 31:16 | — | — | — | INT0IP<2:0> | | | INT0IS<1:0> | | — | — | — | CS1IP<2:0> | | | CS1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CS0IP<2:0> | | | CS0IS<1:0> | | — | — | — | CTIP<2:0> | | | CTIS<1:0> | | 0000 |
| 10A0 | IPC1 | 31:16 | — | — | — | INT1IP<2:0> | | | INT1IS<1:0> | | — | — | — | OC1IP<2:0> | | | OC1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC1IP<2:0> | | | IC1IS<1:0> | | — | — | — | T1IP<2:0> | | | T1IS<1:0> | | 0000 |
| 10B0 | IPC2 | 31:16 | — | — | — | INT2IP<2:0> | | | INT2IS<1:0> | | — | — | — | OC2IP<2:0> | | | OC2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC2IP<2:0> | | | IC2IS<1:0> | | — | — | — | T2IP<2:0> | | | T2IS<1:0> | | 0000 |
| 10C0 | IPC3 | 31:16 | — | — | — | INT3IP<2:0> | | | INT3IS<1:0> | | — | — | — | OC3IP<2:0> | | | OC3IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC3IP<2:0> | | | IC3IS<1:0> | | — | — | — | T3IP<2:0> | | | T3IS<1:0> | | 0000 |
| 10D0 | IPC4 | 31:16 | — | — | — | INT4IP<2:0> | | | INT4IS<1:0> | | — | — | — | OC4IP<2:0> | | | OC4IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC4IP<2:0> | | | IC4IS<1:0> | | — | — | — | T4IP<2:0> | | | T4IS<1:0> | | 0000 |
| 10E0 | IPC5 | 31:16 | — | — | — | SPI1IP<2:0> | | | SPI1IS<1:0> | | — | — | — | OC5IP<2:0> | | | OC5IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC5IP<2:0> | | | IC5IS<1:0> | | — | — | — | T5IP<2:0> | | | T5IS<1:0> | | 0000 |
| 10F0 | IPC6 | 31:16 | — | — | — | AD1IP<2:0> | | | AD1IS<1:0> | | — | — | — | CNIP<2:0> | | | CNIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | I2C1IP<2:0> | | | I2C1IS<1:0> | | — | — | — | U1IP<2:0> | | | U1IS<1:0> | | 0000 |
| 1100 | IPC7 | 31:16 | — | — | — | SPI2IP<2:0> | | | SPI2IS<1:0> | | — | — | — | CMP2IP<2:0> | | | CMP2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CMP1IP<2:0> | | | CMP1IS<1:0> | | — | — | — | PMPIP<2:0> | | | PMPIS<1:0> | | 0000 |
| 1110 | IPC8 | 31:16 | — | — | — | RTCCIP<2:0> | | | RTCCIS<1:0> | | — | — | — | FSCMIP<2:0> | | | FSCMIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | I2C2IP<2:0> | | | I2C2IS<1:0> | | — | — | — | U2IP<2:0> | | | U2IS<1:0> | | 0000 |
| 1120 | IPC9 | 31:16 | — | — | — | DMA3IP<2:0> | | | DMA3IS<1:0> | | — | — | — | DMA2IP<2:0> | | | DMA2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | DMA1IP<2:0> | | | DMA1IS<1:0> | | — | — | — | DMA0IP<2:0> | | | DMA0IS<1:0> | | 0000 |
| 1140 | IPC11 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | FCEIP<2:0> | | | FCEIS<1:0> | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** This register does not have associated CLR, SET, and INV registers.

**TABLE 4-13: ADC REGISTERS MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 9110 | ADC1BUFA | 31:16 | ADC Result Word A (ADC1BUFA<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9120 | ADC1BUFB | 31:16 | ADC Result Word B (ADC1BUFB<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9130 | ADC1BUFC | 31:16 | ADC Result Word C (ADC1BUFC<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9140 | ADC1BUFD | 31:16 | ADC Result Word D (ADC1BUFD<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9150 | ADC1BUFE | 31:16 | ADC Result Word E (ADC1BUFE<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9160 | ADC1BUFF | 31:16 | ADC Result Word F (ADC1BUFF<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

## TABLE 4-19: FLASH CONTROLLER REGISTERS MAP

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F400 | NVMCON(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | WR | WREN | WRERR | LVDERR | LVDSTAT | — | — | — | — | — | — | — | NVMOP<3:0> | | | | 0000 |
| F410 | NVMKEY | 31:16 | NVMKEY<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| F420 | NVMADDR(1) | 31:16 | NVMADDR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| F430 | NVMDATA | 31:16 | NVMDATA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| F440 | NVMSRC ADDR | 31:16 | NVMSRCADDR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

## TABLE 4-20: SYSTEM CONTROL REGISTERS MAP(1,2)

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F000 | OSCCON | 31:16 | — | — | PLLODIV<2:0> | | | FRCDIV<2:0> | | | — | SOSCRDY | — | PBDIV<1:0> | | PLLMULT<2:0> | | | 0000 |
| | | 15:0 | — | COSC<2:0> | | | — | NOSC<2:0> | | | CLKLOCK | ULOCK | SLOCK | SLPEN | CF | UFRCEN | SOSCEN | OSWEN | 0000 |
| F010 | OSCTUN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | TUN<5:0> | | | | | | 0000 |
| 0000 | WDTCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | — | — | — | — | — | — | — | SWDTPS<4:0> | | | | | — | WDTCLR | 0000 |
| F600 | RCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CMR | VREGS | EXTR | SWR | — | WDTO | SLEEP | IDLE | BOR | POR | 0000 |
| F610 | RSWRST | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SWRST | 0000 |
| F230 | SYSKEY(3) | 31:16 | SYSKEY<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

**3:** This register does not have associated CLR, SET, and INV registers.

**TABLE 4-43: USB REGISTERS MAP(1) (CONTINUED)**

| Virtual Address (BF88_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 5280 | U1FRML(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | FRML<7:0> | | | | | | | | 0000 |
| 5290 | U1FRMH(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | FRMH<10:8> | | | 0000 |
| 52A0 | U1TOK | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | PID<3:0> | | | | EP<3:0> | | | | 0000 |
| 52B0 | U1SOF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CNT<7:0> | | | | | | | | 0000 |
| 52C0 | U1BDTP2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | BDTPTRH<7:0> | | | | | | | | 0000 |
| 52D0 | U1BDTP3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | BDTPTRU<7:0> | | | | | | | | 0000 |
| 52E0 | U1CNFG1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | UTEYE | UOEMON | USBFRZ | USBSIDL | — | — | — | — | 0000 |
| 5300 | U1EP0 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | LSPD | RETRYDIS | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5310 | U1EP1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5320 | U1EP2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5330 | U1EP3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5340 | U1EP4 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5350 | U1EP5 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5360 | U1EP6 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5370 | U1EP7 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

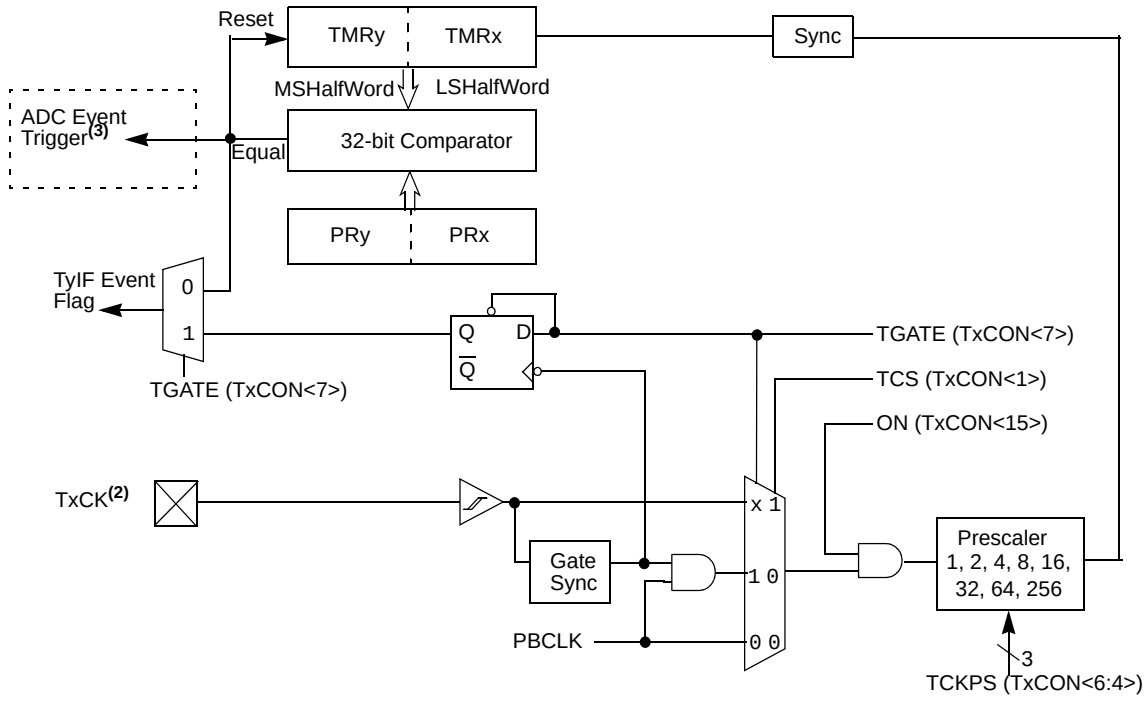
**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** This register does not have associated CLR, SET, and INV registers.

**3:** All bits in this register are read-only; therefore, CLR, SET, and INV registers are not supported.

**4:** The reset value for this bit is undefined.

**FIGURE 14-2: TIMER2/3, 4/5 BLOCK DIAGRAM (32-BIT)**




**Note 1:** In this diagram, the use of 'x' in registers TxCON, TMRx, PRx and TxCK refers to either Timer2 or Timer4; the use of 'y' in registers TyCON, TMRy, PRy and TyIF refers to either Timer3 or Timer5.

**2:** TxCK pins are not available on 64-pin devices.

**3:** ADC event trigger is available only on Timer2/3 pair.

## 25.0 POWER-SAVING FEATURES

**Note 1:** This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Features"** (DS61130) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This section describes power-saving for the PIC32MX3XX/4XX. The PIC32MX devices offer a total of nine methods and modes that are organized into two categories that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

### 25.1 Power-Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the PBCLK, and by individually disabling modules. These methods are grouped into the following modes:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers.
- LPRC Run mode: the CPU is clocked from the LPRC clock source.
- SOSC Run mode: the CPU is clocked from the SOSC clock source.
- Peripheral Bus Scaling mode: peripherals are clocked at programmable fraction of the CPU clock (SYSCLK).

### 25.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which halt the clock to the CPU. These modes operate with all clock sources, as listed below:

- POSC Idle Mode: the system clock is derived from the POSC. The system clock source continues to operate.

  Peripherals continue to operate, but can optionally be individually disabled.
- FRC Idle Mode: the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.
- SOSC Idle Mode: the system clock is derived from the SOSC. Peripherals continue to operate, but can optionally be individually disabled.
- LPRC Idle Mode: the system clock is derived from the LPRC.

  Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.
- Sleep Mode: the CPU, the system clock source, and any peripherals that operate from the system clock source, are halted.

  Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

### 25.3 Power-Saving Operation

The purpose of all power-saving is to reduce power consumption by reducing the device clock frequency. To achieve this, low-frequency clock sources can be selected. In addition, the peripherals and CPU can be halted or disabled to further reduce power consumption.

#### 25.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device Power-Saving operating modes. The CPU and most peripherals are halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep mode.

Sleep mode includes the following characteristics:

- The CPU is halted.
- The system clock source is typically shut down. See **Section 25.3.2 "Idle Mode"** for specific information.
- There can be a wake-up delay based on the oscillator selection.
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode.
- The BOR circuit, if enabled, remains operative during Sleep mode.
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode.
- Some peripherals can continue to operate in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator, e.g., RTCC and Timer 1.
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep.
- The USB module can override the disabling of the POSC or FRC. Refer to **Section 11.0 "USB On-The-Go (OTG)"** for specific details.
- Some modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption.

**REGISTER 26-3: DEVCFG2: DEVICE CONFIGURATION WORD 2**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 23:16 | r-1 | r-1 | r-1 | r-1 | r-1 | R/P | R/P | R/P |
| | — | — | — | — | — | FPLLODIV<2:0> | | |
| 15:8 | R/P | r-1 | r-1 | r-1 | r-1 | R/P | R/P | R/P |
| | UPLLEN | — | — | — | — | UPLLIDIV<2:0> | | |
| 7:0 | r-1 | R/P | R/P | R/P | r-1 | R/P | R/P | R/P |
| | — | FPLLMUL<2:0> | | | — | FPLLIDIV<2:0> | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | P = Programmable bit | r = Reserved bit |
| U = Unimplemented bit | -n = Bit Value at POR: (‘0’, ‘1’, x = Unknown) | | |

bit 31-19 **Reserved:** Write ‘1’

bit 18-16 **FPLLODIV<2:0>:** Default Postscaler for PLL bits
- 111 = PLL output divided by 256
- 110 = PLL output divided by 64
- 101 = PLL output divided by 32
- 100 = PLL output divided by 16
- 011 = PLL output divided by 8
- 010 = PLL output divided by 4
- 001 = PLL output divided by 2
- 000 = PLL output divided by 1

bit 15 **UPLLEN:** USB PLL Enable bit
- 1 = Disable and bypass USB PLL
- 0 = Enable USB PLL

bit 14-11 **Reserved:** Write ‘1’

bit 10-8 **UPLLIDIV<2:0>:** PLL Input Divider bits
- 111 = 12x divider
- 110 = 10x divider
- 101 = 6x divider
- 100 = 5x divider
- 011 = 4x divider
- 010 = 3x divider
- 010 = 3x divider
- 001 = 2x divider
- 000 = 1x divider

bit 7 **Reserved:** Write ‘1’

bit 6-4 **FPLLMUL<2:0>:** PLL Multiplier bits
- 111 = 24x multiplier
- 110 = 21x multiplier
- 101 = 20x multiplier
- 100 = 19x multiplier
- 011 = 18x multiplier
- 010 = 17x multiplier
- 001 = 16x multiplier
- 000 = 15x multiplier

bit 3 **Reserved:** Write ‘1’

bit 2-0 **FPLLIDIV<2:0>:** PLL Input Divider bits
- 111 = 12x divider
- 110 = 10x divider
- 101 = 6x divider
- 100 = 5x divider
- 011 = 4x divider
- 010 = 3x divider
- 001 = 2x divider
- 000 = 1x divider

**TABLE 27-1: MIPS32® INSTRUCTION SET (CONTINUED)**

| Instruction | Description | Function |
|---|---|---|
| TGE | Trap if Greater Than or Equal | if (int)Rs >= (int)Rt<br>TrapException |
| TGEI | Trap if Greater Than or Equal Immediate | if (int)Rs >= (int)Immed<br>TrapException |
| TGEIU | Trap if Greater Than or Equal Immediate Unsigned | if (uns)Rs >= (uns)Immed<br>TrapException |
| TGEU | Trap if Greater Than or Equal Unsigned | if (uns)Rs >= (uns)Rt<br>TrapException |
| TLT | Trap if Less Than | if (int)Rs < (int)Rt<br>TrapException |
| TLTI | Trap if Less Than Immediate | if (int)Rs < (int)Immed<br>TrapException |
| TLTIU | Trap if Less Than Immediate Unsigned | if (uns)Rs < (uns)Immed<br>TrapException |
| TLTU | Trap if Less Than Unsigned | if (uns)Rs < (uns)Rt<br>TrapException |
| TNE | Trap if Not Equal | if Rs != Rt<br>TrapException |
| TNEI | Trap if Not Equal Immediate | if Rs != (int)Immed<br>TrapException |
| WAIT | Wait for Interrupt | Go to a low power mode and stall until interrupt occurs |
| WRPGPR | Write to GPR in Previous Shadow Set | SGPR[$SRSCtl_{PSS}$, Rd> = Rt |
| WSBH | Word Swap Bytes Within Halfwords | Rd = $Rt_{23..16}$ \|\| $Rt_{31..24}$ \|\| $Rt_{7..0}$ \|\| $Rt_{15..8}$ |
| XOR | Exclusive OR | Rd = Rs ^ Rt |
| XORI | Exclusive OR Immediate | Rt = Rs ^ (uns)Immed |

**Note 1:** This instruction is deprecated and should not be used.

**FIGURE 29-5: EXTERNAL RESET TIMING CHARACTERISTICS**

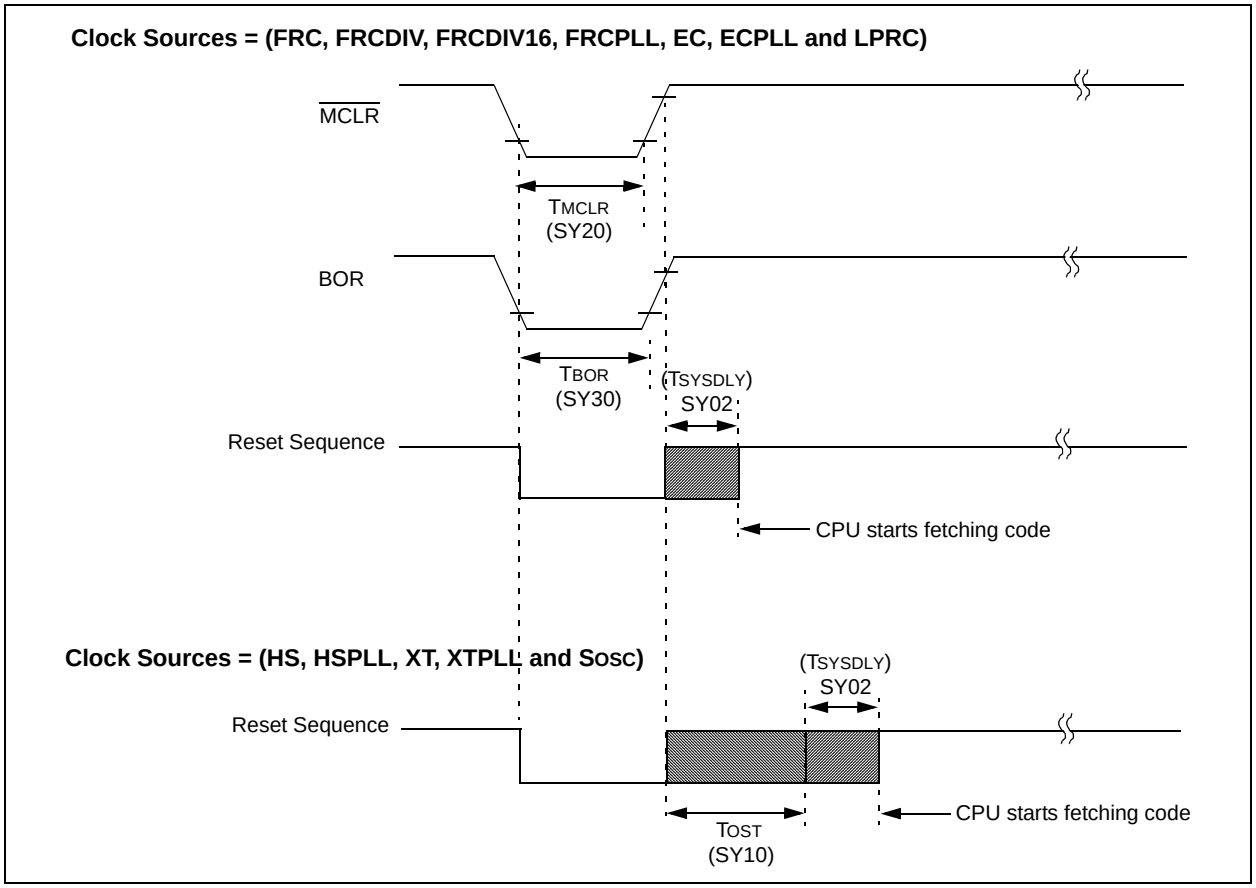
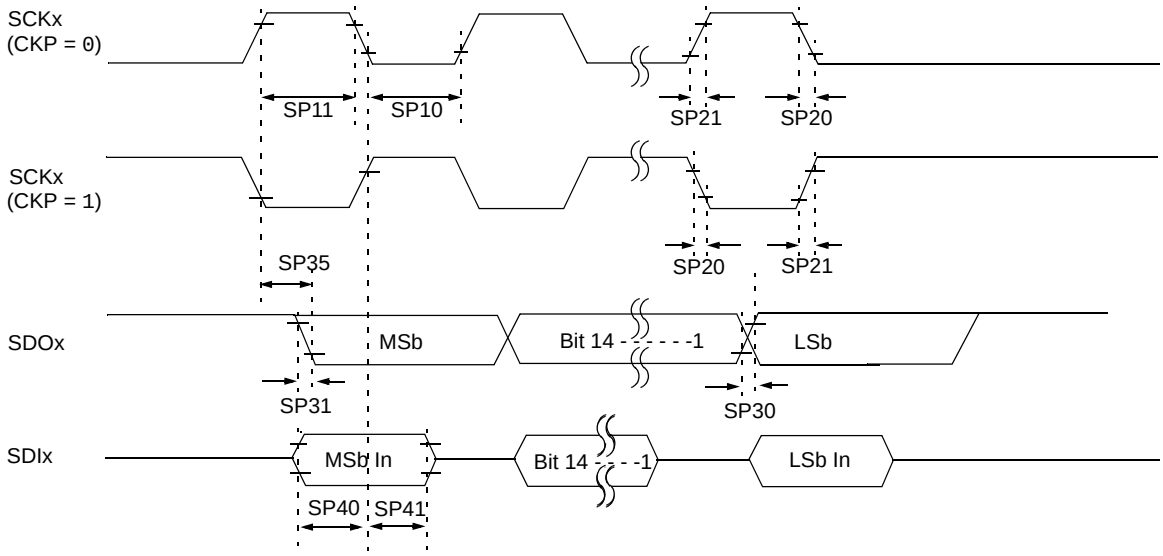



**TABLE 29-22: RESETS TIMING**

| AC CHARACTERISTICS | | | **Standard Operating Conditions: 2.3V to 3.6V**<br>(unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| SY00 | TPU | Power-up Period<br>Internal Voltage Regulator Enabled | — | 400 | 600 | µs | -40°C to +85°C |
| SY01 | TPWRT | Power-up Period<br>External Vcore Applied<br>(Power-Up-Timer Active) | 48 | 64 | 80 | ms | -40°C to +85°C |
| SY02 | TSYSDLY | System Delay Period:<br>Time required to reload Device Configuration Fuses plus SYSCLK delay before first instruction is fetched. | — | 1 µs<br>+<br>8 SYSCLK<br>cycles | — | — | -40°C to +85°C |
| SY20 | TMCLR | $\overline{\text{MCLR}}$ Pulse Width (low) | — | 2 | — | µs | -40°C to +85°C |
| SY30 | TBOR | BOR Pulse Width (low) | — | 1 | — | µs | -40°C to +85°C |

**Note 1:** These parameters are characterized, but not tested in manufacturing.
**2:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.

**FIGURE 29-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 29-1 for load conditions.

**TABLE 29-28: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | TscL | SCKx Output Low Time(3) | Tsck/2 | — | — | ns | — |
| SP11 | TscH | SCKx Output High Time(3) | Tsck/2 | — | — | ns | — |
| SP20 | TscF | SCKx Output Fall Time(4) | — | — | — | ns | See parameter DO32 |
| SP21 | TscR | SCKx Output Rise Time(4) | — | — | — | ns | See parameter DO31 |
| SP30 | TdoF | SDOx Data Output Fall Time(4) | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time(4) | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 15 | ns | VDD > 2.7V |
| | | | — | — | 20 | ns | VDD < 2.7V |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |

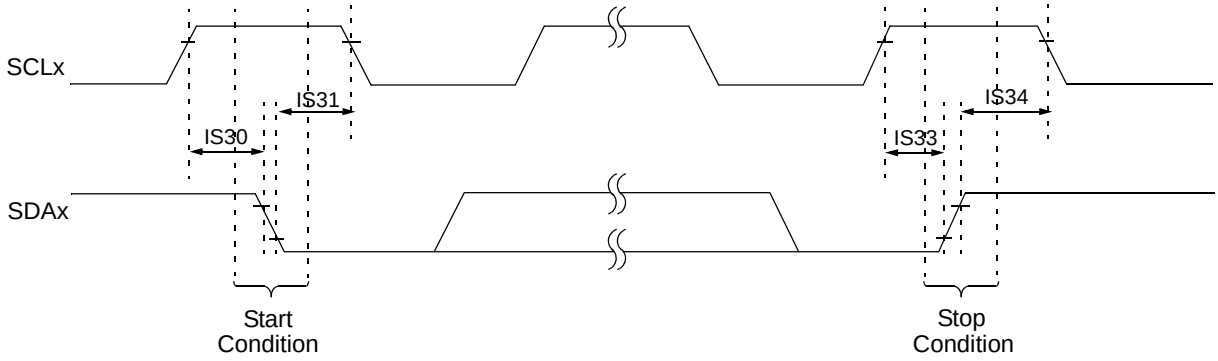
**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

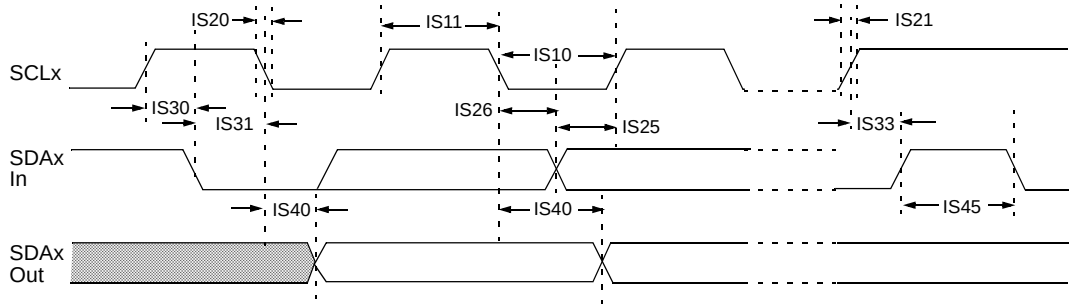
**4:** Assumes 50 pF load on all SPIx pins.

**FIGURE 29-16: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)**




**Note:** Refer to Figure 29-1 for load conditions.

**FIGURE 29-17: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)**




**Note:** Refer to Figure 29-1 for load conditions.

**TABLE 29-36: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS**

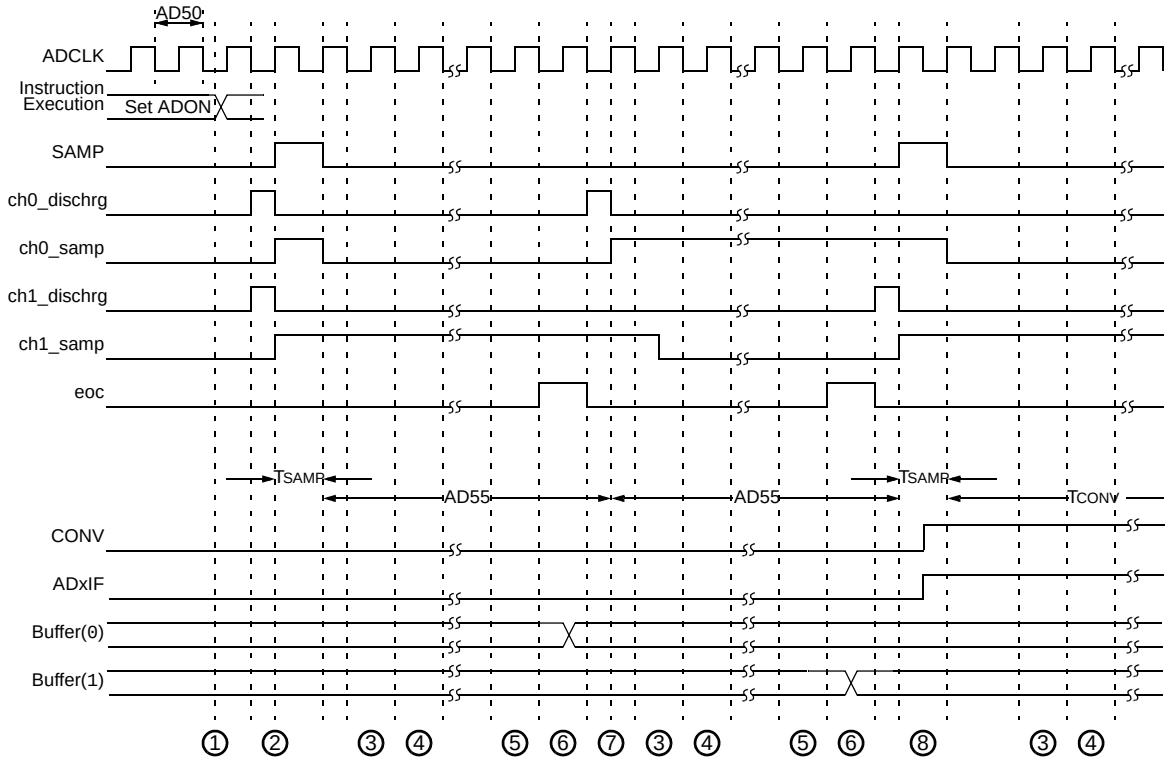
| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| **Clock Parameters** | | | | | | | |
| AD50 | TAD | Analog-to-Digital Clock Period | 65 | — | — | ns | See Table 29-35 and **Note 2** |
| AD51 | TRC | Analog-to-Digital Internal RC Oscillator Period | — | 250 | — | ns | See **Note 3** |
| **Conversion Rate** | | | | | | | |
| AD55 | TCONV | Conversion Time | — | 12 TAD | — | — | — |
| AD56 | FCNV | Throughput Rate (Sampling Speed) | — | — | 1000 | KSPS | AVDD = 3.0V to 3.6V |
| | | | — | — | 400 | KSPS | AVDD = 2.5V to 3.6V |
| AD57 | TSAMP | Sample Time | 1 TAD | — | — | — | TSAMP must be ≥ 132 ns. |
| **Timing Parameters** | | | | | | | |
| AD60 | TPCS | Conversion Start from Sample Trigger | — | 1.0 TAD | — | — | Auto-Convert Trigger (SSRC<2:0> = 111) not selected. See **Note 3** |
| AD61 | TPSS | Sample Start from Setting Sample (SAMP) bit | 0.5 TAD | — | 1.5 TAD | — | — |
| AD62 | TCSS | Conversion Completion to Sample Start (ASAM = 1) | — | 0.5 TAD | — | — | See **Note 3** |
| AD63 | TDPU | Time to Stabilize Analog Stage from Analog-to-Digital OFF to Analog-to-Digital ON | — | — | 2 | µs | See **Note 3** |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

**3:** Characterized by design but not tested.

**FIGURE 29-19: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRC<2:0> = 111, SAMC<4:0> = 00001)**




(1) – Software sets ADxCON. ADON to start AD operation.

(2) – Sampling starts after discharge period. TSAMP is described in **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS61104) of the *"PIC32 Family Reference Manual"*.

(3) – Convert bit 9.

(4) – Convert bit 8.

(5) – Convert bit 0.

(6) – One TAD for end of conversion.

(7) – Begin conversion of next channel.

(8) – Sample for time specified by SAMC<4:0>.

**FIGURE 29-23: EJTAG TIMING CHARACTERISTICS**

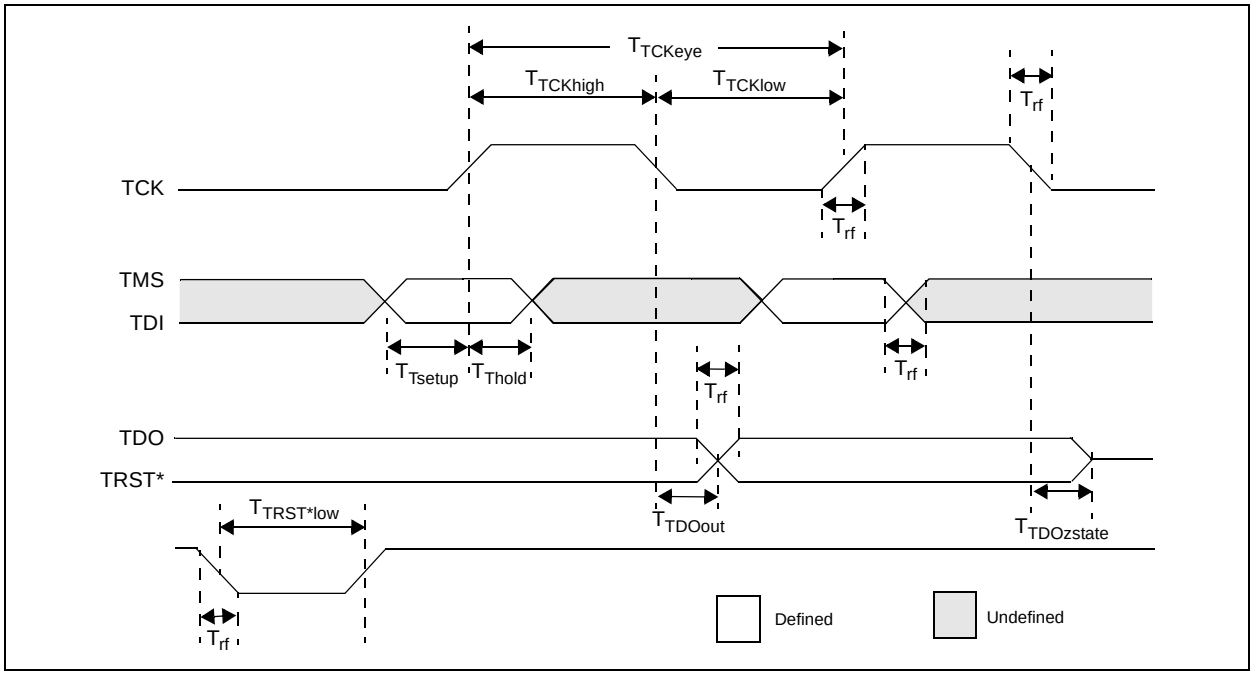


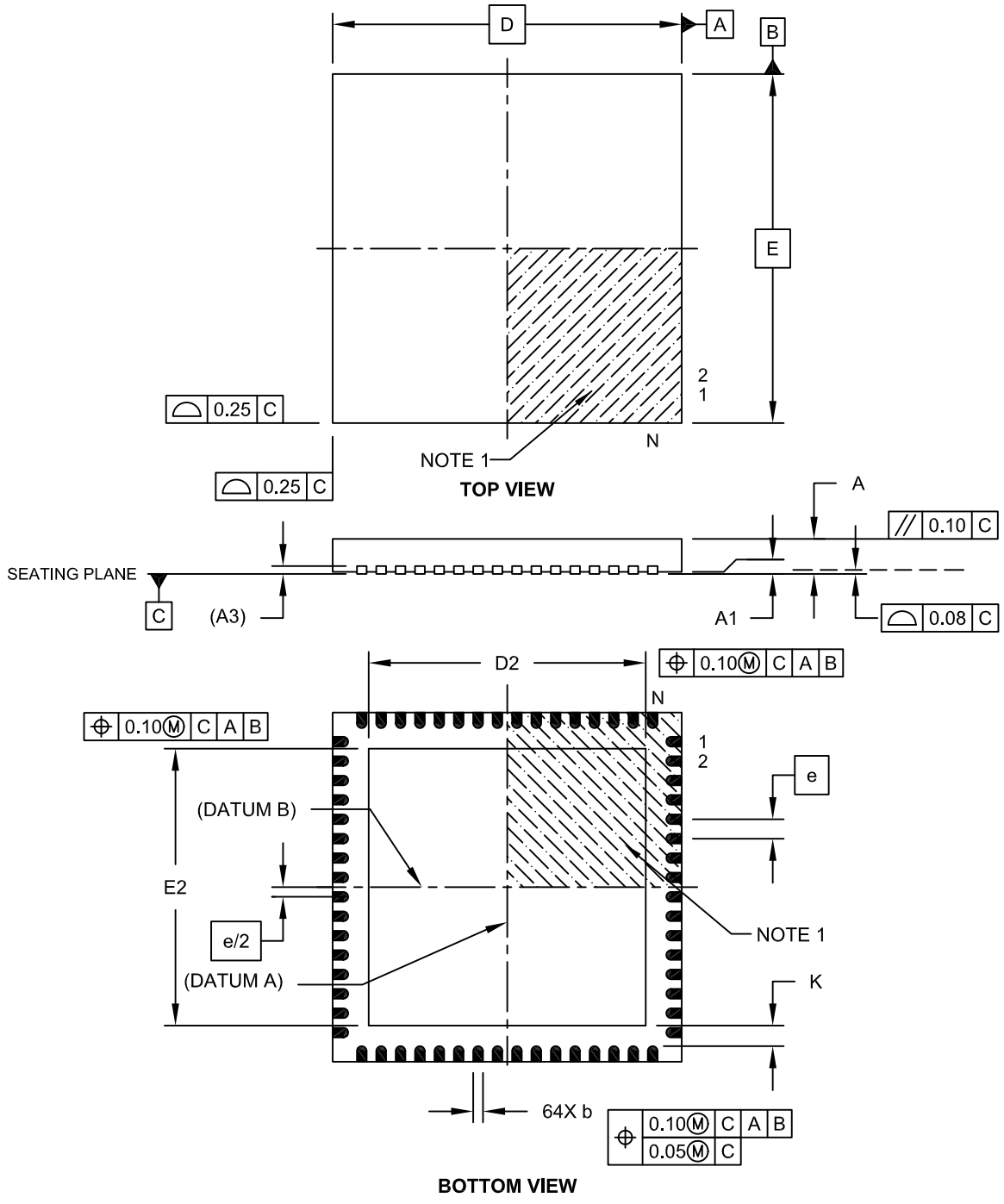

**TABLE 29-41: EJTAG TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+105°C for V-Temp | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Description(1)** | **Min.** | **Max.** | **Units** | **Conditions** |
| EJ1 | TTCKCYC | TCK Cycle Time | 25 | — | ns | — |
| EJ2 | TTCKHIGH | TCK High Time | 10 | — | ns | — |
| EJ3 | TTCKLOW | TCK Low Time | 10 | — | ns | — |
| EJ4 | TTSETUP | TAP Signals Setup Time Before Rising TCK | 5 | — | ns | — |
| EJ5 | TTHOLD | TAP Signals Hold Time After Rising TCK | 3 | — | ns | — |
| EJ6 | TTDOOUT | TDO Output Delay Time from Falling TCK | — | 5 | ns | — |
| EJ7 | TTDOZSTATE | TDO 3-State Delay Time from Falling TCK | — | 5 | ns | — |
| EJ8 | TTRSTLOW | TRST Low Time | 25 | — | ns | — |
| EJ9 | TRF | TAP Signals Rise/Fall Time, All Input and Output | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]**
**With 7.15 x 7.15 Exposed Pad [QFN]**

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




Microchip Technology Drawing C04-149C Sheet 1 of 2