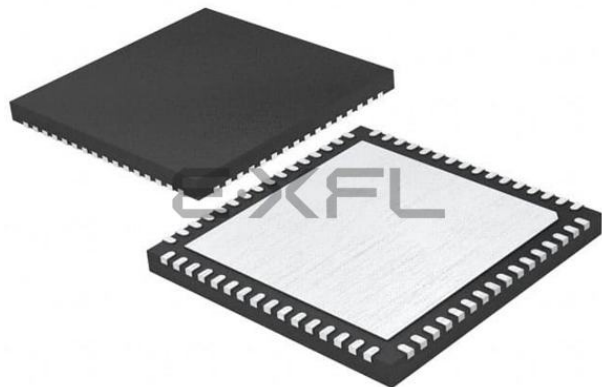




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Details

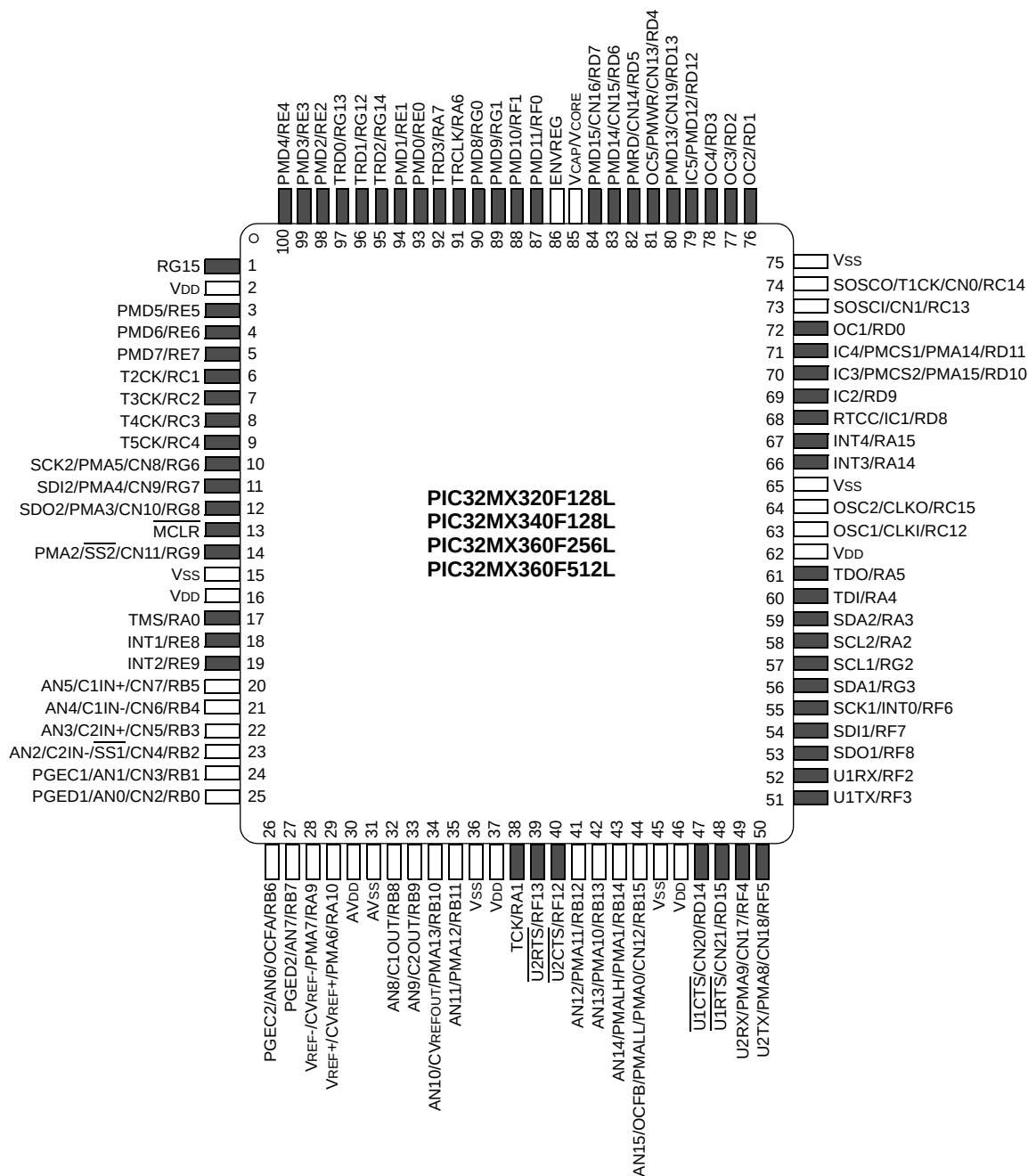
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx320f064ht-80i-mr

PIC32MX3XX/4XX

Pin Diagrams (Continued)

100-Pin TQFP (General Purpose)

■ = Pins are up to 5V tolerant



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PIC32MX3XX/4XX

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number ⁽¹⁾			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
PMD0	60	93	A4	I/O	TTL/ST	Parallel Master Port Data (De-multiplexed Master mode) or Address/Data (Multiplexed Master modes).
PMD1	61	94	B4	I/O	TTL/ST	
PMD2	62	98	B3	I/O	TTL/ST	
PMD3	63	99	A2	I/O	TTL/ST	
PMD4	64	100	A1	I/O	TTL/ST	
PMD5	1	3	D3	I/O	TTL/ST	
PMD6	2	4	C1	I/O	TTL/ST	
PMD7	3	5	D2	I/O	TTL/ST	
PMD8	—	90	A5	I/O	TTL/ST	
PMD9	—	89	E6	I/O	TTL/ST	
PMD10	—	88	A6	I/O	TTL/ST	
PMD11	—	87	B6	I/O	TTL/ST	
PMD12	—	79	A9	I/O	TTL/ST	
PMD13	—	80	D8	I/O	TTL/ST	
PMD14	—	83	D7	I/O	TTL/ST	
PMD15	—	84	C7	I/O	TTL/ST	
PMRD	53	82	B8	O	—	Parallel Master Port Read Strobe.
PMWR	52	81	C8	O	—	Parallel Master Port Write Strobe.
PMALL	30	44	L8	O	—	Parallel Master Port Address Latch Enable low-byte (Multiplexed Master modes).
PMALH	29	43	K7	O	—	Parallel Master Port Address Latch Enable high-byte (Multiplexed Master modes).
VBUS	34	54	H8	I	Analog	USB Bus Power Monitor.
VUSB	35	55	H9	P	—	USB Internal Transceiver Supply. If the USB module is <i>not</i> used, this pin must be connected to VDD.
VBUSON	11	20	H1	O	—	USB Host and OTG Bus Power Control Output.
D+	37	57	H10	I/O	Analog	USB D+.
D-	36	56	J11	I/O	Analog	USB D-.
USBID	33	51	K10	I	ST	USB OTG ID Detect.
ENVREG	57	86	A7	I	ST	Enable for On-Chip Voltage Regulator.
TRCLK	—	91	C5	O	—	Trace Clock.
TRD0	—	97	A3	O	—	Trace Data Bits 0-3.
TRD1	—	96	C3	O	—	
TRD2	—	95	C4	O	—	
TRD3	—	92	B5	O	—	
PGED1	16	25	K2	I/O	ST	Data I/O pin for programming/debugging communication channel 1.
PGEC1	15	24	K1	I	ST	Clock input pin for programming/debugging communication channel 1.

Legend: CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = TTL input buffer

Analog = Analog input
 O = Output

P = Power
 I = Input

Note 1: Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternately, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 2, MPLAB ICD 3 or MPLAB REAL ICE™.

For more information on ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- "MPLAB® ICD 2 In-Circuit Debugger User's Guide" DS51331
- "Using MPLAB® ICD 2" (poster) DS51265
- "MPLAB® ICD 2 Design Advisory" DS51566
- "Using MPLAB® ICD 3" (poster) DS51765
- "MPLAB® ICD 3 Design Advisory" DS51764
- "MPLAB® REAL ICE™ In-Circuit Debugger User's Guide" DS51616
- "Using MPLAB® REAL ICE™" (poster) DS51749

2.6 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternately, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

2.7 Trace

The trace pins can be connected to a hardware-trace-enabled programmer to provide a compress real time instruction trace. When used for trace the TRD3, TRD2, TRD1, TRD0 and TRCLK pins should be dedicated for this use. The trace hardware requires a 22 Ohm series resistor between the trace pins and the trace connector.

2.8 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT

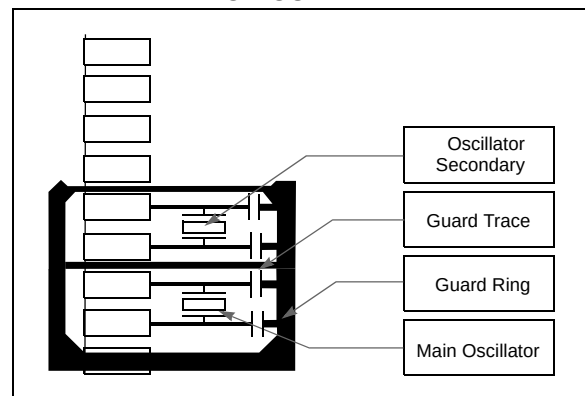


TABLE 4-9: OUTPUT COMPARE1-5 REGISTERS MAP⁽¹⁾

Virtual Address (BF80-#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	OC1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3010	OC1R	31:16	OC1R<31:0>																XXXX
		15:0																	XXXX
3020	OC1RS	31:16	OC1RS<31:0>																XXXX
		15:0																	XXXX
3200	OC2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3210	OC2R	31:16	OC2R<31:0>																XXXX
		15:0																	XXXX
3220	OC2RS	31:16	OC2RS<31:0>																XXXX
		15:0																	XXXX
3400	OC3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3410	OC3R	31:16	OC3R<31:0>																XXXX
		15:0																	XXXX
3420	OC3RS	31:16	OC3RS<31:0>																XXXX
		15:0																	XXXX
3600	OC4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3610	OC4R	31:16	OC4R<31:0>																XXXX
		15:0																	XXXX
3620	OC4RS	31:16	OC4RS<31:0>																XXXX
		15:0																	XXXX
3800	OC5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3810	OC5R	31:16	OC5R<31:0>																XXXX
		15:0																	XXXX
3820	OC5RS	31:16	OC5RS<31:0>																XXXX
		15:0																	XXXX

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 4-16: DMA CHANNELS 0-3 REGISTERS MAP FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY⁽¹⁾

Virtual Address (BF88-#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
3060	DCH0CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	0000	
3070	DCH0ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>							00FF	
		15:0	CHSIRQ<7:0>							CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00	
3080	DCH0INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3090	DCH0SSA	31:16	CHSSA<31:0>															0000	
		15:0																0000	
30A0	DCH0DSA	31:16	CHDSA<31:0>															0000	
		15:0																0000	
30B0	DCH0SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHSSIZ<7:0>							0000	
30C0	DCH0DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHDSIZ<7:0>							0000	
30D0	DCH0SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHSTR<7:0>							0000	
30E0	DCH0DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHDPTR<7:0>							0000	
30F0	DCH0CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHCSIZ<7:0>							0000	
3100	DCH0CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHCPTR<7:0>							0000	
3110	DCH0DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>							0000	
3120	DCH1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	0000
3130	DCH1ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>							00FF	
		15:0	CHSIRQ<7:0>							CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00	
3140	DCH1INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3150	DCH1SSA	31:16	CHSSA<31:0>															0000	
		15:0																0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers except DCHxSPTR, DCHxDPTR and DCHxCPTR have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-17: COMPARATOR REGISTERS MAP⁽¹⁾

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A000	CM1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		00C3
A010	CM2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		00C3
A060	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	C2OUT	C1OUT	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 4-18: COMPARATOR VOLTAGE REFERENCE REGISTERS MAP⁽¹⁾

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9800	CVRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	CVROE	CVRR	CVRSS	CVR<3:0>				0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 4-19: FLASH CONTROLLER REGISTERS MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
F400	NVMCON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WR	WREN	WRERR	LVDERR	LVDSTAT	—	—	—	—	—	—	NVMOP<3:0>				0000
F410	NVMKEY	31:16	NVMKEY<31:0>															0000
		15:0																0000
F420	NVMADDR ⁽¹⁾	31:16	NVMADDR<31:0>															0000
		15:0																0000
F430	NVMDATA	31:16	NVMDATA<31:0>															0000
		15:0																0000
F440	NVMSRC ADDR	31:16	NVMSRCADDR<31:0>															0000
		15:0																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 4-20: SYSTEM CONTROL REGISTERS MAP^(1,2)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F000	OSCCON	31:16	—	—	PLLODIV<2:0>			FRCDIV<2:0>			—	SOSCRDY	—	PBDIV<1:0>		PLLMULT<2:0>			0000
		15:0	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	ULOCK	SLOCK	SLPEN	CF	UFRGEN	SOSCEN	OSWEN	0000
F010	OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000
0000	WDTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	SWDTPS<4:0>					—	WDTCLR	0000
F600	RCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CMR	VREGS	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR	POR
F610	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST
F230	SYSKEY ⁽³⁾	31:16	SYSKEY<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

2: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

3: This register does not have associated CLR, SET, and INV registers.

TABLE 4-37: PARALLEL MASTER PORT REGISTERS MAP⁽¹⁾

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7000	PMCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	ADRMUX<1:0>		PMP TTL	PTWREN	PTRDEN	CSF<1:0>		ALP	CS2P	CS1P	—	WRSP	RDSP	0000
7010	PMMODE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>		WAITB<1:0>		WAITM<3:0>			WAITE<1:0>			0000
7020	PMADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CS2EN/A15	CS1EN/A14	ADDR<13:0>														
7030	PMDOUT	31:16	DATAOUT<31:0>																0000
		15:0																	0000
7040	PMDIN	31:16	DATAIN<31:0>																0000
		15:0																	0000
7050	PMAEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PTEN<15:0>																0000
7060	PMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 4-38: PROGRAMMING AND DIAGNOSTICS REGISTERS MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F200	DDPCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	JTAGEN	TROEN	—	—	0008

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-39: PREFETCH REGISTERS MAP

Virtual Address (BF88_#)	Register Name	Bit Range	Bits															All Resets			
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0		
4000	CHECON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CHECOH	0000		
		15:0	—	—	—	—	—	—	DCSZ<1:0>		—	—	PREFEN<1:0>		—	PFMWS<2:0>			0007		
4010	CHEACC ⁽¹⁾	31:16	CHEWEN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	CHEIDX<3:0>				00xx		
4020	CHETAG ⁽¹⁾	31:16	LTAGBOOT	—	—	—	—	—	—	—	LTAG<23:16>										xxx0
		15:0	LTAG<15:4>												LVALID		LLOCK	LTYPE	—	xxx2	
4030	CHEMSK ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	LMASK<15:5>												—	—	—	—	—	xxxx	
4040	CHEW0	31:16	CHEW0<31:0>																xxxx		
		15:0																	xxxx		
4050	CHEW1	31:16	CHEW1<31:0>																xxxx		
		15:0																	xxxx		
4060	CHEW2	31:16	CHEW2<31:0>																xxxx		
		15:0																	xxxx		
4070	CHEW3	31:16	CHEW3<31:0>																xxxx		
		15:0																	xxxx		
4080	CHELRU	31:16	—	—	—	—	—	—	—	CHELRU<24:16>										0000	
		15:0	CHELRU<15:0>																0000		
4090	CHEHIT	31:16	CHEHIT<31:0>																xxxx		
		15:0																	xxxx		
40A0	CHEMIS	31:16	CHEMIS<31:0>																xxxx		
		15:0																	xxxx		
40C0	CHEPFABT	31:16	CHEPFABT<31:0>																xxxx		
		15:0																	xxxx		

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 4-43: USB REGISTERS MAP⁽¹⁾

Virtual Address (BF88-#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5040	U1OTG IR ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF	0000
5050	U1OTG IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE	0000
5060	U1OTG STAT ⁽³⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD	0000
5070	U1OTG CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
5080	U1PWRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UACTPND ⁽⁴⁾	—	—	USLPGRD	—	—	USUSPEND	USBPWR	0000
5200	U1IR ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF DETACHIF	0000 0000
5210	U1IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE DETACHIE	0000 0000
5220	U1EIR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF EOFEF	PIDEF	0000 0000
5230	U1EIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE EOFEE	PIDEE	0000 0000
5240	U1STAT ⁽³⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ENDPT<3:0> ⁽⁴⁾				DIR	PPBI	—	—	0000
5250	U1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	JSTATE ⁽⁴⁾	SE0 ⁽⁴⁾	PKTDIS TOKBUSY	USBRST	HOSTEN	RESUME	PPBRST	USBEN SOFEN	0000 0000
5260	U1ADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPDEN	DEVADDR<6:0>							0000
5270	U1BDTP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRL<7:1>							—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
- 2:** This register does not have associated CLR, SET, and INV registers.
- 3:** All bits in this register are read-only; therefore, CLR, SET, and INV registers are not supported.
- 4:** The reset value for this bit is undefined.

PIC32MX3XX/4XX

NOTES:

14.0 TIMER2/3 AND TIMER4/5

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. “Timers”** (DS61105) of the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

This family of PIC32MX devices features four synchronous 16-bit timers (default) that can operate as a free-running interval timer for various timing applications and counting external events. The following modes are supported:

- Synchronous Internal 16-bit Timer
- Synchronous Internal 16-bit Gated Timer
- Synchronous External 16-bit Timer

Two 32-bit synchronous timers are available by combining Timer2 with Timer3 and Timer4 with Timer5. The 32-bit timers can operate in three modes:

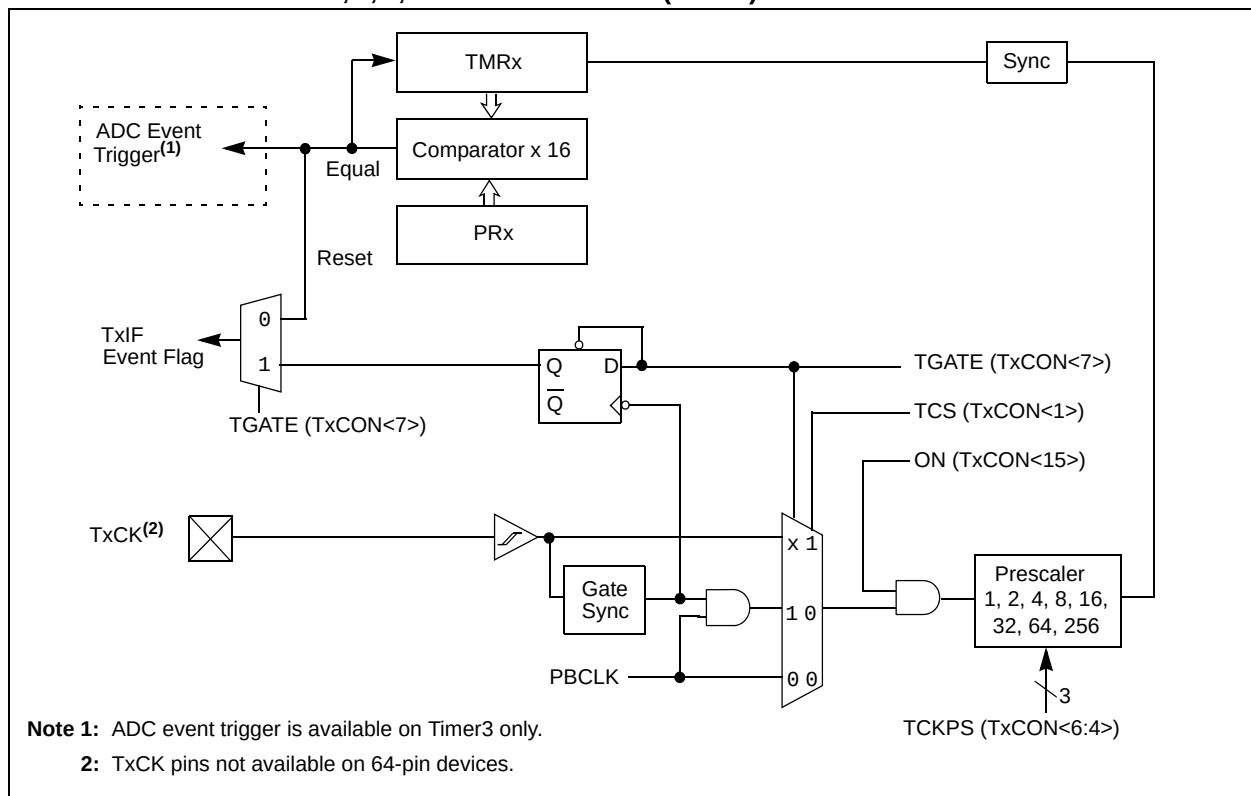
- Synchronous Internal 32-bit Timer
- Synchronous Internal 32-bit Gated Timer
- Synchronous External 32-bit Timer

Note: Throughout this chapter, references to registers TxCON, TMRx and PRx use 'x' to represent Timer2 through 5 in 16-bit modes. In 32-bit modes, 'x' represents Timer2 or 4; 'y' represents Timer3 or 5.

14.1 Additional Supported Features

- Selectable clock prescaler
- Timers operational during CPU Idle
- Time base for input capture and output compare modules (Timer2 and Timer3 only)
- ADC event trigger (Timer3 only)
- Fast bit manipulation using CLR, SET and INV registers

FIGURE 14-1: TIMER2, 3, 4, 5 BLOCK DIAGRAM (16-BIT)



18.0 INTER-INTEGRATED CIRCUIT™ (I²C™)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. “Inter-Integrated Circuit (I²C™)”** (DS61116) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

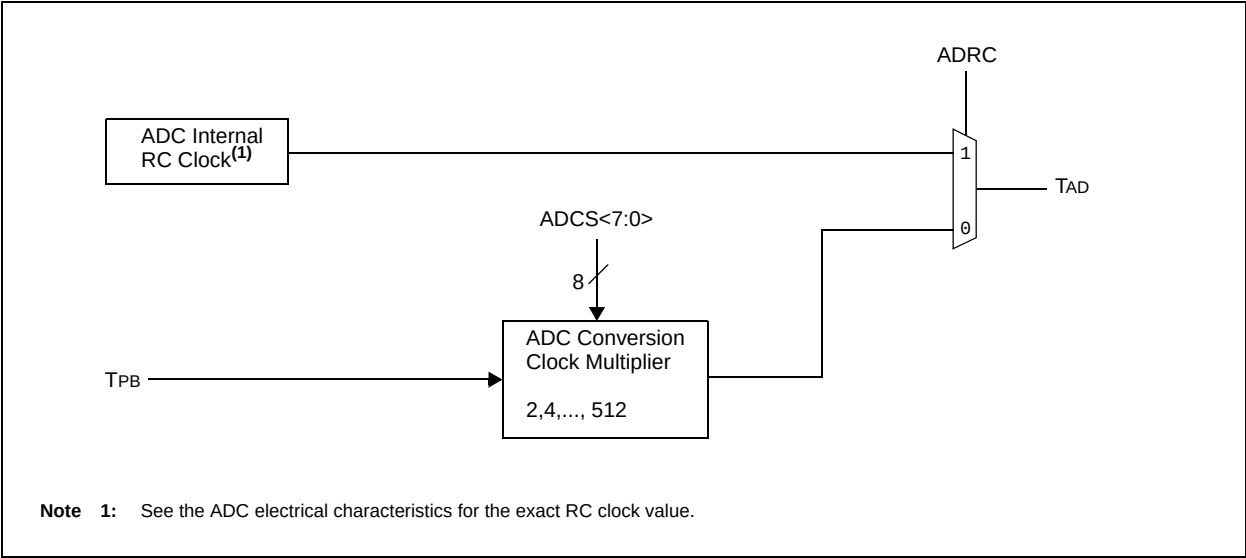
The I²C module provides complete hardware support for both Slave and Multi-Master modes of the I²C serial communication standard. Figure 18-1 illustrates the I²C module block diagram.

The PIC32MX3XX/4XX devices have up to two I²C interface modules, denoted as I2C1 and I2C2. Each I²C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I²C module, ‘I2Cx’ (x = 1 or 2), offers the following key features:

- I²C Interface Supporting both Master and Slave Operation.
- I²C Slave Mode Supports 7 and 10-bit Address.
- I²C Master Mode Supports 7 and 10-bit Address.
- I²C Port allows Bidirectional Transfers between Master and Slaves.
- Serial Clock Synchronization for I²C Port can be used as a Handshake Mechanism to Suspend and Resume Serial Transfer (SCLREL control).
- I²C Supports Multi-master Operation; Detects Bus Collision and Arbitrates Accordingly.
- Provides Support for Address Bit Masking.

FIGURE 22-2: ADC CONVERSION CLOCK PERIOD BLOCK DIAGRAM



REGISTER 26-2: DEVCFG1: DEVICE CONFIGURATION WORD 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	R/P	r-1	r-1	R/P	R/P	R/P	R/P	R/P
	FWDTEN	—	—	WDTPS<4:0>				
15:8	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P
	IESO	—	FSOSCEN	—	—	FNOSC<2:0>		

Legend:

R = Readable bit

W = Writable bit

P = Programmable bit

r = Reserved bit

U = Unimplemented bit

-n = Bit Value at POR: ('0', '1', x = Unknown)

bit 31-24 **Reserved:** Write '1'

bit 23 **FWDTEN:** Watchdog Timer Enable bit

1 = The WDT is enabled and cannot be disabled by software

0 = The WDT is not enabled; it can be enabled in software

bit 22-21 **Reserved:** Write '1'

bit 20-16 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits

10100 = 1:1048576

10011 = 1:524288

10010 = 1:262144

10001 = 1:131072

10000 = 1:65536

01111 = 1:32768

01110 = 1:16384

01101 = 1:8192

01100 = 1:4096

01011 = 1:2048

01010 = 1:1024

01001 = 1:512

01000 = 1:256

00111 = 1:128

00110 = 1:64

00101 = 1:32

00100 = 1:16

00011 = 1:8

00010 = 1:4

00001 = 1:2

00000 = 1:1

All other combinations not shown result in operation = '10100'

bit 15-14 **FCKSM<1:0>:** Clock Switching and Monitor Selection Configuration bits

1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled

01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled

00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

Note 1: Do not disable Posc (POSCMOD = 00) when using this oscillator source.

27.0 INSTRUCTION SET

The PIC32MX3XX/4XX family instruction set complies with the MIPS32 Release 2 instruction set architecture. PIC32MX does not support the following features:

- CoreExtend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Table 27-1 provides a summary of the instructions that are implemented by the PIC32MX3XX/4XX family core.

Note: Refer to “MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set” at www.mips.com for more information.

TABLE 27-1: MIPS32® INSTRUCTION SET

Instruction	Description	Function
ADD	Integer Add	$Rd = Rs + Rt$
ADDI	Integer Add Immediate	$Rt = Rs + \text{Immed}$
ADDIU	Unsigned Integer Add Immediate	$Rt = Rs +_U \text{Immed}$
ADDU	Unsigned Integer Add	$Rd = Rs +_U Rt$
AND	Logical AND	$Rd = Rs \& Rt$
ANDI	Logical AND Immediate	$Rt = Rs \& (0_{16} \parallel \text{Immed})$
B	Unconditional Branch (Assembler idiom for: BEQ r0, r0, offset)	$PC += (\text{int})\text{offset}$
BAL	Branch and Link (Assembler idiom for: BGEZAL r0, offset)	$GPR[31] = PC + 8$ $PC += (\text{int})\text{offset}$
BEQ	Branch on Equal	if $Rs == Rt$ $PC += (\text{int})\text{offset}$
BEQL	Branch on Equal Likely ⁽¹⁾	if $Rs == Rt$ $PC += (\text{int})\text{offset}$ else Ignore Next Instruction
BGEZ	Branch on Greater Than or Equal to Zero	if $!Rs[31]$ $PC += (\text{int})\text{offset}$
BGEZAL	Branch on Greater Than or Equal to Zero and Link	$GPR[31] = PC + 8$ if $!Rs[31]$ $PC += (\text{int})\text{offset}$
BGEZALL	Branch on Greater Than or Equal to Zero and Link Likely ⁽¹⁾	$GPR[31] = PC + 8$ if $!Rs[31]$ $PC += (\text{int})\text{offset}$ else Ignore Next Instruction
BGEZL	Branch on Greater Than or Equal to Zero Likely ⁽¹⁾	if $!Rs[31]$ $PC += (\text{int})\text{offset}$ else Ignore Next Instruction
BGTZ	Branch on Greater Than Zero	if $!Rs[31] \&\& Rs != 0$ $PC += (\text{int})\text{offset}$
BGTZL	Branch on Greater Than Zero Likely ⁽¹⁾	if $!Rs[31] \&\& Rs != 0$ $PC += (\text{int})\text{offset}$ else Ignore Next Instruction
BLEZ	Branch on Less Than or Equal to Zero	if $Rs[31] \parallel Rs == 0$ $PC += (\text{int})\text{offset}$

Note 1: This instruction is deprecated and should not be used.

29.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of PIC32MX3XX/4XX electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MX3XX/4XX are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings (Note 1)

Ambient temperature under bias.....	-40°C to +105°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to VSS	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to VSS (Note 3).....	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 2.3V (Note 3).....	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to VSS when VDD < 2.3V (Note 3).....	-0.3V to +3.6V
Voltage on VCore with respect to VSS	-0.3V to 2.0V
Voltage on VBUS with respect to VSS	-0.3V to +5.5V
Maximum current out of VSS pin(s).....	300 mA
Maximum current into VDD pin(s) (Note 2).....	300 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports (Note 2).....	200 mA

Note 1: Stresses above those listed under “**Absolute Maximum Ratings**” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

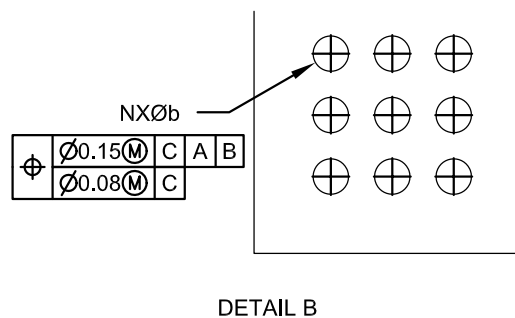
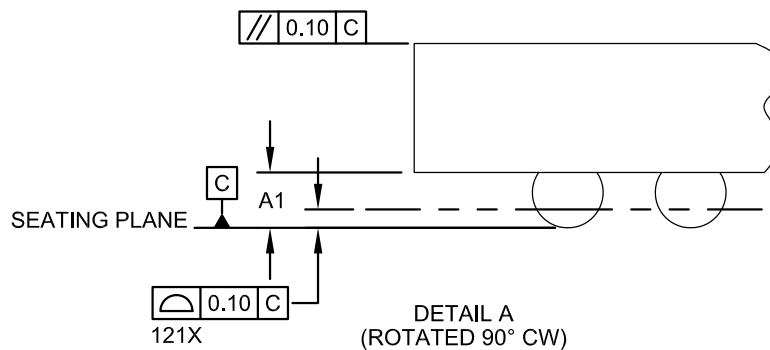
2: Maximum allowable current is a function of device maximum power dissipation (see Table 29-2).

3: See the “**Pin Diagrams**” section for the 5V tolerant pins.

PIC32MX3XX/4XX

121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [XBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Contacts	N	121		
Contact Pitch	e	0.80 BSC		
Overall Height	A	1.00	1.10	1.20
Standoff	A1	0.25	0.30	0.35
Molded Package Thickness	A2	0.55	0.60	0.65
Overall Width	E	10.00 BSC		
Array Width	E1	8.00 BSC		
Overall Length	D	10.00 BSC		
Array Length	D1	8.00 BSC		
Contact Diameter	b	0.40 TYP		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
3. The outer rows and columns of balls are located with respect to datums A and B.

Microchip Technology Drawing C04-148 Rev B Sheet 2 of 2

Revision G (April 2010)

The revision includes the following global update:

- Added Note 2 to the shaded table that appears at the beginning of each chapter. This new note provides information regarding the availability of registers and their associated bits.

This revision also includes minor typographical and formatting changes throughout the data sheet text. Major updates are referenced by their respective section in the following table.

TABLE A-2: MAJOR SECTION UPDATES

Section Name	Update Description
“High-Performance, General Purpose and USB 32-bit Flash Microcontrollers”	Updated the crystal oscillator range to 3 MHz to 25 MHz (see Peripheral Features): Added the 121-pin Ball Grid Array (XBGA) pin diagram. Updated Table 1: “PIC32MX General Purpose – Features” and Table 2: “PIC32MX USB – Features” Added the following tables: - Table 3: “Pin Names: PIC32MX320F128L, PIC32MX340F128L, and PIC32MX360F128L, and PIC32MX360F512L Devices”, - Table 4: “Pin Names: PIC32MX440F128L, PIC32MX460F256L and PIC32MX460F512L Devices” Updated the following pins as 5V tolerant: - 64-pin QFN (USB): Pin 34 (VBUS), Pin 36 (D-/RG3) and Pin 37 (D+/RG2) - 64-pin TQFP (USB): Pin 34 (Vbus), Pin 36 (D-/RG3), Pin 37 (D+/RG2) and Pin 42 (IC1/RTCC/INT1/RD8) - 100-pin TQFP (USB): Pin 54 (VBUS), Pin 56 (D-/RG3) and Pin 57 (D+/RG2)
Section 1.0 “Device Overview”	Updated the Pinout I/O Descriptions table to include the device pin numbers (see Table 1-1)
Section 2.0 “Guidelines for Getting Started with 32-bit Microcontrollers”	Updated the Ohm value for the low-ESR capacitor from less than 5 to less than 1 (see Section 2.3.1 “Internal Regulator Mode”). Labeled the capacitor on the VCAP/VDDCORE pin as CEFC in Figure 2-1. Changed 10 µF capacitor to CEFC capacitor in Section 2.3 “Capacitor on Internal Voltage Regulator (VCAP/VCORE)”.
Section 4.0 “Memory Organization”	Updated all register map tables to include the “All Resets” column. Separated the PORT register maps into individual tables (see Table 4-21 through Table 4-34). In addition, formatting changes were made to improve readability.
Section 12.0 “I/O Ports”	Updated the second paragraph of Section 12.1.2 “Digital Inputs” and removed Table 12-1.
Section 22.0 “10-bit Analog-to-Digital Converter (ADC)”	Updated the ADC Conversion Clock Period Block Diagram (see Figure 22-2).
Section 26.0 “Special Features”	Extensive updates were made to Section 26.2 “Watchdog Timer (WDT)” and Section 26.3 “On-Chip Voltage Regulator” .