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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx320f064ht-80v-pt

PIC32MX3XX/4XX

TABLE 3: PIN NAMES: PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F128L, AND PIC32MX360F512L DEVICES

Pin Number	Full Pin Name
A1	PMD4/RE4
A2	PMD3/RE3
A3	TRD0/RG13
A4	PMD0/RE0
A5	PMD8/RG0
A6	PMD10/RF1
A7	ENVREG
A8	Vss
A9	IC5/PMD12/RD12
A10	OC3/RD2
A11	OC2/RD1
B1	No Connect (NC)
B2	RG15
B3	PMD2/RE2
B4	PMD1/RE1
B5	TRD3/RA7
B6	PMD11/RF0
B7	VCAP/VCORE
B8	PMRD/CN14/RD5
B9	OC4/RD3
B10	Vss
B11	SOSCO/T1CK/CN0/RC14
C1	PMD6/RE6
C2	VDD
C3	TRD1/RG12
C4	TRD2/RG14
C5	TRCLK/RA6
C6	No Connect (NC)
C7	PMD15/CN16/RD7
C8	OC5/PMWR/CN13/RD4
C9	VDD
C10	SOSCI/CN1/RC13
C11	IC4/PMCS1/PMA14/RD11
D1	T2CK/RC1
D2	PMD7/RE7
D3	PMD5/RE5
D4	Vss
D5	Vss
D6	No Connect (NC)
D7	PMD14/CN15/RD6
D8	PMD13/CN19/RD13
D9	OC1/RD0
D10	No Connect (NC)
D11	IC3/PMCS2/PMA15/RD10
E1	T5CK/RC4
E2	T4CK/RC3
E3	SCK2/PMA5/CN8/RG6
E4	T3CK/RC2
E5	VDD
E6	PMD9/RG1
E7	Vss

Pin Number	Full Pin Name
E8	INT4/RA15
E9	RTCC/IC1/RD8
E10	IC2/RD9
E11	INT3/RA14
F1	MCLR
F2	SDO2/PMA3/CN10/RG8
F3	SS2/PMA2/CN11/RG9
F4	SDI2/PMA4/CN9/RG7
F5	Vss
F6	No Connect (NC)
F7	No Connect (NC)
F8	VDD
F9	OSC1/CLKI/RC12
F10	Vss
F11	OSC2/CLKO/RC15
G1	INT1/RE8
G2	INT2/RE9
G3	TMS/RA0
G4	No Connect (NC)
G5	VDD
G6	Vss
G7	Vss
G8	No Connect (NC)
G9	TDO/RA5
G10	SDA2/RA3
G11	TDI/RA4
H1	AN5/C1IN+/CN7/RB5
H2	AN4/C1IN-/CN6/RB4
H3	Vss
H4	VDD
H5	No Connect (NC)
H6	VDD
H7	No Connect (NC)
H8	SDI1/RF7
H9	SCK1/INT0/RF6
H10	SCL1/RG2
H11	SCL2/RA2
J1	AN3/C2IN+/CN5/RB3
J2	AN2/C2IN-/SS1/CN4/RB2
J3	PGED2/AN7/RB7
J4	AVDD
J5	AN11/PMA12/RB11
J6	TCK/RA1
J7	AN12/PMA11/RB12
J8	No Connect (NC)
J9	No Connect (NC)
J10	SDO1/RF8
J11	SDA1/RG3
K1	PGEC1/AN1/CN3/RB1
K2	PGED1/AN0/CN2/RB0
K3	VREF+/CVREF+/PMA6/RA10

Pin Diagrams (Continued)

121-Pin XBGA⁽¹⁾

● = Pins are up to 5V tolerant

PIC32MX440F128L
PIC32MX460F256L
PIC32MX460F512L

	1	2	3	4	5	6	7	8	9	10	11
A	● RE4	● RE3	● RG13	● RE0	● RG0	● RF1	○ ENVREG	○ Vss	● RD12	● RD2	● RD1
B	● NC	● RG15	● RE2	● RE1	● RA7	● RF0	○ Vcore/ VCAP	● RD5	● RD3	○ Vss	○ RC14
C	● RE6	○ VDD	● RG12	● RG14	● RA6	● NC	● RD7	● RD4	○ VDD	○ RC13	● RD11
D	● RC1	● RE7	● RE5	○ Vss	○ Vss	● NC	● RD6	● RD13	● RD0	● NC	● RD10
E	● RC4	● RC3	● RG6	● RC2	○ VDD	● RG1	○ Vss	● RA15	● RD8	● RD9	● RA14
F	● MCLR	● RG8	● RG9	● RG7	○ Vss	● NC	● NC	○ VDD	○ RC12	○ Vss	○ RC15
G	● RE8	● RE9	● RA0	● NC	○ VDD	○ Vss	○ Vss	● NC	● RA5	● RA3	● RA4
H	○ RB5	○ RB4	○ Vss	○ VDD	● NC	○ VDD	● NC	● VBUS	○ VUSB	● RG2	● RA2
J	○ RB3	○ RB2	○ RB7	○ AVDD	○ RB11	○ RA1	○ RB12	● NC	● NC	● RF8	○ RG3
K	○ RB1	○ RB0	○ RA10	○ RB8	● NC	● RF12	○ RB14	○ VDD	● RD15	● RF3	● RF2
L	○ RB6	○ RA9	○ AVss	○ RB9	○ RB10	● RF13	○ RB13	○ RB15	● RD14	● RF4	● RF5

Note 1: Refer to Table 4 for full pin names.

PIC32MX3XX/4XX

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number ⁽¹⁾			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
AN0	16	25	K2	I	Analog	Analog input channels.
AN1	15	24	K1	I	Analog	
AN2	14	23	J2	I	Analog	
AN3	13	22	J1	I	Analog	
AN4	12	21	H2	I	Analog	
AN5	11	20	H1	I	Analog	
AN6	17	26	L1	I	Analog	
AN7	18	27	J3	I	Analog	
AN8	21	32	K4	I	Analog	
AN9	22	33	L4	I	Analog	
AN10	23	34	L5	I	Analog	
AN11	24	35	J5	I	Analog	
AN12	27	41	J7	I	Analog	
AN13	28	42	L7	I	Analog	
AN14	29	43	K7	I	Analog	
AN15	30	44	L8	I	Analog	
CLKI	39	63	F9	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	40	64	F11	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	39	63	F9	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	40	64	F11	I/O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	47	73	C10	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	48	74	B11	O	—	32.768 kHz low-power oscillator crystal output.

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer

Analog = Analog input P = Power
O = Output I = Input

Note 1: Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

PIC32MX3XX/4XX

TABLE 3-2: COPROCESSOR 0 REGISTERS (CONTINUED)

Register Number	Register Name	Function
17-22	Reserved	Reserved
23	Debug ⁽²⁾	Debug control and exception status
24	DEPC ⁽²⁾	Program counter at last debug exception
25-29	Reserved	Reserved
30	ErrorEPC ⁽¹⁾	Program counter at last error
31	DESAVE ⁽²⁾	Debug handler scratchpad register

Note 1: Registers used in exception processing.

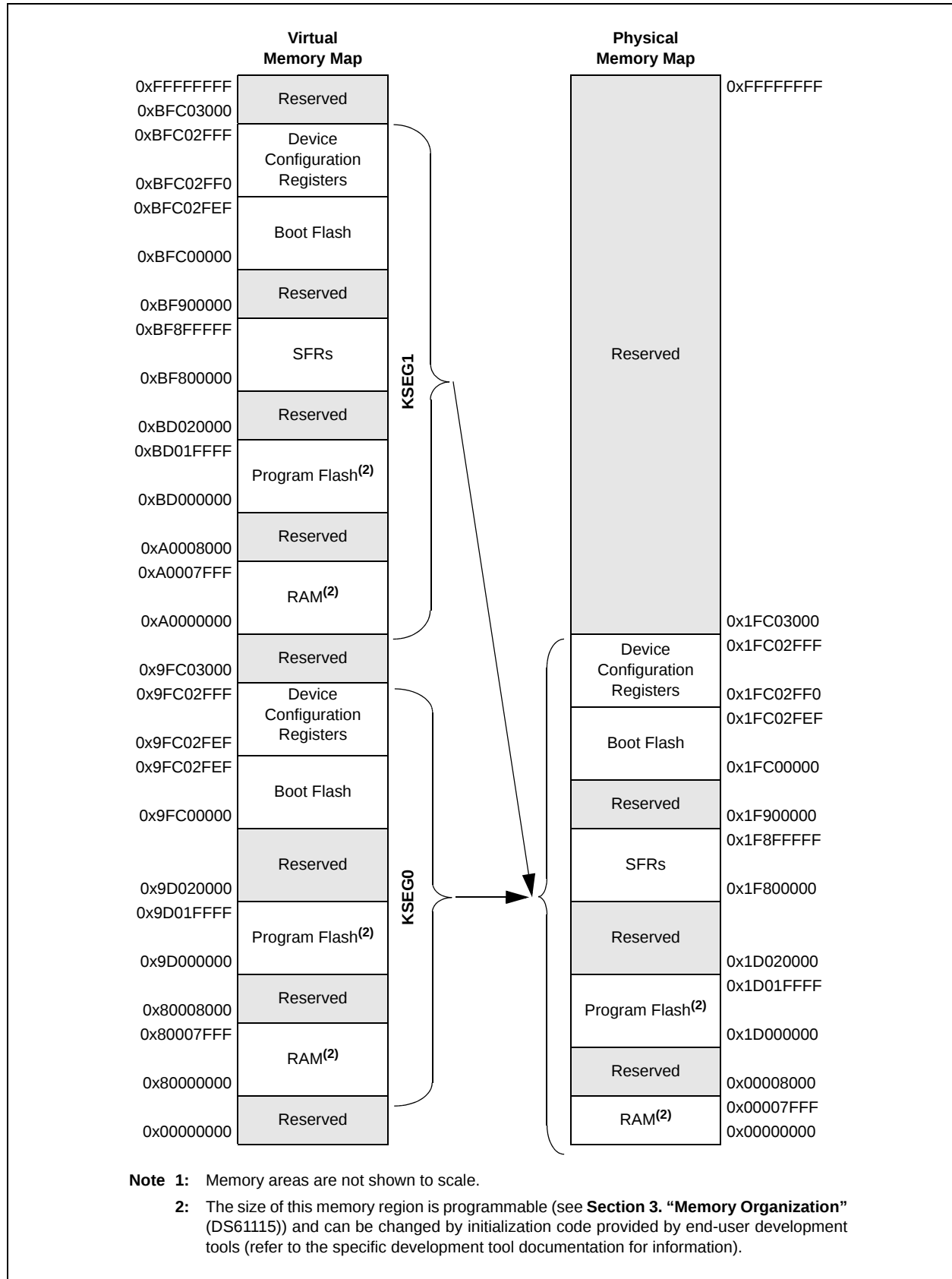
2: Registers used during debug.

Coprocessor 0 also contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including alignment errors in data, external events or program errors. Table 3-3 shows the exception types in order of priority.

TABLE 3-3: PIC32MX3XX/4XX FAMILY CORE EXCEPTION TYPES

Exception	Description
Reset	Assertion $\overline{\text{MCLR}}$ or a Power-on Reset (POR)
DSS	EJTAG Debug Single Step
DINT	EJTAG Debug Interrupt. Caused by the assertion of the external <i>EJ_DINT</i> input, or by setting the <i>EjtagBrk</i> bit in the ECR register
NMI	Assertion of NMI signal
Interrupt	Assertion of unmasked hardware or software interrupt signal
DIB	EJTAG debug hardware instruction break matched
AdEL	Fetch address alignment error Fetch reference to protected address
IBE	Instruction fetch bus error
DBp	EJTAG Breakpoint (execution of SDBBP instruction)
Sys	Execution of SYSCALL instruction
Bp	Execution of BREAK instruction
RI	Execution of a Reserved Instruction
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled
CEU	Execution of a CorExtend instruction when CorExtend is not enabled
Ov	Execution of an arithmetic instruction that overflowed
Tr	Execution of a trap (when trap condition is true)
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG Data Value Break on Store (address + value)
AdEL	Load address alignment error Load reference to protected address
AdES	Store address alignment error Store to protected address
DBE	Load or store bus error
DDBL	EJTAG data hardware breakpoint matched in load data compare

FIGURE 4-4: MEMORY MAP ON RESET FOR PIC32MX340F128H, PIC32MX340F128L, PIC32MX440F128H AND PIC32MX440F128L DEVICES⁽¹⁾



PIC32MX3XX/4XX

FIGURE 4-5: MEMORY MAP ON RESET FOR PIC32MX340F256H, PIC32MX360F256L, PIC32MX440F256H AND PIC32MX460F256L DEVICES⁽¹⁾

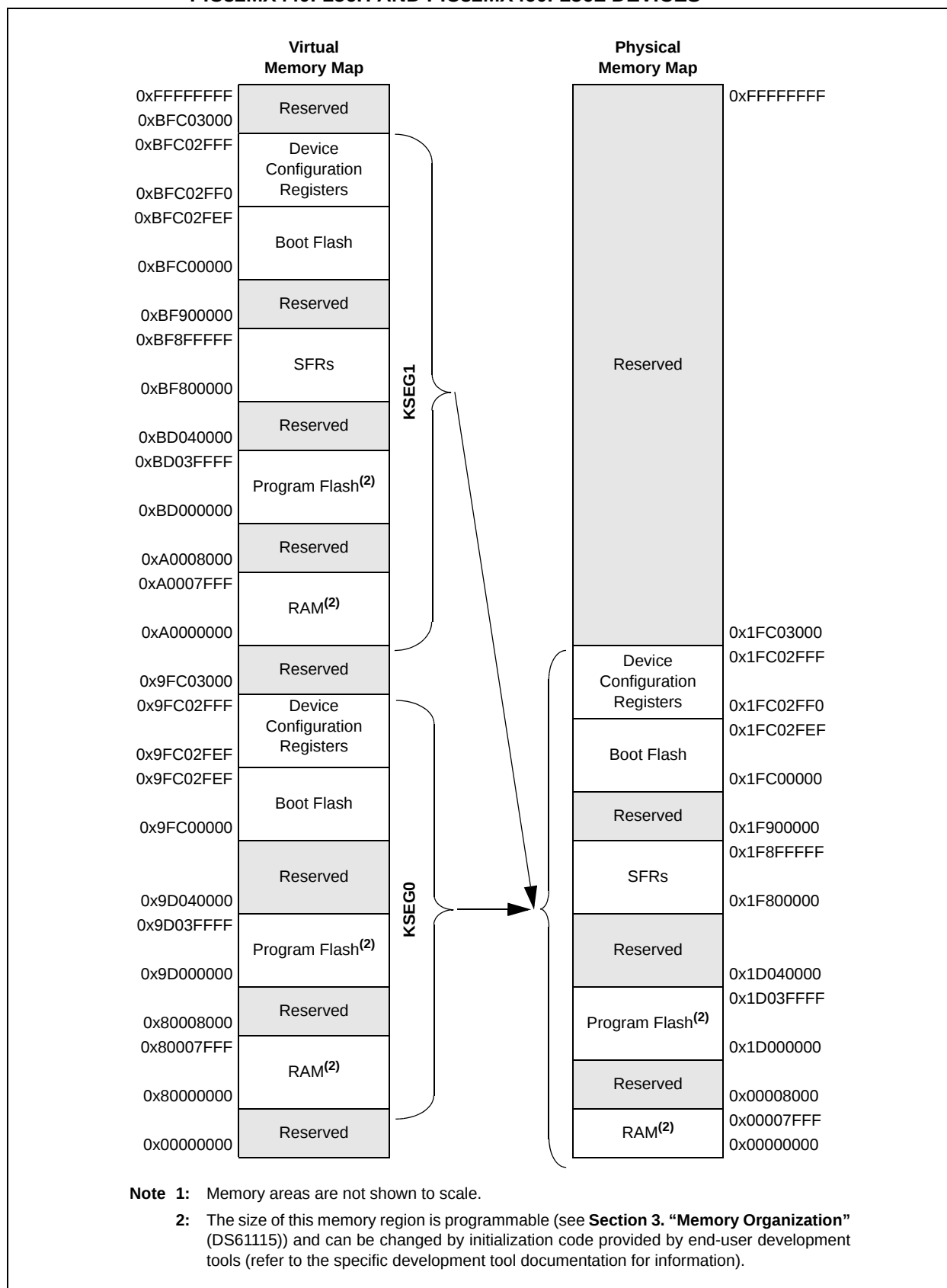


TABLE 4-14: DMA GLOBAL REGISTERS MAP FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	DMACON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	SUSPEND	—	—	—	—	—	—	—	—	—	—	—	—	0000
3010	DMASTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RDWR	—	DMACH<1:0>	—	0000
3020	DMAADDR	31:16	DMAADDR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 4-15: DMA CRC REGISTERS MAP FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY⁽¹⁾

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3030	DCRCCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	PLEN<3:0>				CRCEN	CRCAPP	—	—	—	—	CRCCH<1:0>		0000
3040	DCRCDATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DCRCDATA<15:0>																0000
3050	DCRCXOR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DCRCXOR<15:0>																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 4-29: PORTF REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L AND PIC32MX360F512L DEVICES ONLY⁽¹⁾

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6140	TRISF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	TRISF13	TRISF12	—	—	—	TRISF8	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	31FF
6150	PORTF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	RF13	RF12	—	—	—	RF8	RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
6160	LATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	LATF13	LATF12	—	—	—	LATF8	LATF7	LATF6	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
6170	ODCF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ODCF13	ODCF12	—	—	—	ODCF8	ODCF7	ODCF6	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 4-30: PORTF REGISTERS MAP FOR PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY⁽¹⁾

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6140	TRISF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	TRISF13	TRISF12	—	—	—	TRISF8	—	—	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	313F
6150	PORTF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	RF13	RF12	—	—	—	RF8	—	—	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
6160	LATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	LATF13	LATF12	—	—	—	LATF8	—	—	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
6170	ODCF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ODCF13	ODCF12	—	—	—	ODCF8	—	—	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 4-42: DEVICE AND REVISION ID SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F220	DEVID	31:16	VER<3:0>				DEVID<27:16>												xxxx
		15:0	DEVID<15:0>																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

PIC32MX3XX/4XX

NOTES:

PIC32MX3XX/4XX

NOTES:

25.0 POWER-SAVING FEATURES

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. “Power-Saving Features”** (DS61130) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

This section describes power-saving for the PIC32MX3XX/4XX. The PIC32MX devices offer a total of nine methods and modes that are organized into two categories that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

25.1 Power-Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the PBCLK, and by individually disabling modules. These methods are grouped into the following modes:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers.
- LPRC Run mode: the CPU is clocked from the LPRC clock source.
- Sosc Run mode: the CPU is clocked from the Sosc clock source.
- Peripheral Bus Scaling mode: peripherals are clocked at programmable fraction of the CPU clock (SYSCLK).

25.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which halt the clock to the CPU. These modes operate with all clock sources, as listed below:

- Posc Idle Mode: the system clock is derived from the Posc. The system clock source continues to operate.
Peripherals continue to operate, but can optionally be individually disabled.
- FRC Idle Mode: the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.
- Sosc Idle Mode: the system clock is derived from the Sosc. Peripherals continue to operate, but can optionally be individually disabled.

- LPRC Idle Mode: the system clock is derived from the LPRC.

Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.

- Sleep Mode: the CPU, the system clock source, and any peripherals that operate from the system clock source, are halted.

Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

25.3 Power-Saving Operation

The purpose of all power-saving is to reduce power consumption by reducing the device clock frequency. To achieve this, low-frequency clock sources can be selected. In addition, the peripherals and CPU can be halted or disabled to further reduce power consumption.

25.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device Power-Saving operating modes. The CPU and most peripherals are halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep mode.

Sleep mode includes the following characteristics:

- The CPU is halted.
- The system clock source is typically shut down. See **Section 25.3.2 “Idle Mode”** for specific information.
- There can be a wake-up delay based on the oscillator selection.
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode.
- The BOR circuit, if enabled, remains operative during Sleep mode.
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode.
- Some peripherals can continue to operate in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator, e.g., RTCC and Timer 1.
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep.
- The USB module can override the disabling of the Posc or FRC. Refer to **Section 11.0 “USB On-The-Go (OTG)”** for specific details.
- Some modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption.

28.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB C Compiler for Various Device Families
 - HI-TECH C for Various Device Families
 - MPASM™ Assembler
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
 - MPLAB ICD 3
 - PICKit™ 3 Debug Express
- Device Programmers
 - PICKit™ 2 Programmer
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

28.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
 - Simulator
 - Programmer (sold separately)
 - In-Circuit Emulator (sold separately)
 - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
 - Source files (C or assembly)
 - Mixed C and assembly
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

PIC32MX3XX/4XX

TABLE 29-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
DO10 DO16	VOL	Output Low Voltage I/O Ports	—	—	0.4	V	IO _L = 7 mA, V _{DD} = 3.6V
			—	—	0.4	V	IO _L = 6 mA, V _{DD} = 2.3V
		OSC2/CLKO	—	—	0.4	V	IO _L = 3.5 mA, V _{DD} = 3.6V
			—	—	0.4	V	IO _L = 2.5 mA, V _{DD} = 2.3V
DO20 DO26	VOH	Output High Voltage I/O Ports	2.4	—	—	V	IO _H = -12 mA, V _{DD} = 3.6V
			1.4	—	—	V	IO _H = -12 mA, V _{DD} = 2.3V
		OSC2/CLKO	2.4	—	—	V	IO _H = -12 mA, V _{DD} = 3.6V
			1.4	—	—	V	IO _H = -12 mA, V _{DD} = 2.3V

TABLE 29-10: ELECTRICAL CHARACTERISTICS: BROWN-OUT RESET (BOR)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
BO10	VBOR	BOR Event on V _{DD} transition high-to-low	2.0	—	2.3	V	—

PIC32MX3XX/4XX

TABLE 29-17: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
OS10	Fosc	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4	— —	50 ⁽³⁾ 50 ⁽⁵⁾	MHz MHz	EC (Note 5) ECPLL (Note 4)
OS11		Oscillator Crystal Frequency	3	—	10	MHz	XT (Note 5)
OS12			4	—	10	MHz	XTPLL (Notes 4, 5)
OS13			10	—	25	MHz	HS (Note 5)
OS14			10	—	25	MHz	HSPLL (Notes 4, 5)
OS15			32	32.768	100	kHz	Sosc (Note 5)
OS20	Tosc	Tosc = 1/Fosc = Tcy ⁽²⁾	—	—	—	—	See parameter OS10 for Fosc value
OS30	TosL, TosH	External Clock In (OSC1) High or Low Time	0.45 x Tosc	—	—	ns	EC (Note 5)
OS31	TosR, TosF	External Clock In (OSC1) Rise or Fall Time	—	—	0.05 x Tosc	ns	EC (Note 5)
OS40	TOST	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, XT, XTPLL and Sosc Clock Oscillator modes)	—	1024	—	Tosc	(Note 5)
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	(Note 5)
OS42	GM	External Oscillator Transconductance	—	12	—	mA/V	VDD = 3.3V TA = +25°C (Note 5)

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are characterized but are not tested.

- 2:** Instruction cycle period (Tcy) equals the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin.
- 3:** 40 MHz maximum for PIC32MX320F032H and PIC32MX420F032H devices.
- 4:** PLL input requirements: 4 MHz ≤F_{PLLIN} ≤5 MHz (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.
- 5:** This parameter is characterized, but not tested in manufacturing.

PIC32MX3XX/4XX

FIGURE 29-5: EXTERNAL RESET TIMING CHARACTERISTICS

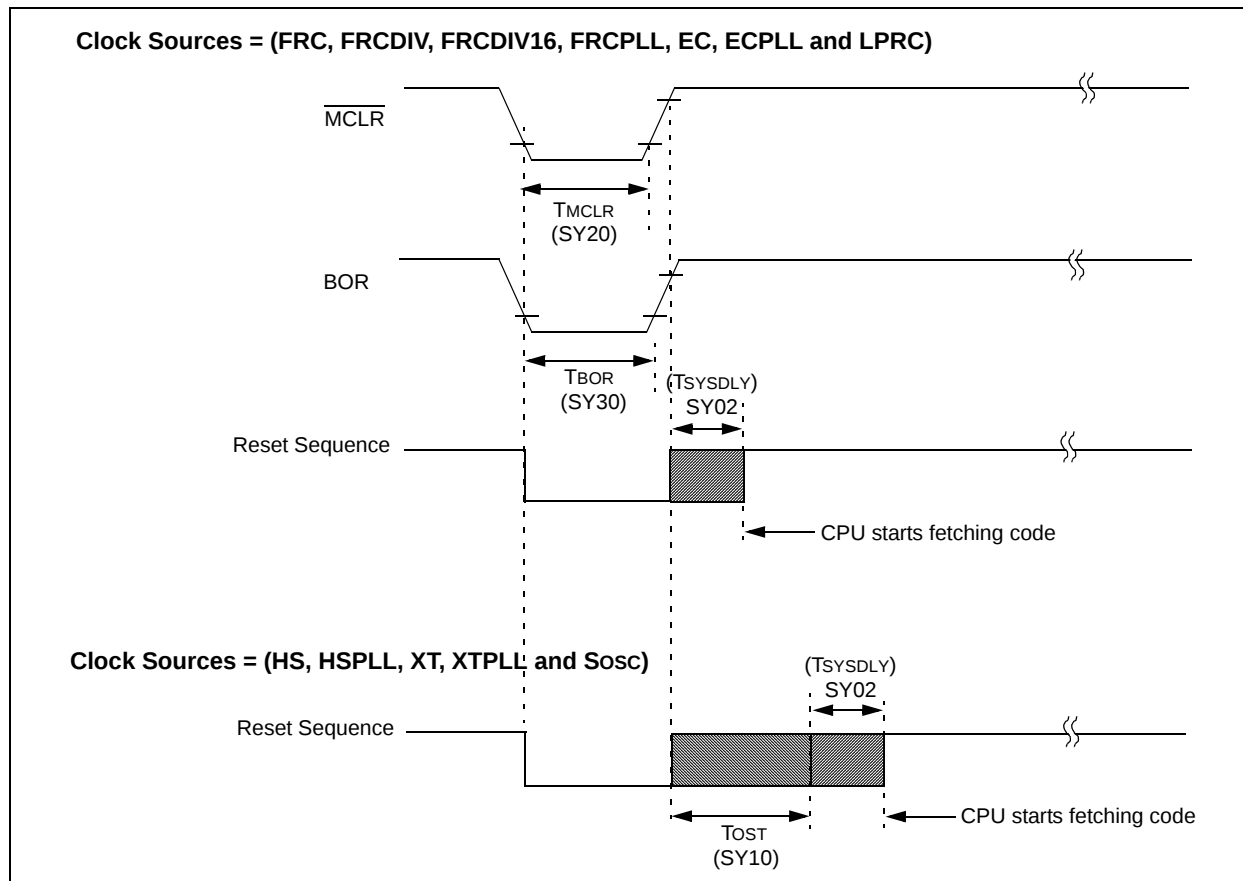


TABLE 29-22: RESETS TIMING

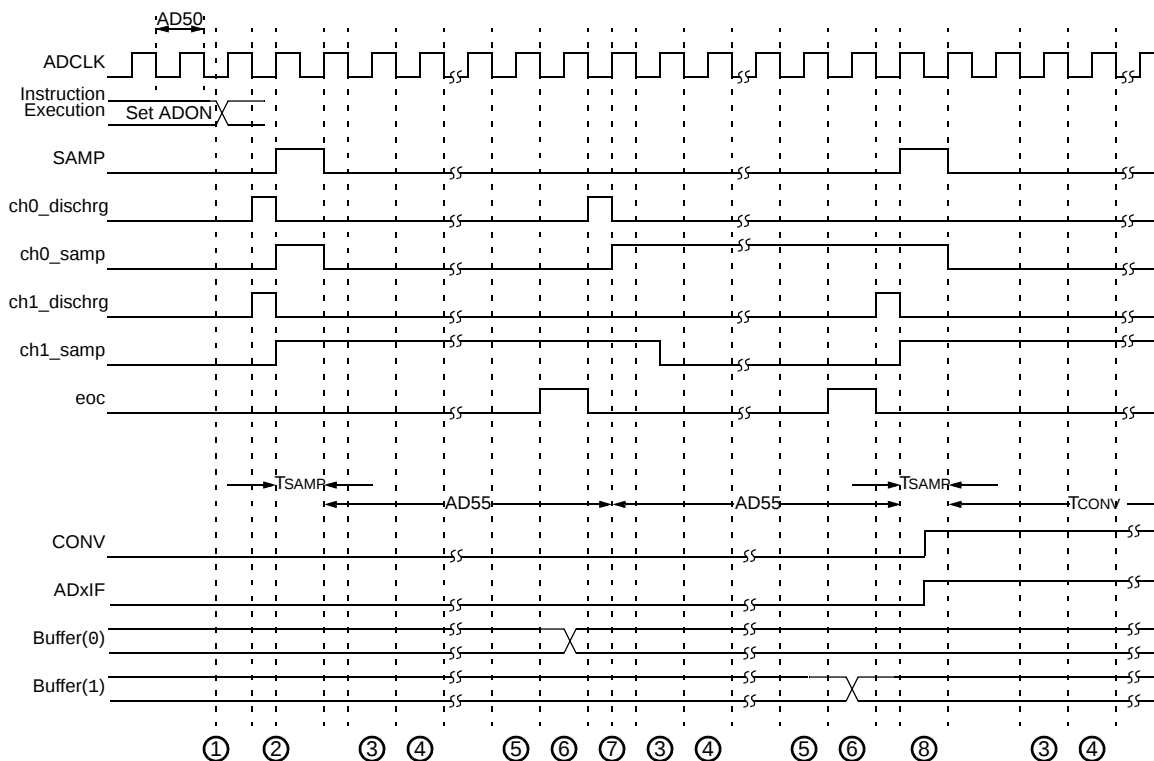
AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SY00	TPU	Power-up Period Internal Voltage Regulator Enabled	—	400	600	μs	-40°C to +85°C
SY01	TPWRT	Power-up Period External Vcore Applied (Power-Up-Timer Active)	48	64	80	ms	-40°C to +85°C
SY02	TSYSDLY	System Delay Period: Time required to reload Device Configuration Fuses plus SYSCLK delay before first instruction is fetched.	—	1 μs + 8 SYSCLK cycles	—	—	-40°C to +85°C
SY20	TMCLR	MCLR Pulse Width (low)	—	2	—	μs	-40°C to +85°C
SY30	TBOR	BOR Pulse Width (low)	—	1	—	μs	-40°C to +85°C

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.

PIC32MX3XX/4XX

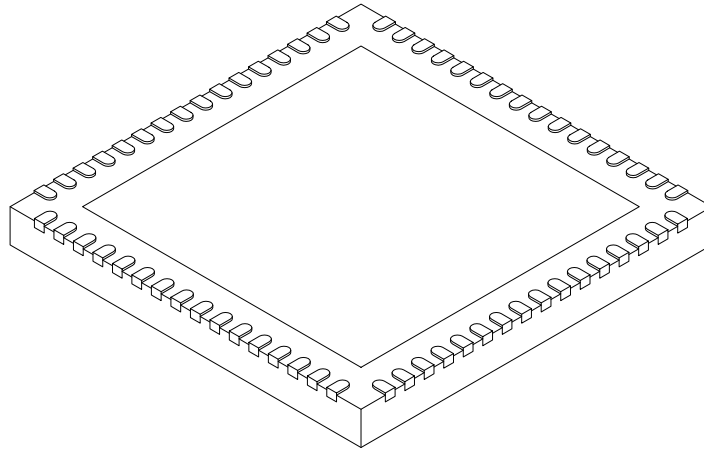
FIGURE 29-19: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS
(CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRC<2:0> = 111, SAMC<4:0> = 00001)



- ① – Software sets ADxCON. ADON to start AD operation.
- ② – Sampling starts after discharge period. TSAMP is described in **Section 17. “10-bit Analog-to-Digital Converter (ADC)”** (DS61104) of the “PIC32 Family Reference Manual”.
- ③ – Convert bit 9.
- ④ – Convert bit 8.
- ⑤ – Convert bit 0.
- ⑥ – One TAD for end of conversion.
- ⑦ – Begin conversion of next channel.
- ⑧ – Sample for time specified by SAMC<4:0>.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.15 x 7.15 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	64		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	9.00 BSC		
Exposed Pad Width	E2	7.05	7.15	7.50
Overall Length	D	9.00 BSC		
Exposed Pad Length	D2	7.05	7.15	7.50
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

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