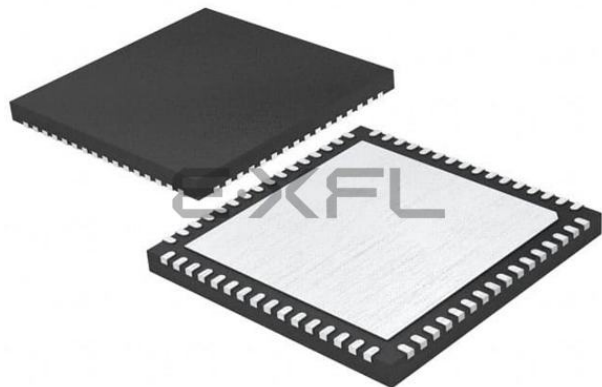




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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx320f128h-80i-mr

Pin Diagrams (Continued)

121-Pin XBGA⁽¹⁾

● = Pins are up to 5V tolerant

PIC32MX320F128L
PIC32MX340F128L
PIC32MX360F256L
PIC32MX360F512L

	1	2	3	4	5	6	7	8	9	10	11
A	● RE4	● RE3	● RG13	● RE0	● RG0	● RF1	○ ENVREG	○ Vss	● RD12	● RD2	● RD1
B	● NC	● RG15	● RE2	● RE1	● RA7	● RF0	○ Vcore/ VCAP	● RD5	● RD3	○ Vss	○ RC14
C	● RE6	○ VDD	● RG12	● RG14	● RA6	● NC	● RD7	● RD4	○ VDD	○ RC13	● RD11
D	● RC1	● RE7	● RE5	○ Vss	○ Vss	● NC	● RD6	● RD13	● RD0	● NC	● RD10
E	● RC4	● RC3	● RG6	● RC2	○ VDD	● RG1	○ Vss	● RA15	● RD8	● RD9	● RA14
F	● MCLR	● RG8	● RG9	● RG7	○ Vss	● NC	● NC	○ VDD	○ RC12	○ Vss	○ RC15
G	● RE8	● RE9	● RA0	● NC	○ VDD	○ Vss	○ Vss	● NC	● RA5	● RA3	● RA4
H	○ RB5	○ RB4	○ Vss	○ VDD	● NC	○ VDD	● NC	● RF7	● RF6	● RG2	● RA2
J	○ RB3	○ RB2	○ RB7	○ AVDD	○ RB11	○ RA1	○ RB12	● NC	● NC	● RF8	○ RG3
K	○ RB1	○ RB0	○ RA10	○ RB8	● NC	● RF12	○ RB14	○ VDD	● RD15	● RF3	● RF2
L	○ RB6	○ RA9	○ AVss	○ RB9	○ RB10	● RF13	○ RB13	○ RB15	● RD14	● RF4	● RF5

Note 1: Refer to Table 3 for full pin names.

PIC32MX3XX/4XX

TABLE 3: PIN NAMES: PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F128L, AND PIC32MX360F512L DEVICES

Pin Number	Full Pin Name
A1	PMD4/RE4
A2	PMD3/RE3
A3	TRD0/RG13
A4	PMD0/RE0
A5	PMD8/RG0
A6	PMD10/RF1
A7	ENVREG
A8	Vss
A9	IC5/PMD12/RD12
A10	OC3/RD2
A11	OC2/RD1
B1	No Connect (NC)
B2	RG15
B3	PMD2/RE2
B4	PMD1/RE1
B5	TRD3/RA7
B6	PMD11/RF0
B7	VCAP/VCORE
B8	PMRD/CN14/RD5
B9	OC4/RD3
B10	Vss
B11	SOSCO/T1CK/CN0/RC14
C1	PMD6/RE6
C2	VDD
C3	TRD1/RG12
C4	TRD2/RG14
C5	TRCLK/RA6
C6	No Connect (NC)
C7	PMD15/CN16/RD7
C8	OC5/PMWR/CN13/RD4
C9	VDD
C10	SOSCI/CN1/RC13
C11	IC4/PMCS1/PMA14/RD11
D1	T2CK/RC1
D2	PMD7/RE7
D3	PMD5/RE5
D4	Vss
D5	Vss
D6	No Connect (NC)
D7	PMD14/CN15/RD6
D8	PMD13/CN19/RD13
D9	OC1/RD0
D10	No Connect (NC)
D11	IC3/PMCS2/PMA15/RD10
E1	T5CK/RC4
E2	T4CK/RC3
E3	SCK2/PMA5/CN8/RG6
E4	T3CK/RC2
E5	VDD
E6	PMD9/RG1
E7	Vss

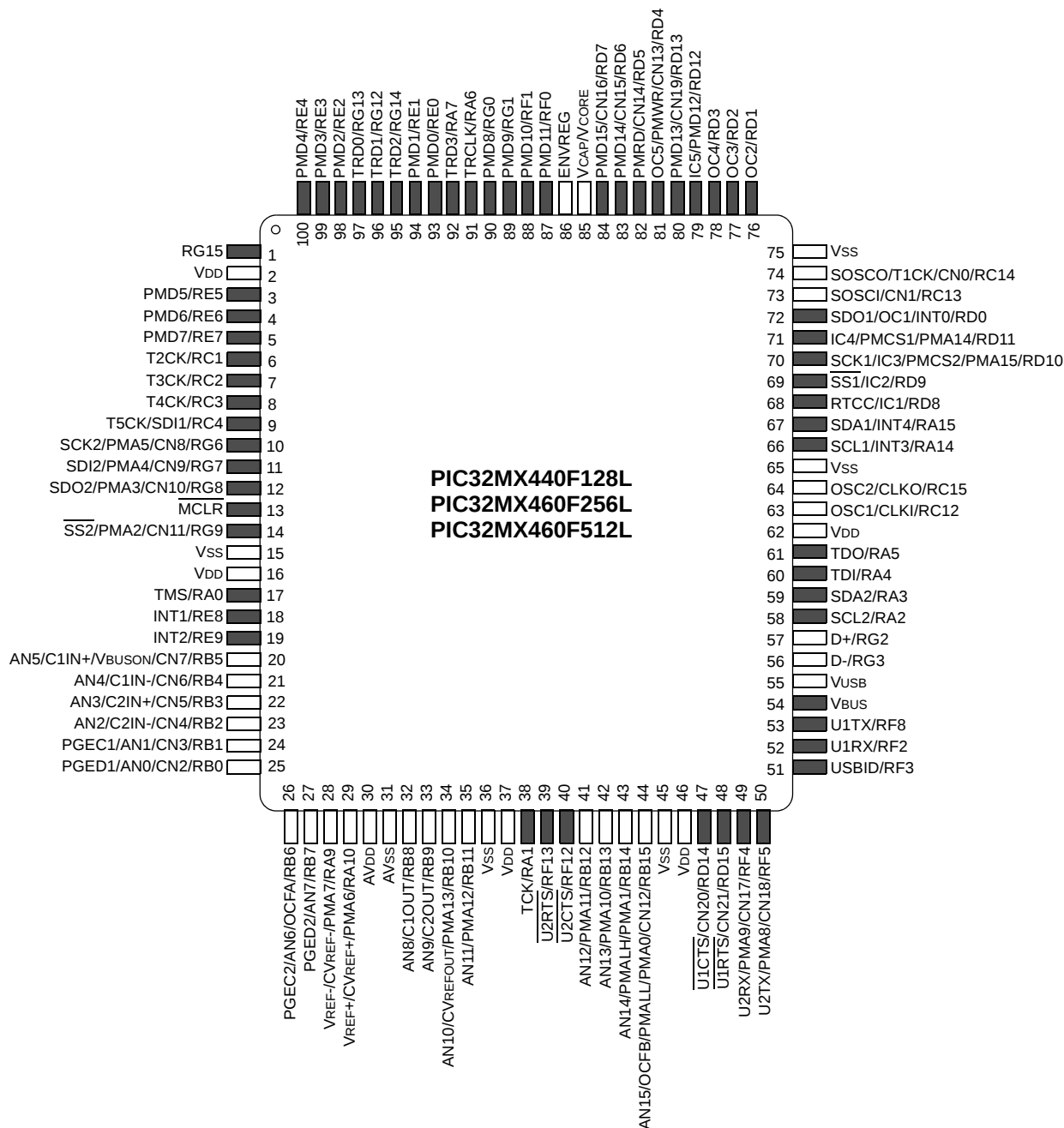
Pin Number	Full Pin Name
E8	INT4/RA15
E9	RTCC/IC1/RD8
E10	IC2/RD9
E11	INT3/RA14
F1	MCLR
F2	SDO2/PMA3/CN10/RG8
F3	SS2/PMA2/CN11/RG9
F4	SDI2/PMA4/CN9/RG7
F5	Vss
F6	No Connect (NC)
F7	No Connect (NC)
F8	VDD
F9	OSC1/CLKI/RC12
F10	Vss
F11	OSC2/CLKO/RC15
G1	INT1/RE8
G2	INT2/RE9
G3	TMS/RA0
G4	No Connect (NC)
G5	VDD
G6	Vss
G7	Vss
G8	No Connect (NC)
G9	TDO/RA5
G10	SDA2/RA3
G11	TDI/RA4
H1	AN5/C1IN+/CN7/RB5
H2	AN4/C1IN-/CN6/RB4
H3	Vss
H4	VDD
H5	No Connect (NC)
H6	VDD
H7	No Connect (NC)
H8	SDI1/RF7
H9	SCK1/INT0/RF6
H10	SCL1/RG2
H11	SCL2/RA2
J1	AN3/C2IN+/CN5/RB3
J2	AN2/C2IN-/SS1/CN4/RB2
J3	PGED2/AN7/RB7
J4	AVDD
J5	AN11/PMA12/RB11
J6	TCK/RA1
J7	AN12/PMA11/RB12
J8	No Connect (NC)
J9	No Connect (NC)
J10	SDO1/RF8
J11	SDA1/RG3
K1	PGEC1/AN1/CN3/RB1
K2	PGED1/AN0/CN2/RB0
K3	VREF+/CVREF+/PMA6/RA10

PIC32MX3XX/4XX

Pin Diagrams (Continued)

100-Pin TQFP (USB)

■ = Pins are up to 5V tolerant



4.0 MEMORY ORGANIZATION

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 3. “Memory Organization”** (DS61115) of the “*PIC32 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX3XX/4XX microcontrollers provide 4 GB of unified virtual memory address space. All memory regions including program, data memory, SFRs and Configuration registers reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX3XX/4XX to execute from data memory.

4.1 Key Features

- 32-bit native data width
- Separate User and Kernel mode address space
- Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable and non-cacheable address regions

4.2 PIC32MX3XX/4XX Memory Layout

PIC32MX3XX/4XX microcontrollers implement two address spaces: Virtual and Physical. All hardware resources such as program memory, data memory and peripherals are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by peripherals such as DMA and Flash controller that access memory independently of CPU.

PIC32MX3XX/4XX

FIGURE 4-5: MEMORY MAP ON RESET FOR PIC32MX340F256H, PIC32MX360F256L, PIC32MX440F256H AND PIC32MX460F256L DEVICES⁽¹⁾

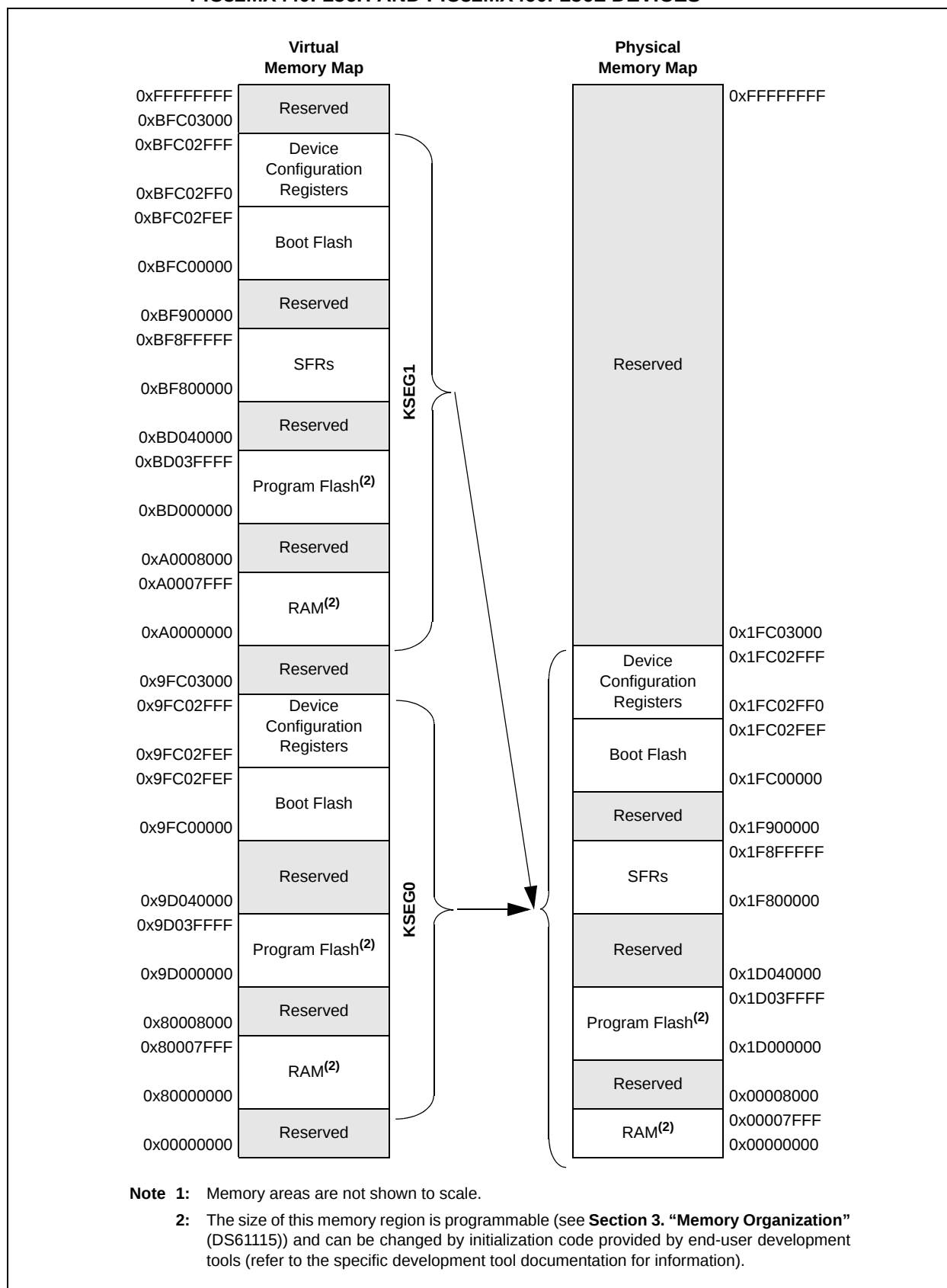


TABLE 4-1: BUS MATRIX REGISTERS MAP

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	BMX CON ⁽¹⁾	31:16	—	—	—	—	—	BMXCHEDMA	—	—	—	—	—	BMXERRIXI	BMXERRICD	BMXERRDMA	BMXERRDS	BMXERRIS	001F
		15:0	—	—	—	—	—	—	—	—	—	BMXWSDRM	—	—	—	BMXARB<2:0>			0042
2010	BMX DKPBA ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BMXDKPBA<15:0>																0000
2020	BMX DUDBA ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BMXDUDBA<15:0>																0000
2030	BMX DUPBA ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BMXDUPBA<15:0>																0000
2040	BMX DRMSZ	31:16	BMXDRMSZ<31:0>																xxxx
		15:0																	xxxx
2050	BMX PUPBA ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	BMXPUPBA<19:16>				0000
		15:0	BMXPUPBA<15:0>																0000
2060	BMX PFMSZ	31:16	BMXPFMSZ<31:0>																xxxx
		15:0																	xxxx
2070	BMX BOOTSZ	31:16	BMXBOOTSZ<31:0>																0000
		15:0																	3000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 4-12: SPI1-2 REGISTERS MAP^(1,2)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5800	SPI1CON	31:16	FRMEN	FRMSYNC	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	SPIFE	—	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	—	—	—	—	0000
5810	SPI1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	SPIBUSY	—	—	—	—	SPIROV	—	—	SPITBE	—	—	SPIRBF	0008
5820	SPI1BUF	31:16	DATA<31:0>																0000
		15:0																	0000
5830	SPI1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	BRG<8:0>										
5A00	SPI2CON	31:16	FRMEN	FRMSYNC	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	SPIFE	—	0008
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	—	—	—	—	0000
5A10	SPI2STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	SPIBUSY	—	—	—	—	SPIROV	—	—	SPITBE	—	—	SPIRBF	0008
5A20	SPI2BUF	31:16	DATA<31:0>																0000
		15:0																	0000
5A30	SPI2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	BRG<8:0>										

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** All registers in this table except SPIxBUF have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.
- Note 2:** SPI2 Module is not present on PIC32MX420FXXXX/440FXXXX devices.

PIC32MX3XX/4XX

NOTES:

10.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. “Direct Memory Access (DMA) Controller”** (DS61117) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

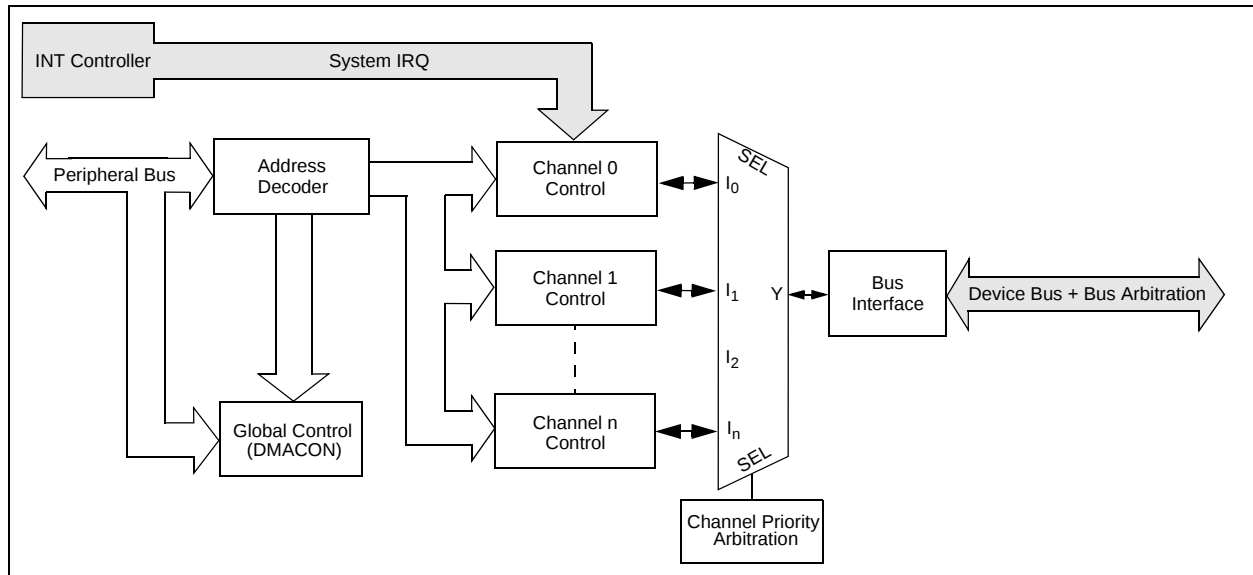
The PIC32MX Direct Memory Access (DMA) controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the PIC32MX (such as Peripheral Bus (PBUS) devices: SPI, UART, PMP, and so on) or memory itself.

Following are some of the key features of the DMA controller module:

- Four Identical Channels, each featuring:
 - Auto-Increment Source and Destination Address Registers
 - Source and Destination Pointers
 - Memory to Memory and Memory to Peripheral Transfers

- Automatic Word-Size Detection:
 - Transfer Granularity, down to byte level
 - Bytes need not be word-aligned at source and destination
- Fixed Priority Channel Arbitration
- Flexible DMA Channel Operating Modes:
 - Manual (software) or automatic (interrupt) DMA requests
 - One-Shot or Auto-Repeat Block Transfer modes
 - Channel-to-channel chaining
- Flexible DMA Requests:
 - A DMA request can be selected from any of the peripheral interrupt sources
 - Each channel can select any (appropriate) observable interrupt as its DMA request source
 - A DMA transfer abort can be selected from any of the peripheral interrupt sources
 - Pattern (data) match transfer termination
- Multiple DMA Channel Status Interrupts:
 - DMA channel block transfer complete
 - Source empty or half empty
 - Destination full or half-full
 - DMA transfer aborted due to an external event
 - Invalid DMA address generated
- DMA Debug Support Features:
 - Most recent address accessed by a DMA channel
 - Most recent DMA channel to transfer data
- CRC Generation Module:
 - CRC module can be assigned to any of the available channels
 - CRC module is highly configurable

FIGURE 10-1: DMA BLOCK DIAGRAM



13.0 TIMER1

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. “Timers”** (DS61105) of the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

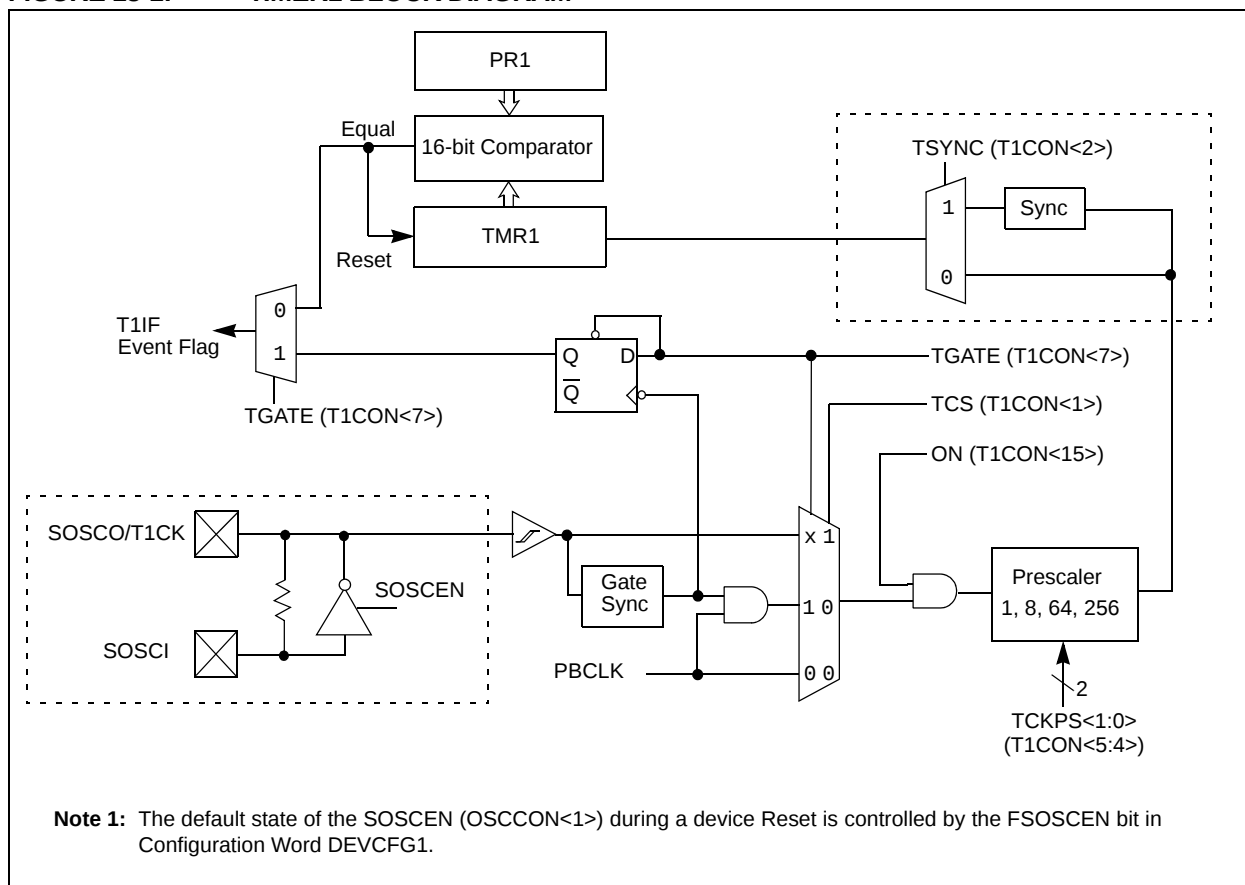
This family of PIC32MX devices features one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the Secondary Oscillator (Sosc) for real-time clock applications. The following modes are supported:

- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

13.1 Additional Supported Features

- Selectable clock prescaler
- Timer operation during CPU Idle and Sleep mode
- Fast bit manipulation using CLR, SET and INV registers
- Asynchronous mode can be used with the Sosc to function as a Real-Time Clock (RTC)

FIGURE 13-1: TIMER1 BLOCK DIAGRAM⁽¹⁾



PIC32MX3XX/4XX

NOTES:

PIC32MX3XX/4XX

NOTES:

26.2 Watchdog Timer (WDT)

This section describes the operation of the WDT and Power-Up Timer of the PIC32MX3XX/4XX.

The WDT, when enabled, operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are some of the key features of the WDT module:

- Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle

FIGURE 26-1: WATCHDOG AND POWER-UP TIMER BLOCK DIAGRAM

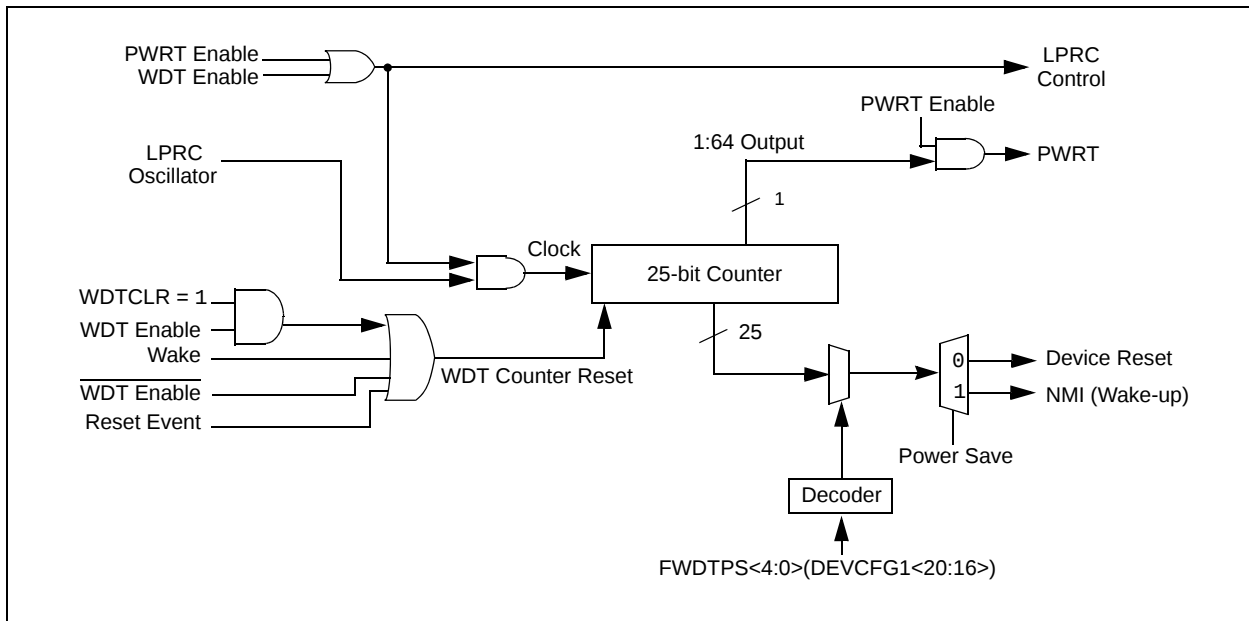


TABLE 27-1: MIPS32® INSTRUCTION SET (CONTINUED)

Instruction	Description	Function
JAL	Jump and Link	$GPR[31] = PC + 8$ $PC = PC[31:28] \parallel offset \ll 2$
JALR	Jump and Link Register	$Rd = PC + 8$ $PC = Rs$
JALR.HB	Jump and Link Register with Hazard Barrier	Like JALR, but also clears execution and instruction hazards
JR	Jump Register	$PC = Rs$
JR.HB	Jump Register with Hazard Barrier	Like JR, but also clears execution and instruction hazards
LB	Load Byte	$Rt = (\text{byte})Mem[Rs+offset]$
LBU	Unsigned Load Byte	$Rt = (\text{ubyte})Mem[Rs+offset]$
LH	Load Halfword	$Rt = (\text{half})Mem[Rs+offset]$
LHU	Unsigned Load Halfword	$Rt = (\text{uhalf})Mem[Rs+offset]$
LL	Load Linked Word	$Rt = Mem[Rs+offset]$ $LL_{bit} = 1$ $LLAdr = Rs + offset$
LUI	Load Upper Immediate	$Rt = \text{immediate} \ll 16$
LW	Load Word	$Rt = Mem[Rs+offset]$
LWPC	Load Word, PC relative	$Rt = Mem[PC+offset]$
LWL	Load Word Left	$Re = Re \text{ MERGE } Mem[Rs+offset]$
LWR	Load Word Right	$Re = Re \text{ MERGE } Mem[Rs+offset]$
MADD	Multiply-Add	$HI \mid LO += (\text{int})Rs * (\text{int})Rt$
MADDU	Multiply-Add Unsigned	$HI \mid LO += (\text{uns})Rs * (\text{uns})Rt$
MFC0	Move from Coprocessor 0	$Rt = CPR[0, Rd, sel]$
MFHI	Move from HI	$Rd = HI$
MFLO	Move from LO	$Rd = LO$
MOVN	Move Conditional on Not Zero	if $Rt \neq 0$ then $Rd = Rs$
MOVZ	Move Conditional on Zero	if $Rt = 0$ then $Rd = Rs$
MSUB	Multiply-Subtract	$HI \mid LO -= (\text{int})Rs * (\text{int})Rt$
MSUBU	Multiply-Subtract Unsigned	$HI \mid LO -= (\text{uns})Rs * (\text{uns})Rt$
MTC0	Move to Coprocessor 0	$CPR[0, n, Sel] = Rt$
MTHI	Move to HI	$HI = Rs$
MTLO	Move to LO	$LO = Rs$
MUL	Multiply with register write	$HI \mid LO = \text{Unpredictable}$ $Rd = ((\text{int})Rs * (\text{int})Rt)_{31..0}$
MULT	Integer Multiply	$HI \mid LO = (\text{int})Rs * (\text{int})Rd$
MULTU	Unsigned Multiply	$HI \mid LO = (\text{uns})Rs * (\text{uns})Rd$
NOP	No Operation (Assembler idiom for: SLL r0, r0, r0)	
NOR	Logical NOR	$Rd = \sim(Rs \mid Rt)$
OR	Logical OR	$Rd = Rs \mid Rt$
ORI	Logical OR Immediate	$Rt = Rs \mid \text{Immed}$
RDHWR	Read Hardware Register (if enabled by HWRE _{na} Register)	$Re = HWR[Rd]$

Note 1: This instruction is deprecated and should not be used.

PIC32MX3XX/4XX

TABLE 29-6: DC CHARACTERISTICS: IDLE CURRENT (IDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp			
Parameter No.	Typical ⁽²⁾	Max.	Units	Conditions		
Idle Current (IDLE): Core OFF, Clock ON Base Current (Note 1)						
DC30	—	5	mA	-40°C, +25°C, +85°C	2.3V	4 MHz
DC30a	1.4	—	mA	-40°C, +25°C, +85°C	—	
DC30b	—	5	mA	-40°C, +25°C, +85°C	3.6V	
DC30c	—	8	mA	+105°C		
DC31	—	15	mA	-40°C, +25°C, +85°C	2.3V	20 MHz (Note 3)
DC31a	13	—	mA	-40°C, +25°C, +85°C	—	
DC31b	—	17	mA	-40°C, +25°C, +85°C	3.6V	
DC31c	—	25	mA	+105°C		
DC32	—	22	mA	-40°C, +25°C, +85°C	2.3V	60 MHz (Note 3)
DC32a	20	—	mA	-40°C, +25°C, +85°C	—	
DC32b	—	25	mA	-40°C, +25°C, +85°C	3.6V	
DC32c	—	32	mA	+105°C		
DC33	—	29	mA	-40°C, +25°C, +85°C	2.3V	80 MHz
DC33a	24	—	mA	-40°C, +25°C, +85°C	—	
DC33b	—	32	mA	-40°C, +25°C, +85°C	3.6V	
DC33c	—	40	mA	+105°C		
DC34	—	36	μA	-40°C	2.3V	LPRC (31 kHz) (Note 3)
DC34a	—	62	μA	+25°C		
DC34b	—	392	μA	+85°C		
DC34c	—	550	μA	+105°C		
DC35	35	—	μA	-40°C	3.3V	
DC35a	65	—	μA	+25°C		
DC35b	242	—	μA	+85°C		
DC35c	350	—	μA	+105°C		
DC36	—	43	μA	-40°C	3.6V	
DC36a	—	106	μA	+25°C		
DC36b	—	414	μA	+85°C		
DC36c	—	600	μA	+105°C		

Note 1: The test conditions for base IDLE current measurements are as follows: System clock is enabled and PBCLK divisor = 1:8. CPU in Idle mode (CPU core halted). Only digital peripheral modules are enabled (ON bit = 1) and being clocked. WDT and FSCM are disabled. All I/O pins are configured as inputs and pulled to Vss. MCLR = VDD.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: This parameter is characterized, but not tested in manufacturing.

PIC32MX3XX/4XX

TABLE 29-17: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
OS10	Fosc	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4	— —	50 ⁽³⁾ 50 ⁽⁵⁾	MHz MHz	EC (Note 5) ECPLL (Note 4)
OS11		Oscillator Crystal Frequency	3	—	10	MHz	XT (Note 5)
OS12			4	—	10	MHz	XTPLL (Notes 4, 5)
OS13			10	—	25	MHz	HS (Note 5)
OS14			10	—	25	MHz	HSPLL (Notes 4, 5)
OS15			32	32.768	100	kHz	Sosc (Note 5)
OS20	Tosc	Tosc = 1/Fosc = Tcy ⁽²⁾	—	—	—	—	See parameter OS10 for Fosc value
OS30	TosL, TosH	External Clock In (OSC1) High or Low Time	0.45 x Tosc	—	—	ns	EC (Note 5)
OS31	TosR, TosF	External Clock In (OSC1) Rise or Fall Time	—	—	0.05 x Tosc	ns	EC (Note 5)
OS40	TOST	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, XT, XTPLL and Sosc Clock Oscillator modes)	—	1024	—	Tosc	(Note 5)
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	(Note 5)
OS42	GM	External Oscillator Transconductance	—	12	—	mA/V	VDD = 3.3V TA = +25°C (Note 5)

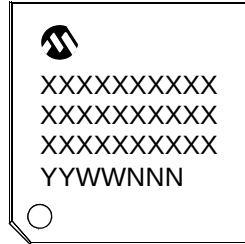
Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are characterized but are not tested.

- 2:** Instruction cycle period (Tcy) equals the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin.
- 3:** 40 MHz maximum for PIC32MX320F032H and PIC32MX420F032H devices.
- 4:** PLL input requirements: 4 MHz ≤ F_{PLLIN} ≤ 5 MHz (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.
- 5:** This parameter is characterized, but not tested in manufacturing.

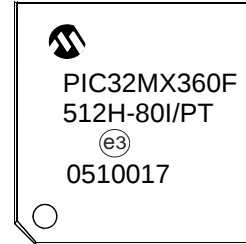
30.0 PACKAGING INFORMATION

30.1 Package Marking Information

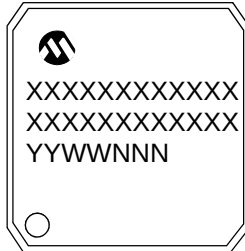
64-Lead TQFP (10x10x1 mm)



Example



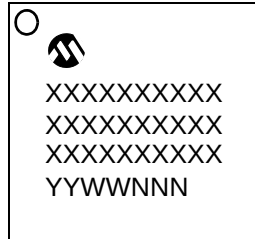
100-Lead TQFP (12x12x1 mm)



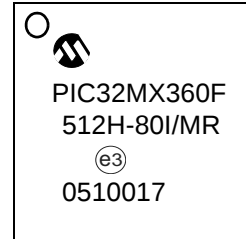
Example



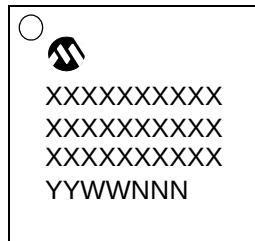
64-Lead QFN (9x9x0.9 mm)



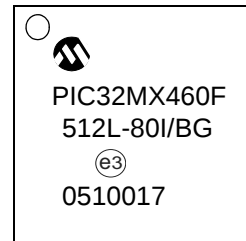
Example



121-Lead XBGA (10x10x1.1 mm)



Example

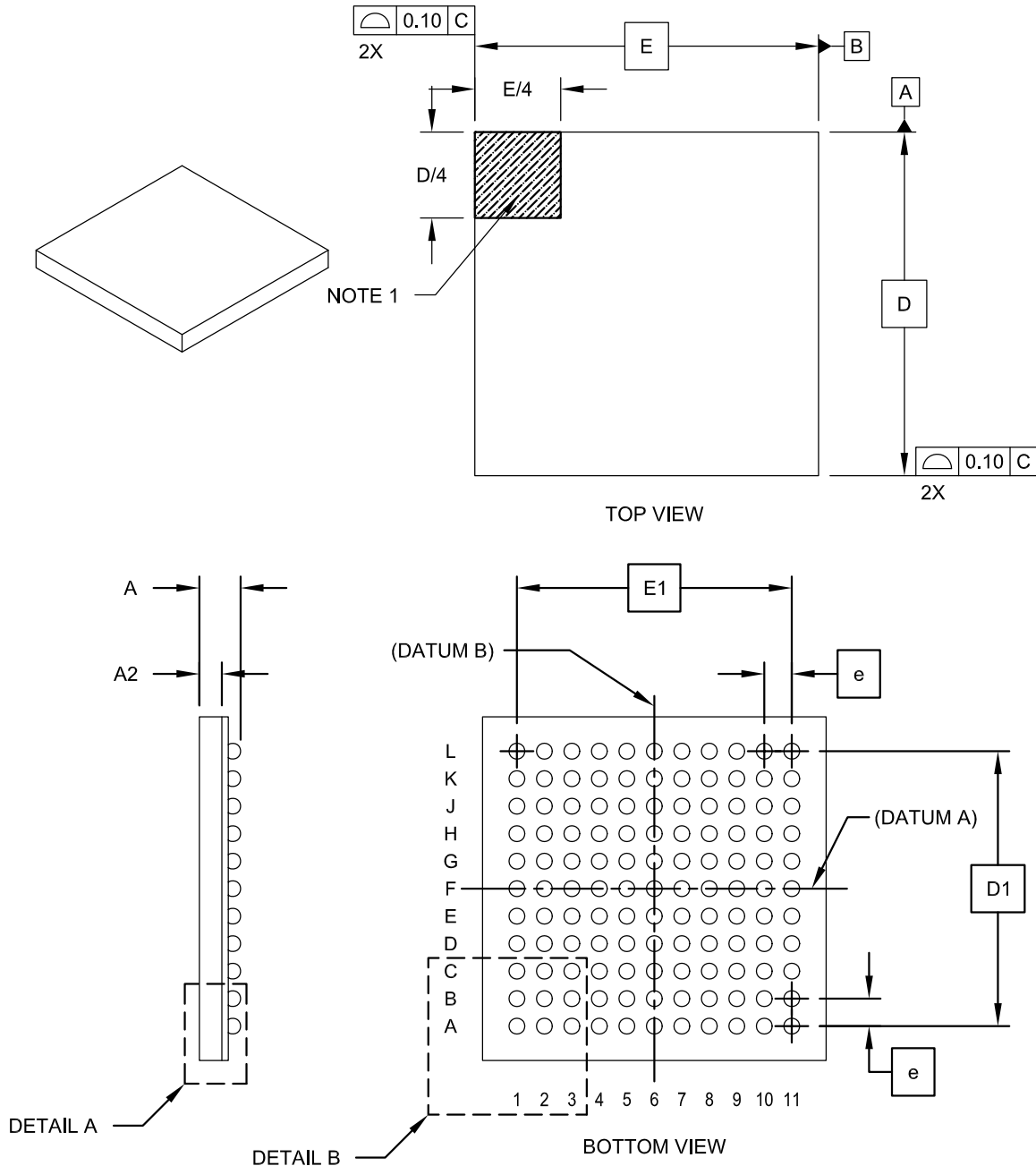


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [XBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-148B Sheet 1 of 2

PIC32MX3XX/4XX

W

Watchdog Timer

Operation	137
WWW Address.....	209
WWW, On-Line Support.....	19

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