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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	-
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx320f128l-80v-bg">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx320f128l-80v-bg</a>

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number <sup>(1)</sup>			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
PGED2	18	27	J3	I/O	ST	Data I/O pin for programming/debugging communication channel 2.
PGEC2	17	26	L1	I	ST	Clock input pin for programming/debugging communication channel 2.
$\overline{\text{MCLR}}$	7	13	F1	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	19	30	J4	P	P	Positive supply for analog modules. This pin must be connected at all times.
AVSS	20	31	L3	P	P	Ground reference for analog modules.
VDD	10, 26, 38	2, 16, 37, 46, 62	C2, C9, E5, F8, G5, H4, H6, K8	P	—	Positive supply for peripheral logic and I/O pins.
VCORE/ VCAP	56	85	B7	P	—	Capacitor for Internal Voltage Regulator.
Vss	9, 25, 41	15, 36, 45, 65, 75	A8, B10, D4, D5, E7, F10, F5, G6, G7, H3	P	—	Ground reference for logic and I/O pins.
VREF+	16	29	K3	I	Analog	Analog voltage reference (high) input.
VREF-	15	28	L2	I	Analog	Analog voltage reference (low) input.

**Legend:** CMOS = CMOS compatible input or output      Analog = Analog input      P = Power  
 ST = Schmitt Trigger input with CMOS levels      O = Output      I = Input  
 TTL = TTL input buffer

**Note 1:** Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

# PIC32MX3XX/4XX

**FIGURE 4-1: MEMORY MAP ON RESET FOR PIC32MX320F032H AND PIC32MX420F032H DEVICES<sup>(1)</sup>**

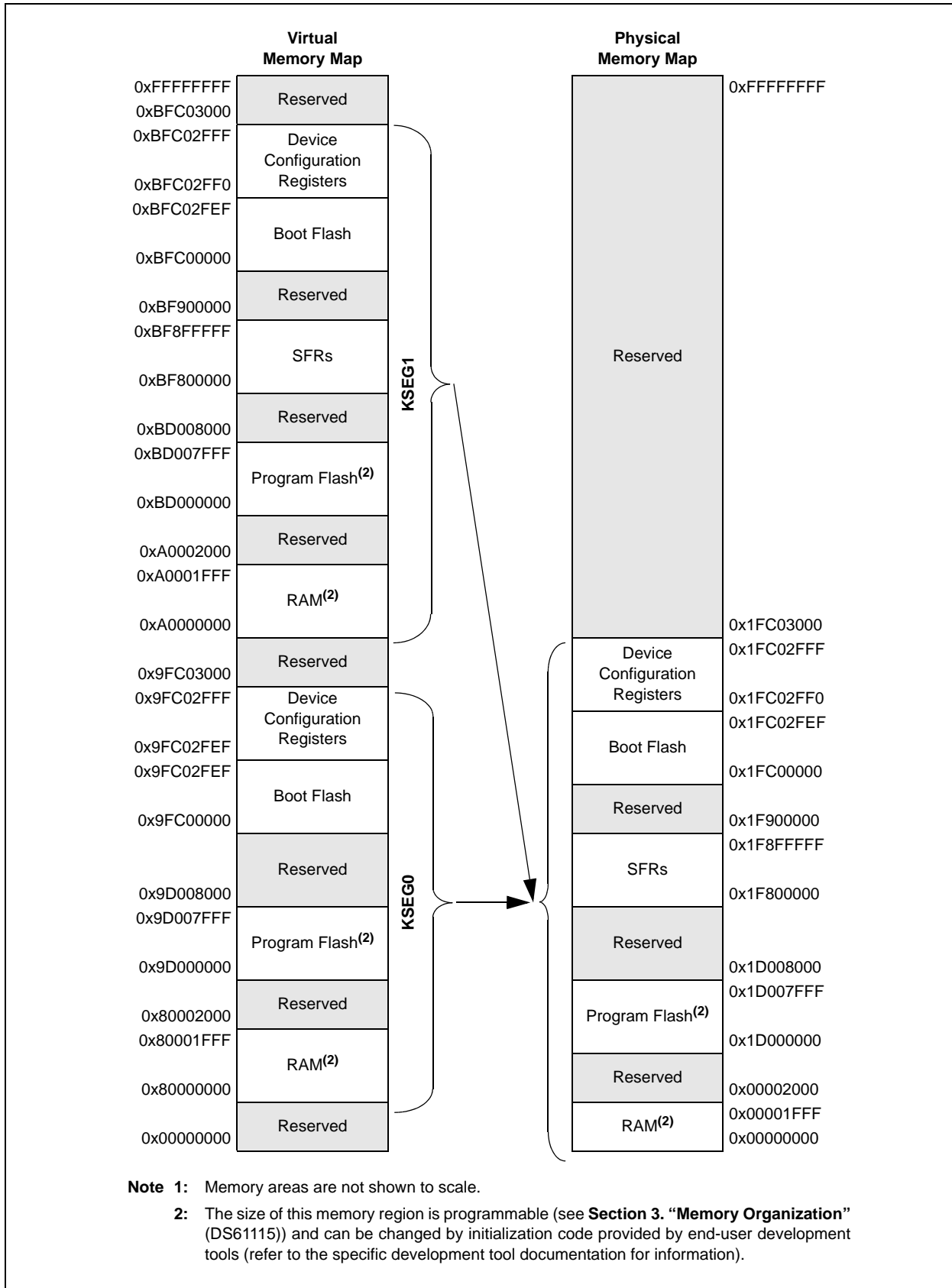


TABLE 4-10: I2C1-2 REGISTERS MAP<sup>(1)</sup>

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
5000	I2C1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
5010	I2C1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	—	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF
5020	I2C1ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5030	I2C1MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5040	I2C1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5050	I2C1TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5260	I2C1RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5200	I2C2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
5210	I2C2STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	—	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF
5220	I2C2ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5230	I2C2MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5240	I2C2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5250	I2C2TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5260	I2C2RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table except I2CxRCV have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**TABLE 4-14: DMA GLOBAL REGISTERS MAP FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY**

Virtual Address (BF88_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
3000	DMACON <sup>(1)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	SUSPEND	—	—	—	—	—	—	—	—	—	—	—	—	—
3010	DMASTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RDWR	—	DMACH<1:0>	—	0000
3020	DMAADDR	31:16	DMAADDR<31:0>															0000	
		15:0																0000	

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 “CLR, SET and INV Registers” for more information.

**TABLE 4-15: DMA CRC REGISTERS MAP FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY<sup>(1)</sup>**

Virtual Address (BF88_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
3030	DCRCCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	PLEN<3:0>				CRCEN	CRCAPP	—	—	—	—	—	—	0000
3040	DCRCDATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DCRCDATA<15:0>															0000	
3050	DCRCXOR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DCRCXOR<15:0>															0000	

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 “CLR, SET and INV Registers” for more information.

**TABLE 4-25: PORTD REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L, PIC32MX360F512L, PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY<sup>(1)</sup>**

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
60C0	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FFFF
60D0	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxxx
60E0	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxxx
60F0	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

**TABLE 4-26: PORTD REGISTERS MAP FOR PIC32MX320F032H, PIC32MX320F064H, PIC32MX320F128H, PIC32MX340F128H, PIC32MX340F256H, PIC32MX340F512H, PIC32MX420F032H, PIC32MX440F128H, PIC32MX440F256H AND PIC32MX440F512H DEVICES ONLY<sup>(1)</sup>**

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
60C0	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	0FFF
60D0	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxxx
60E0	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxxx
60F0	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

**TABLE 4-43: USB REGISTERS MAP<sup>(1)</sup>**

Virtual Address (BF88.#)	Register Name	Bit Range	Bits																All Resets		
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0			
5040	U1OTG IR <sup>(2)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF	0000	
5050	U1OTG IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE	0000	
5060	U1OTG STAT <sup>(3)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD	0000	
5070	U1OTG CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000	
5080	U1PWRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	UACTPND <sup>(4)</sup>	—	—	USLPGRD	—	—	USUSPEND	USBPWR	0000	
5200	U1IR <sup>(2)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF	0000	
5210	U1IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE	0000	
5220	U1EIR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF	EOFEF	PIDEF	0000
5230	U1EIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE	EOFEE	PIDEE	0000
5240	U1STAT <sup>(3)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	ENDPT<3:0> <sup>(4)</sup>					DIR	PPBI	—	—	0000
5250	U1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	JSTATE <sup>(4)</sup>	SE0 <sup>(4)</sup>	PKTDIS	USBRST	HOSTEN	RESUME	PPBRST	USBEN	0000	
5260	U1ADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	LSPDEN	DEVADDR<6:0>								0000
5270	U1BDTP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	BDTPTRL<7:1>								—	0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 “CLR, SET and INV Registers” for more information.
- 2:** This register does not have associated CLR, SET, and INV registers.
- 3:** All bits in this register are read-only; therefore, CLR, SET, and INV registers are not supported.
- 4:** The reset value for this bit is undefined.

**TABLE 7-1: INTERRUPT IRQ AND VECTOR LOCATION (CONTINUED)**

Interrupt Source <sup>(1)</sup>	IRQ	Vector Number	Interrupt Bit Location			
			Flag	Enable	Priority	Subpriority
Highest Natural Order Priority						
SPI2E – SPI2 Fault	37	31	IFS1<5>	IEC1<5>	IPC7<28:26>	IPC7<25:24>
SPI2TX – SPI2 Transfer Done	38	31	IFS1<6>	IEC1<6>	IPC7<28:26>	IPC7<25:24>
SPI2RX – SPI2 Receive Done	39	31	IFS1<7>	IEC1<7>	IPC7<28:26>	IPC7<25:24>
U2E – UART2 Error	40	32	IFS1<8>	IEC1<8>	IPC8<4:2>	IPC8<1:0>
U2RX – UART2 Receiver	41	32	IFS1<9>	IEC1<9>	IPC8<4:2>	IPC8<1:0>
U2TX – UART2 Transmitter	42	32	IFS1<10>	IEC1<10>	IPC8<4:2>	IPC8<1:0>
I2C2B – I2C2 Bus Collision Event	43	33	IFS1<11>	IEC1<11>	IPC8<12:10>	IPC8<9:8>
I2C2S – I2C2 Slave Event	44	33	IFS1<12>	IEC1<12>	IPC8<12:10>	IPC8<9:8>
I2C2M – I2C2 Master Event	45	33	IFS1<13>	IEC1<13>	IPC8<12:10>	IPC8<9:8>
FSCM – Fail-Safe Clock Monitor	46	34	IFS1<14>	IEC1<14>	IPC8<20:18>	IPC8<17:16>
RTCC – Real-Time Clock and Calendar	47	35	IFS1<15>	IEC1<15>	IPC8<28:26>	IPC8<25:24>
DMA0 – DMA Channel 0	48	36	IFS1<16>	IEC1<16>	IPC9<4:2>	IPC9<1:0>
DMA1 – DMA Channel 1	49	37	IFS1<17>	IEC1<17>	IPC9<12:10>	IPC9<9:8>
DMA2 – DMA Channel 2	50	38	IFS1<18>	IEC1<18>	IPC9<20:18>	IPC9<17:16>
DMA3 – DMA Channel 3	51	39	IFS1<19>	IEC1<19>	IPC9<28:26>	IPC9<25:24>
FCE – Flash Control Event	56	44	IFS1<24>	IEC1<24>	IPC11<4:2>	IPC11<1:0>
USB	57	45	IFS1<25>	IEC1<25>	IPC11<12:10>	IPC11<9:8>
Lowest Natural Order Priority						

**Note 1:** Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MX General Purpose – Features”** and **TABLE 2: “PIC32MX USB – Features”** for available peripherals.



## 26.0 SPECIAL FEATURES

**Note:** This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. “Watchdog Timer and Power-up Timer”** (DS61114), **Section 32. “Configuration”** (DS61124) and **Section 33. “Programming and Diagnostics”** (DS61129) of the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site ([www.microchip.com/PIC32](http://www.microchip.com/PIC32)).

PIC32MX3XX/4XX devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. These are:

- Flexible Device Configuration
- Watchdog Timer
- JTAG Interface
- In-Circuit Serial Programming™ (ICSP™)

### 26.1 Configuration Bits

The Configuration bits can be programmed to select various device configurations.

**REGISTER 26-1: DEVCFG0: DEVICE CONFIGURATION WORD 0**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-0	r-1	r-1	R/P	r-1	r-1	r-1	R/P
	—	—	—	CP	—	—	—	BWP
23:16	r-1	r-1	r-1	r-1	R/P	R/P	R/P	R/P
	—	—	—	—	PWP<7:4>			
15:8	R/P	R/P	R/P	R/P	r-1	r-1	r-1	r-1
	PWP<3:0>				—	—	—	—
7:0	r-1	r-1	r-1	r-1	R/P	r-1	R/P	R/P
	—	—	—	—	ICSEL	—	DEBUG<1:0>	

**Legend:**

R = Readable bit                      W = Writable bit                      P = Programmable bit                      r = Reserved bit  
 U = Unimplemented bit                      -n = Bit Value at POR: ('0', '1', x = Unknown)

- bit 31     **Reserved:** Write '0'
- bit 30-29 **Reserved:** Write '1'
- bit 28     **CP:** Code-Protect bit  
 Prevents boot and program Flash memory from being read or modified by an external programming device.  
 1 = Protection disabled  
 0 = Protection enabled
- bit 27-25 **Reserved:** Write '1'
- bit 24     **BWP:** Boot Flash Write-Protect bit  
 Prevents boot Flash memory from being modified during code execution.  
 1 = Boot Flash is writable  
 0 = Boot Flash is not writable
- bit 23-20 **Reserved:** Write '1'

**REGISTER 26-2: DEVCFG1: DEVICE CONFIGURATION WORD 1**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	R/P	r-1	r-1	R/P	R/P	R/P	R/P	R/P
	FWDTEN	—	—	WDTPS<4:0>				
15:8	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P
	IESO	—	FSOSCEN	—	—	FNOSC<2:0>		

**Legend:**

R = Readable bit                      W = Writable bit                      P = Programmable bit                      r = Reserved bit  
 U = Unimplemented bit                      -n = Bit Value at POR: ('0', '1', x = Unknown)

bit 31-24 **Reserved:** Write '1'

bit 23 **FWDTEN:** Watchdog Timer Enable bit

1 = The WDT is enabled and cannot be disabled by software  
 0 = The WDT is not enabled; it can be enabled in software

bit 22-21 **Reserved:** Write '1'

bit 20-16 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits

- 10100 = 1:1048576
- 10011 = 1:524288
- 10010 = 1:262144
- 10001 = 1:131072
- 10000 = 1:65536
- 01111 = 1:32768
- 01110 = 1:16384
- 01101 = 1:8192
- 01100 = 1:4096
- 01011 = 1:2048
- 01010 = 1:1024
- 01001 = 1:512
- 01000 = 1:256
- 00111 = 1:128
- 00110 = 1:64
- 00101 = 1:32
- 00100 = 1:16
- 00011 = 1:8
- 00010 = 1:4
- 00001 = 1:2
- 00000 = 1:1

All other combinations not shown result in operation = '10100'

bit 15-14 **FCKSM<1:0>:** Clock Switching and Monitor Selection Configuration bits

- 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
- 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
- 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

**Note 1:** Do not disable Posc (POSCMOD = 00) when using this oscillator source.

**REGISTER 26-3: DEVCFG2: DEVICE CONFIGURATION WORD 2**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —
23:16	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	R/P FPLL0DIV<2:0>	R/P FPLL1DIV<2:0>	R/P FPLL2DIV<2:0>
15:8	R/P UPLLEN	r-1 —	r-1 —	r-1 —	r-1 —	R/P UPLL0DIV<2:0>	R/P UPLL1DIV<2:0>	R/P UPLL2DIV<2:0>
7:0	r-1 —	R/P FPLLMUL<2:0>	R/P FPLLMUL<2:0>	R/P FPLLMUL<2:0>	r-1 —	R/P FPLLIDIV<2:0>	R/P FPLLIDIV<2:0>	R/P FPLLIDIV<2:0>

**Legend:**

R = Readable bit                      W = Writable bit                      P = Programmable bit                      r = Reserved bit  
 U = Unimplemented bit                      -n = Bit Value at POR: ('0', '1', x = Unknown)

bit 31-19 **Reserved:** Write '1'

bit 18-16 **FPLL0DIV<2:0>:** Default Postscaler for PLL bits

- 111 = PLL output divided by 256
- 110 = PLL output divided by 64
- 101 = PLL output divided by 32
- 100 = PLL output divided by 16
- 011 = PLL output divided by 8
- 010 = PLL output divided by 4
- 001 = PLL output divided by 2
- 000 = PLL output divided by 1

bit 15 **UPLLEN:** USB PLL Enable bit  
 1 = Disable and bypass USB PLL  
 0 = Enable USB PLL

bit 14-11 **Reserved:** Write '1'

bit 10-8 **UPLL0DIV<2:0>:** PLL Input Divider bits

- 111 = 12x divider
- 110 = 10x divider
- 101 = 6x divider
- 100 = 5x divider
- 011 = 4x divider
- 010 = 3x divider
- 010 = 3x divider
- 001 = 2x divider
- 000 = 1x divider

bit 7 **Reserved:** Write '1'

bit 6-4 **FPLLMUL<2:0>:** PLL Multiplier bits

- 111 = 24x multiplier
- 110 = 21x multiplier
- 101 = 20x multiplier
- 100 = 19x multiplier
- 011 = 18x multiplier
- 010 = 17x multiplier
- 001 = 16x multiplier
- 000 = 15x multiplier

bit 3 **Reserved:** Write '1'

bit 2-0 **FPLLIDIV<2:0>:** PLL Input Divider bits

- 111 = 12x divider
- 110 = 10x divider
- 101 = 6x divider
- 100 = 5x divider
- 011 = 4x divider
- 010 = 3x divider
- 001 = 2x divider
- 000 = 1x divider

**TABLE 27-1: MIPS32® INSTRUCTION SET (CONTINUED)**

Instruction	Description	Function
TGE	Trap if Greater Than or Equal	if (int)Rs >= (int)Rt TrapException
TGEI	Trap if Greater Than or Equal Immediate	if (int)Rs >= (int)Immed TrapException
TGEIU	Trap if Greater Than or Equal Immediate Unsigned	if (uns)Rs >= (uns)Immed TrapException
TGEU	Trap if Greater Than or Equal Unsigned	if (uns)Rs >= (uns)Rt TrapException
TLT	Trap if Less Than	if (int)Rs < (int)Rt TrapException
TLTI	Trap if Less Than Immediate	if (int)Rs < (int)Immed TrapException
TLTIU	Trap if Less Than Immediate Unsigned	if (uns)Rs < (uns)Immed TrapException
TLTU	Trap if Less Than Unsigned	if (uns)Rs < (uns)Rt TrapException
TNE	Trap if Not Equal	if Rs != Rt TrapException
TNEI	Trap if Not Equal Immediate	if Rs != (int)Immed TrapException
WAIT	Wait for Interrupt	Go to a low power mode and stall until interrupt occurs
WRPGPR	Write to GPR in Previous Shadow Set	SGPR[SRSCtl <sub>PSS</sub> , Rd] = Rt
WSBH	Word Swap Bytes Within Halfwords	Rd = Rt <sub>23..16</sub>    Rt <sub>31..24</sub>    Rt <sub>7..0</sub>    Rt <sub>15..8</sub>
XOR	Exclusive OR	Rd = Rs ^ Rt
XORI	Exclusive OR Immediate	Rt = Rs ^ (uns)Immed

**Note 1:** This instruction is deprecated and should not be used.

**TABLE 29-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	Typical <sup>(3)</sup>	Max.	Units	Conditions			
<b>Operating Current (IDD)<sup>(1,2)</sup></b>							
DC20	8.5	13	mA	Code executing from Flash	-40°C, +25°C, +85°C	—	4 MHz
	9	15			+105°C		
DC20c	4.0	—	mA	Code executing from SRAM	—	—	—
DC21	23.5	32	mA	Code executing from Flash	—	—	20 MHz <b>(Note 4)</b>
DC21c	16.4	—	mA	Code executing from SRAM			
DC22	48	61	mA	Code executing from Flash	—	—	60 MHz <b>(Note 4)</b>
DC22c	45	—	mA	Code executing from SRAM			
DC23	55	75	mA	Code executing from Flash	-40°C, +25°C, +85°C	2.3V	80 MHz
	60	100			+105°C		
DC23c	55	—	mA	Code executing from SRAM	—	—	—
DC24	—	100	μA	—	-40°C	2.3V	LPRC (31 kHz) <b>(Note 4)</b>
DC24a	—	130	μA	—	+25°C		
DC24b	—	670	μA	—	+85°C		
DC24c	—	850	μA	—	+105°C		
DC25	94	—	μA	—	-40°C	3.3V	
DC25a	125	—	μA	—	+25°C		
DC25b	302	—	μA	—	+85°C		
DC25d	400	—	μA	—	+105°C		
DC25c	71	—	μA	Code executing from SRAM	—	—	
DC26	—	110	μA	—	-40°C	3.6V	
DC26a	—	180	μA	—	+25°C		
DC26b	—	700	μA	—	+85°C		
DC26c	—	900	μA	—	+105°C		

**Note 1:** A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type as well as temperature can have an impact on the current consumption.

**2:** The test conditions for IDD measurements are as follows: Oscillator mode = EC+PLL with OSC1 driven by external square wave from rail to rail and PBCLK divisor = 1:8. CPU, Program Flash and SRAM data memory are operational, Program Flash memory Wait states = 7, program cache and prefetch are disabled and SRAM data memory Wait states = 1. All peripheral modules are disabled (ON bit = 0). WDT and FSCM are disabled. All I/O pins are configured as inputs and pulled to VSS. MCLR = VDD.

**3:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

**4:** This parameter is characterized, but not tested in manufacturing.

**TABLE 29-11: DC CHARACTERISTICS: PROGRAM MEMORY<sup>(3)</sup>**

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical <sup>(1)</sup>	Max.	Units	Conditions
<b>Program Flash Memory</b>							
D130	EP	Cell Endurance	1000	—	—	E/W	—
D131	VPR	VDD for Read	V <sub>MIN</sub>	—	3.6	V	—
D132	VPEW	VDD for Erase or Write	3.0	—	3.6	V	—
D134	TRETD	Characteristic Retention	20	—	—	Year	—
D135	IDDP	Supply Current during Programming	—	10	—	mA	—
	TWW	Word Write Cycle Time	20	—	40	μs	—
D136	TRW	Row Write Cycle Time <sup>(2)</sup> (128 words per row)	3	4.5	—	ms	—
D137	TPE	Page Erase Cycle Time	20	—	—	ms	—
	TCE	Chip Erase Cycle Time	80	—	—	ms	—
D138	LVDstartup	Flash LVD Delay	—	—	6	μs	—

**Note 1:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated.

**2:** The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

**3:** Refer to the “PIC32MX Flash Programming Specification” (DS61145) for operating conditions during programming and erase cycles.

**TABLE 29-12: PROGRAM FLASH MEMORY WAIT STATE CHARACTERISTICS**

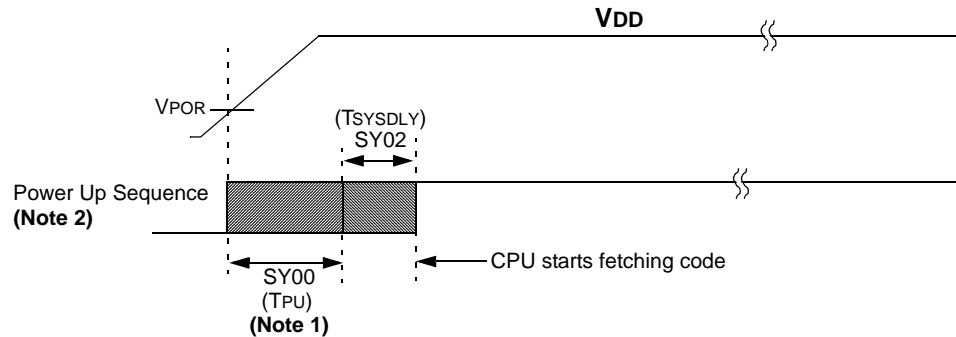
DC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp		
Required Flash wait states	SYSCLK	Units	Comments	
0 Wait State	0 to 30	MHz	—	
1 Wait State	31 to 60			
2 Wait States	61 to 80			

**Note 1:** 40 MHz maximum for PIC32MX320F032H and PIC32MX420F032H devices.

**FIGURE 29-4: POWER-ON RESET TIMING CHARACTERISTICS**

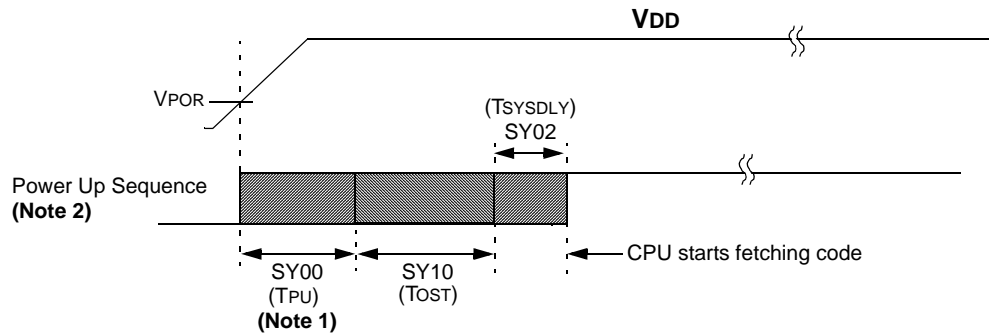
**Internal Voltage Regulator Enabled**

**Clock Sources = (FRC, FRCDIV, FRCDIV16, FRCPLL, EC, ECPLL and LPRC)**



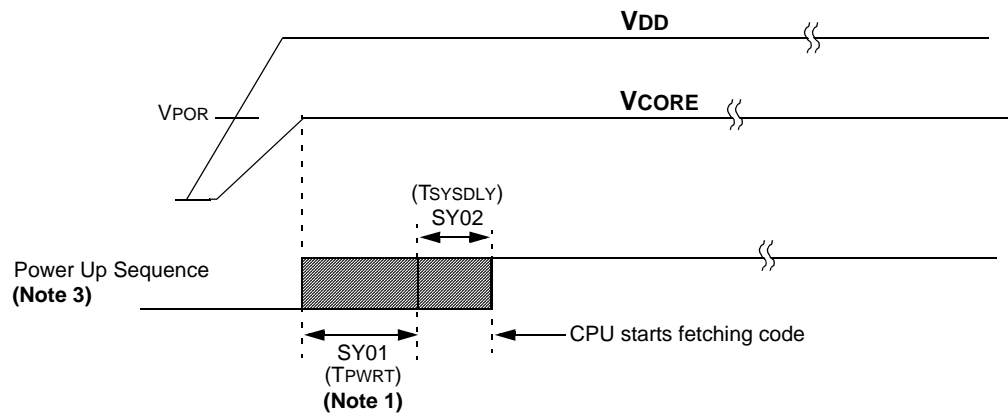
**Internal Voltage Regulator Enabled**

**Clock Sources = (HS, HSPLL, XT, XTPLL and Sosc)**



**External V<sub>CORE</sub> Provided**

**Clock Sources = (FRC, FRCDIV, FRCDIV16, FRCPLL, EC, ECPLL and LPRC)**



- Note 1:** The Power-up period will be extended if the power-up sequence completes before the device exits from BOR ( $V_{DD} < V_{DDMIN}$ ).
- 2:** Includes interval voltage regulator stabilization delay.
- 3:** Power-up Timer (PWRT); only active when the internal voltage regulator is disabled.

# PIC32MX3XX/4XX

**TABLE 29-24: TIMER2, 3, 4, 5 EXTERNAL CLOCK TIMING REQUIREMENTS**

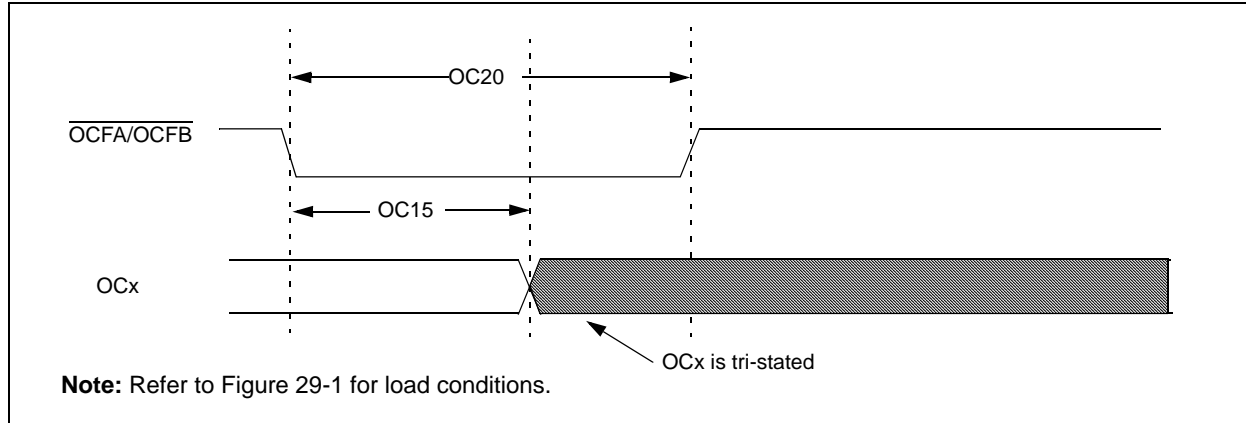
AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp					
Param. No.	Symbol	Characteristics <sup>(1)</sup>	Min.	Max.	Units	Conditions		
TB10	TtXH	TxCK High Time	Synchronous, with prescaler	$[(12.5 \text{ ns or } 1\text{TPB})/N] + 25 \text{ ns}$	—	ns	Must also meet parameter TB15.	N = prescale value (1, 2, 4, 8, 16, 32, 64, 256)
TB11	TtXL	TxCK Low Time	Synchronous, with prescaler	$[(12.5 \text{ ns or } 1\text{TPB})/N] + 25 \text{ ns}$	—	ns	Must also meet parameter TB15.	
TB15	TtXP	TxCK Input Period	Synchronous, with prescaler	$[(\text{Greater of } 25 \text{ ns or } 2 \text{ TPB})/N] + 30 \text{ ns}$	—	ns	VDD > 2.7V	
				$[(\text{Greater of } 25 \text{ ns or } 2 \text{ TPB})/N] + 50 \text{ ns}$	—	ns	VDD < 2.7V	—
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—	1	TPB	—	

**Note 1:** These parameters are characterized, but not tested in manufacturing.



# PIC32MX3XX/4XX

**FIGURE 29-9: OC/PWM MODULE TIMING CHARACTERISTICS**



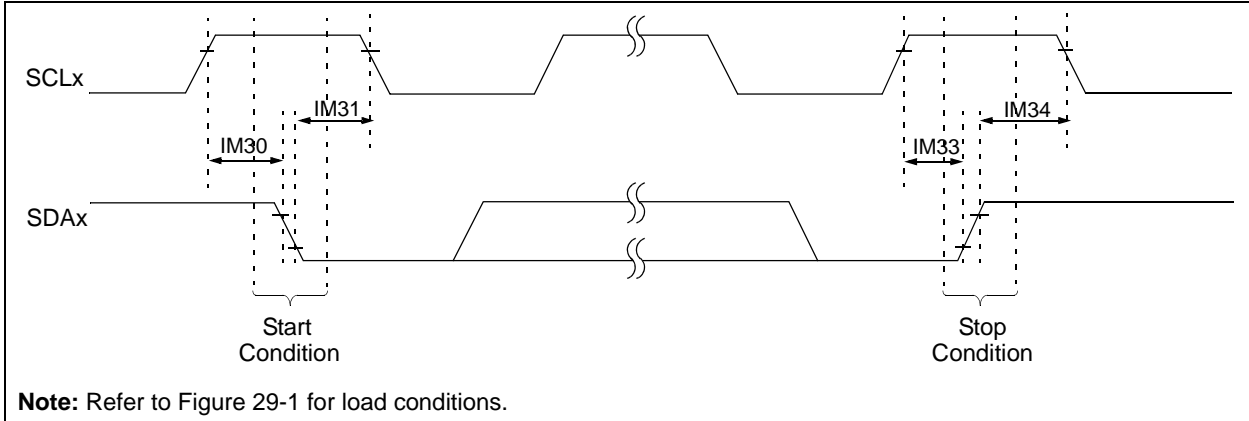
**TABLE 29-27: SIMPLE OC/PWM MODE TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param No.	Symbol	Characteristics <sup>(1)</sup>	Min	Typical <sup>(2)</sup>	Max	Units	Conditions
OC15	TFD	Fault Input to PWM I/O Change	—	—	25	ns	—
OC20	TFLT	Fault Input Pulse Width	50	—	—	ns	—

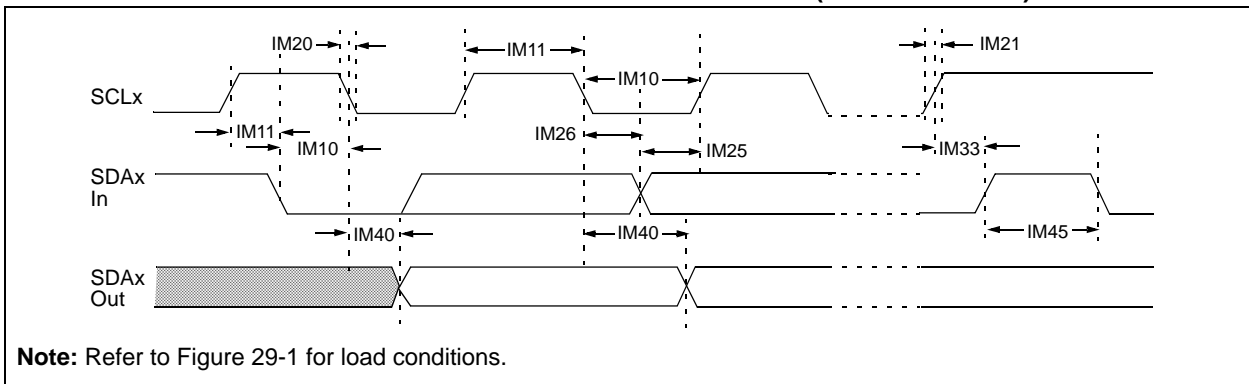
**Note 1:** These parameters are characterized, but not tested in manufacturing.

**Note 2:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

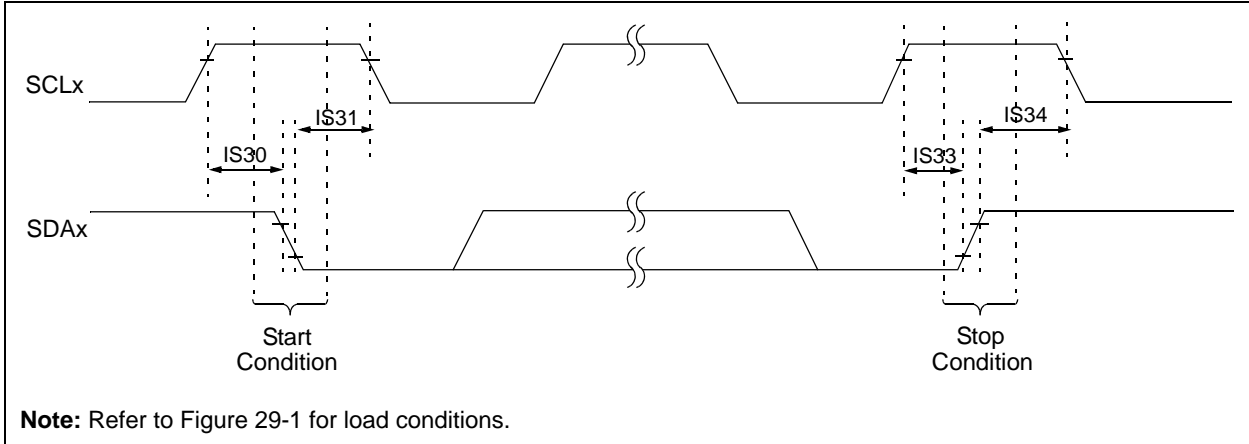
**FIGURE 29-14: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)**



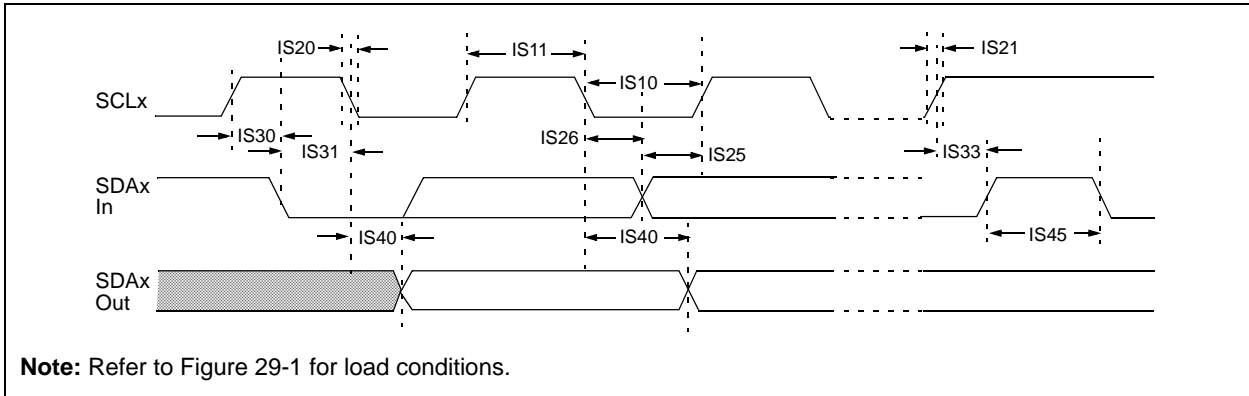
**FIGURE 29-15: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)**



**FIGURE 29-16: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)**



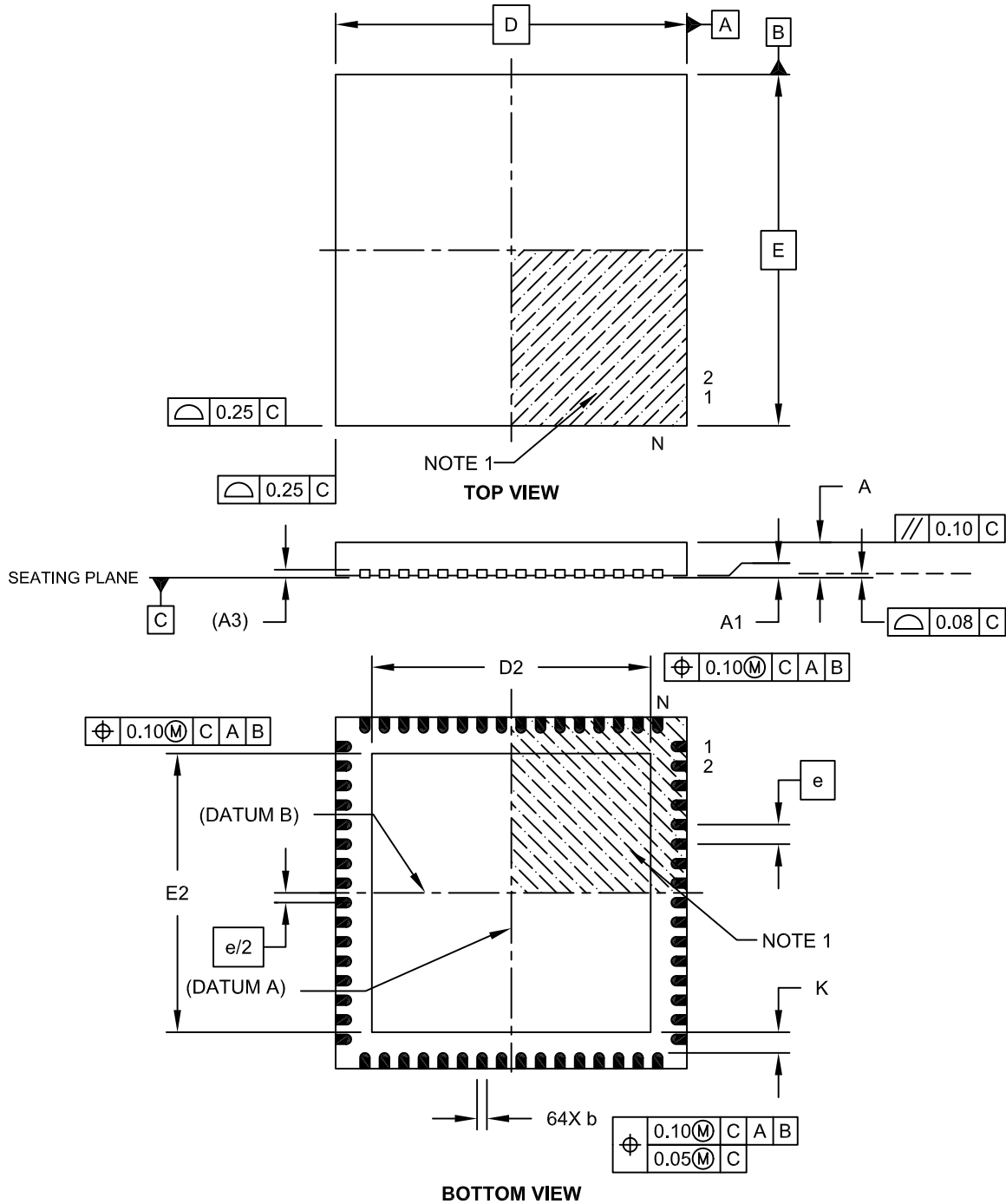
**FIGURE 29-17: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)**



# PIC32MX3XX/4XX

## 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.15 x 7.15 Exposed Pad [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

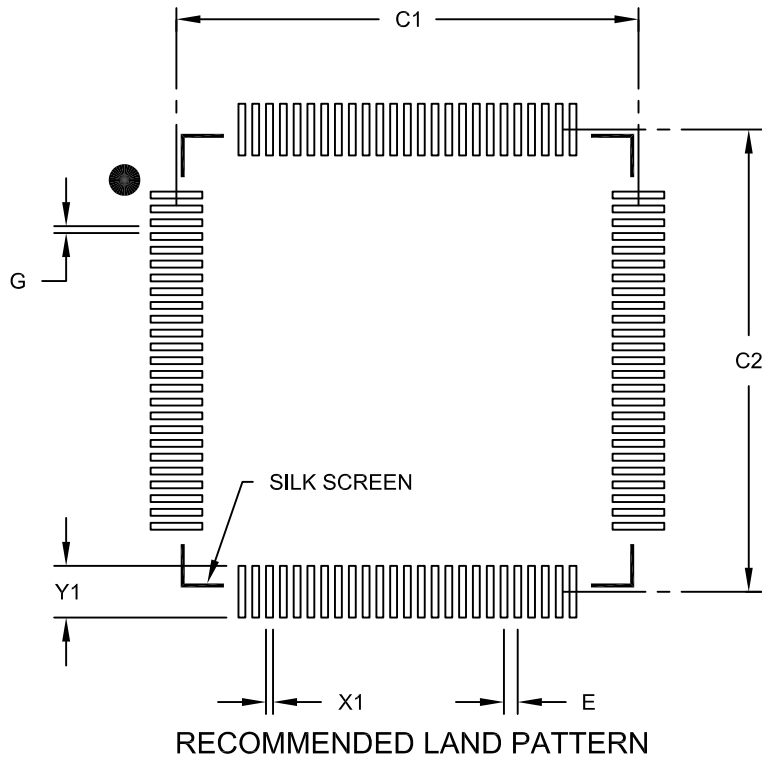


Microchip Technology Drawing C04-149C Sheet 1 of 2

# PIC32MX3XX/4XX

100-Lead Plastic Thin Quad Flatpack (PT)-12x12x1mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0,40 BSC		
Contact Pad Spacing	C1		13,40	
Contact Pad Spacing	C2		13,40	
Contact Pad Width (X100)	X1			0,20
Contact Pad Length (X100)	Y1			1,50
Distance Between Pads	G	0,20		

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100B