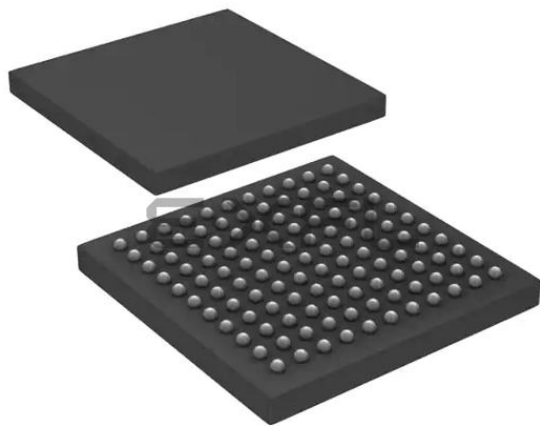




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

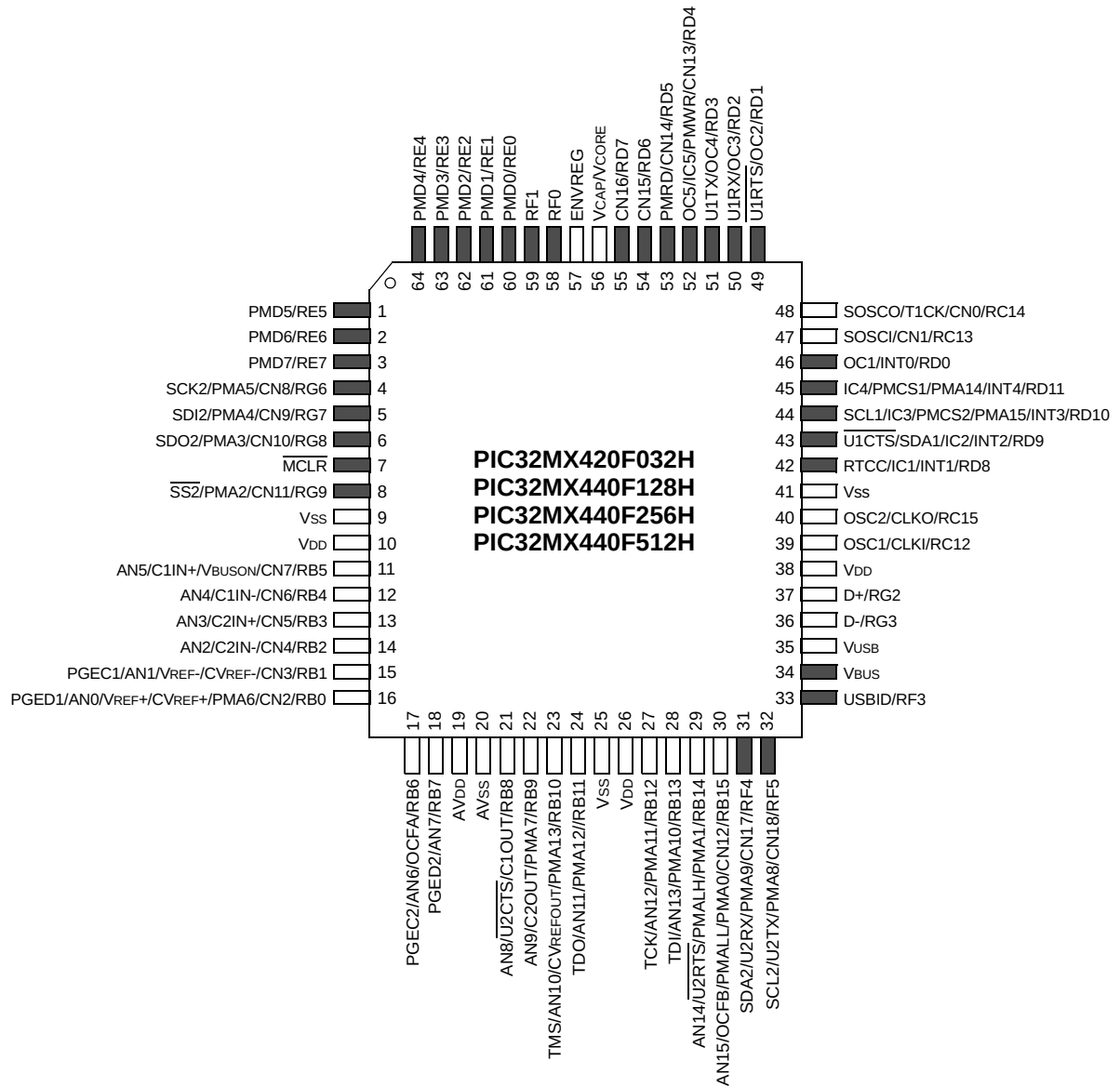
Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx340f128l-80v-bg

Pin Diagrams (Continued)

64-Pin TQFP (USB)

■ = Pins are up to 5V tolerant



2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternately, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 2, MPLAB ICD 3 or MPLAB REAL ICE™.

For more information on ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- "MPLAB® ICD 2 In-Circuit Debugger User's Guide" DS51331
- "Using MPLAB® ICD 2" (poster) DS51265
- "MPLAB® ICD 2 Design Advisory" DS51566
- "Using MPLAB® ICD 3" (poster) DS51765
- "MPLAB® ICD 3 Design Advisory" DS51764
- "MPLAB® REAL ICE™ In-Circuit Debugger User's Guide" DS51616
- "Using MPLAB® REAL ICE™" (poster) DS51749

2.6 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternately, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

2.7 Trace

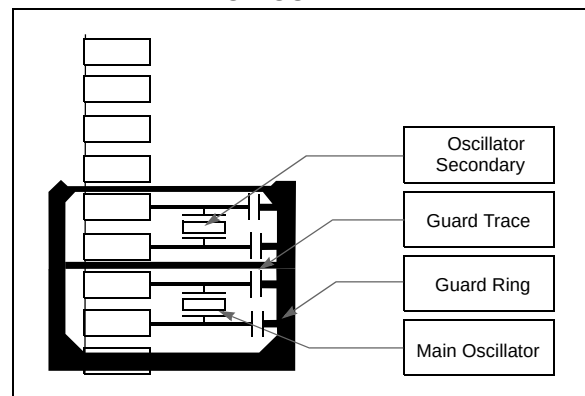
The trace pins can be connected to a hardware-trace-enabled programmer to provide a compress real time instruction trace. When used for trace the TRD3, TRD2, TRD1, TRD0 and TRCLK pins should be dedicated for this use. The trace hardware requires a 22 Ohm series resistor between the trace pins and the trace connector.

2.8 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



PIC32MX3XX/4XX

NOTES:

17.0 SERIAL PERIPHERAL INTERFACE (SPI)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. “Serial Peripheral Interface (SPI)”** (DS61106) of the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

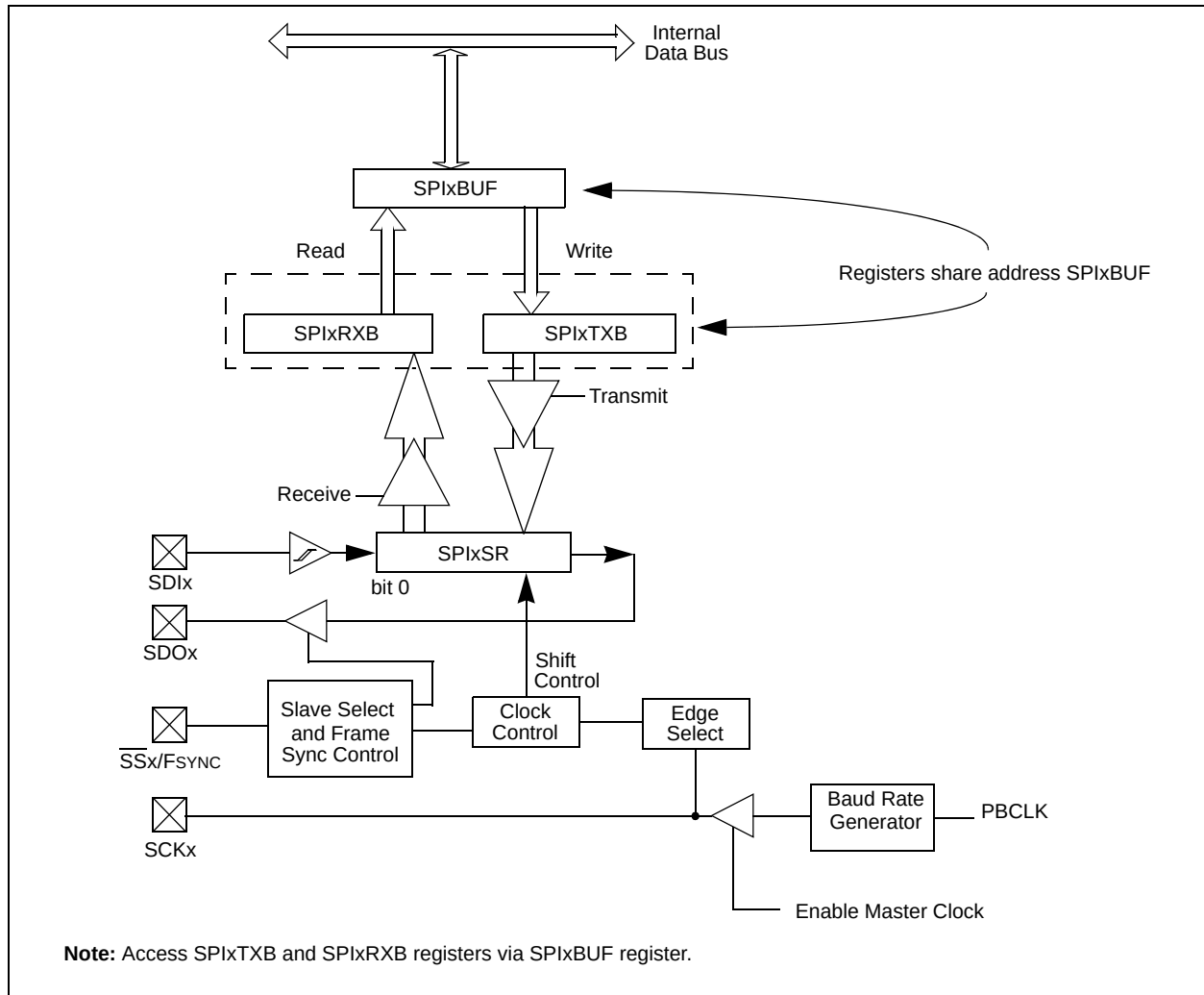
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The SPI module is a synchronous serial interface useful for communicating with external peripherals and other microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, Analog-to-Digital Converters, etc. The PIC32MX SPI module is compatible with Motorola® SPI and SIOP interfaces.

Following are some of the key features of this module:

- Master and Slave Modes Support
- Four Different Clock Formats
- Framed SPI Protocol Support
- User Configurable 8-bit, 16-bit and 32-bit Data Width
- Separate SPI Data Registers for Receive and Transmit
- Programmable Interrupt Event on every 8-bit, 16-bit and 32-bit Data Transfer
- Operation during CPU Sleep and Idle Mode
- Fast Bit Manipulation using CLR, SET and INV Registers

FIGURE 17-1: SPI MODULE BLOCK DIAGRAM



19.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. “Universal Asynchronous Receiver Transmitter (UART)”** (DS61107) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

Note 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

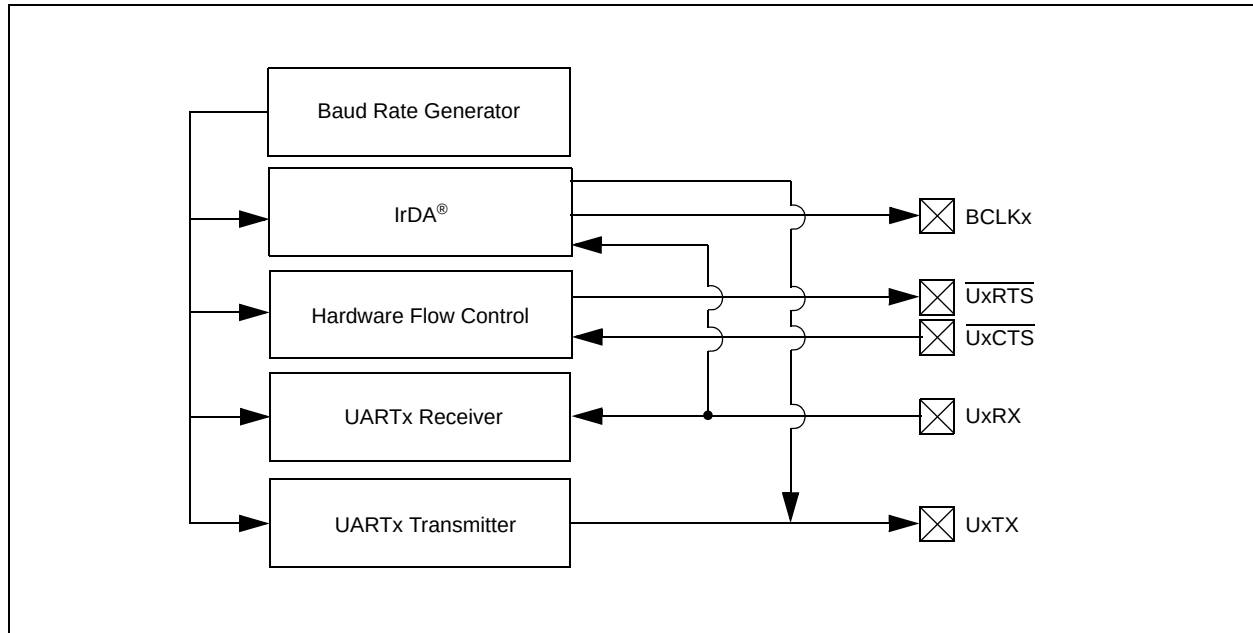
The UART module is one of the serial I/O modules available in PIC32MX3XX/4XX family devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols such as RS-232, RS-485, LIN 1.2 and IrDA®. The module also supports the hardware flow control option, with UxCTS and UxRTS pins, and also includes an IrDA encoder and decoder.

The primary features of the UART module are:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, odd or no parity options (for 8-bit data)
- One or two Stop bits
- Hardware auto-baud feature
- Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 76 bps to 20 Mbps at 80 MHz
- 4-level-deep First-In-First-Out (FIFO) Transmit Data Buffer
- 4-level-deep FIFO Receive Data Buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt only on address detect (9th bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support

Figure 19-1 illustrates a simplified block diagram of the UART.

FIGURE 19-1: UART SIMPLIFIED BLOCK DIAGRAM



20.0 PARALLEL MASTER PORT (PMP)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. “Parallel Master Port (PMP)”** (DS61128) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

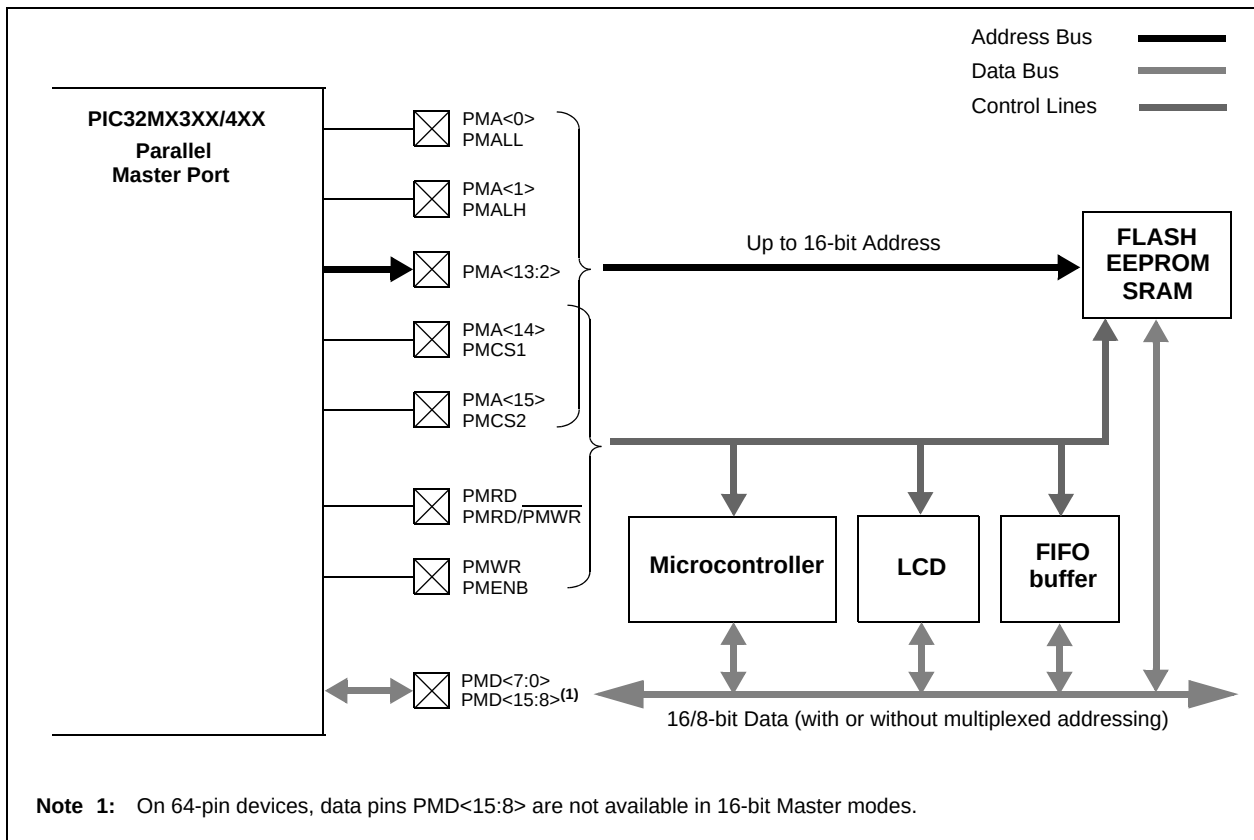
The PMP is a parallel 8-bit/16-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable.

Key features of the PMP module include:

- 8-bit,16-bit interface
- Up to 16 programmable address lines
- Up to two Chip Select lines
- Programmable strobe options
 - Individual read and write strobes, or
 - Read/write strobe with enable strobe
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- Parallel Slave Port support
 - Legacy addressable
 - Address support
 - 4-byte deep auto-incrementing buffer
- Programmable Wait states
- Operate during CPU Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers
- Freeze option for in-circuit debugging

Note: On 64-pin devices, data pins PMD<15:8> are not available.

FIGURE 20-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES



22.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to **Section 17. “10-bit Analog-to-Digital Converter (ADC)”** (DS61104) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The PIC32MX3XX/4XX 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- Up to 1000 kilo samples per second (ksps) conversion speed
- Up to 16 analog input pins
- External voltage reference input pins
- One unipolar, differential Sample-and-Hold Amplifier (SHA)
- Automatic Channel Scan mode
- Selectable conversion trigger source
- 16-word conversion result buffer
- Selectable Buffer Fill modes
- Eight conversion result format options
- Operation during CPU Sleep and Idle modes

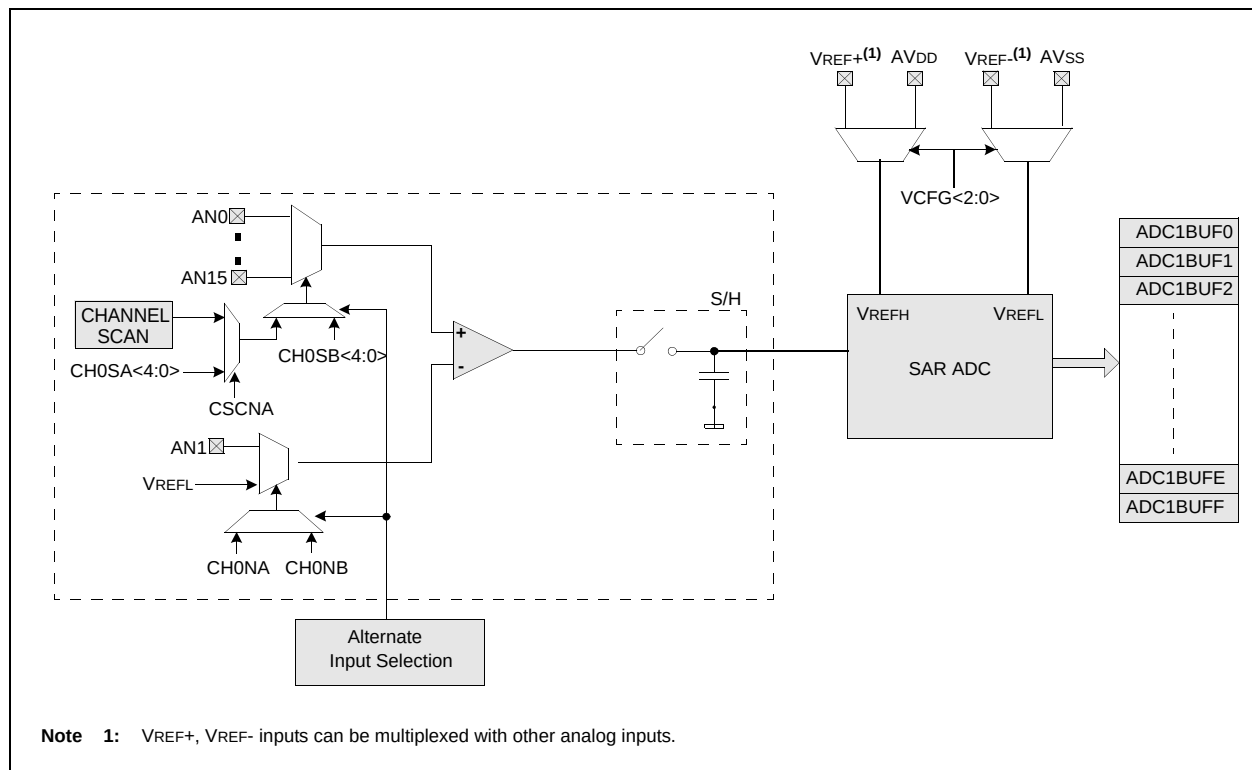
A block diagram of the 10-bit ADC is illustrated in Figure 22-1. The 10-bit ADC has 16 analog input pins, designated AN0-AN15. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.

The analog inputs are connected through two multiplexers (MUXs) to one SHA. The analog input MUXs can be switched between two sets of analog inputs between conversions. Unipolar differential conversions are possible on all channels, other than the pin used as the reference, using a reference input pin (see Figure 22-1).

The Analog Input Scan mode sequentially converts user-specified channels. A control register specifies which analog input channels will be included in the scanning sequence.

The 10-bit ADC is connected to a 16-word result buffer. Each 10-bit result is converted to one of eight, 32-bit output formats when it is read from the result buffer.

FIGURE 22-1: ADC1 MODULE BLOCK DIAGRAM



PIC32MX3XX/4XX

REGISTER 26-2: DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

- bit 13-12 **FPBDIV<1:0>**: Peripheral Bus Clock Divisor Default Value bits
11 = PBCLK is SYSCLK divided by 8
10 = PBCLK is SYSCLK divided by 4
01 = PBCLK is SYSCLK divided by 2
00 = PBCLK is SYSCLK divided by 1
- bit 11 **Reserved**: Write '1'
- bit 10 **OSCIOFNC**: CLKO Enable Configuration bit
1 = CLKO output signal active on the OSCO pin; primary oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 OR 00)
0 = CLKO output disabled
- bit 9-8 **POSCMOD<1:0>**: Primary Oscillator Configuration bits
11 = Primary oscillator disabled
10 = HS oscillator mode selected
01 = XT oscillator mode selected
00 = External clock mode selected
- bit 7 **IESO**: Internal External Switchover bit
1 = Internal External Switchover mode enabled (Two-Speed Start-up enabled)
0 = Internal External Switchover mode disabled (Two-Speed Start-up disabled)
- bit 6 **Reserved**: Write '1'
- bit 5 **FSOSCEN**: Secondary Oscillator Enable bit
1 = Enable Secondary Oscillator
0 = Disable Secondary Oscillator
- bit 4-3 **Reserved**: Write '1'
- bit 2-0 **FNOSC<2:0>**: Oscillator Selection bits
111 = Fast RC Oscillator with divide-by-N (FRCDIV)
110 = FRCDIV16 Fast RC Oscillator with fixed divide-by-16 postscaler
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (Sosc)
011 = Primary Oscillator with PLL module (XT+PLL, HS+PLL, EC+PLL)
010 = Primary Oscillator (XT, HS, EC)⁽¹⁾
001 = Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)
000 = Fast RC Oscillator (FRC)

Note 1: Do not disable Posc (POSCMOD = 00) when using this oscillator source.

26.2 Watchdog Timer (WDT)

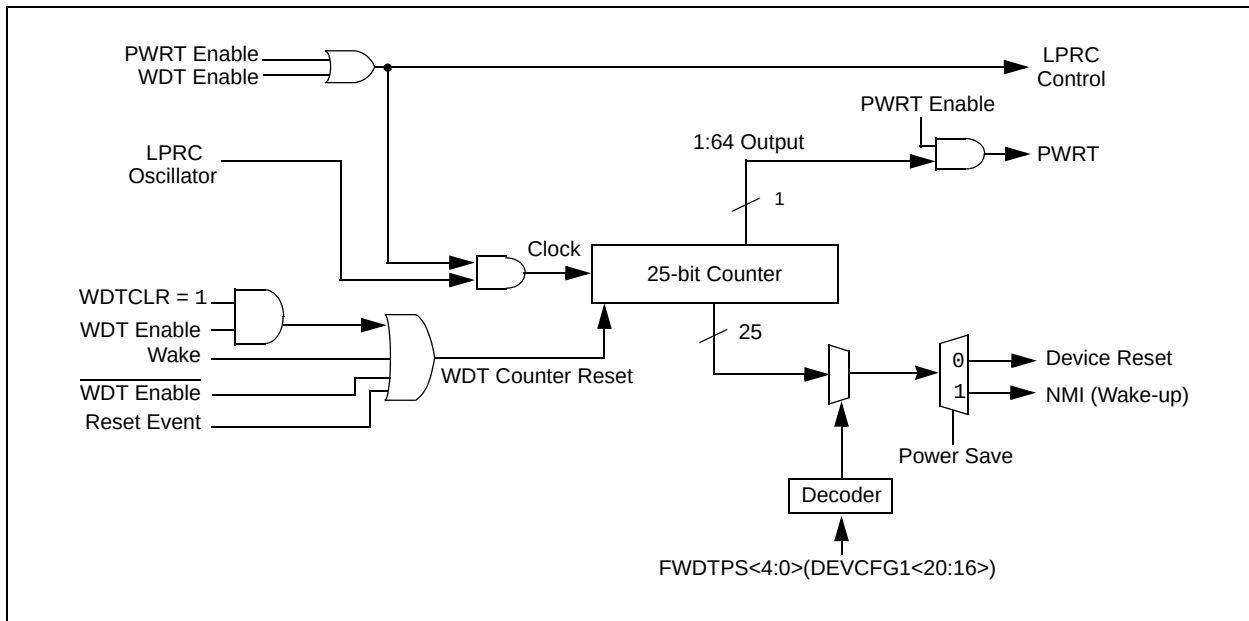
This section describes the operation of the WDT and Power-Up Timer of the PIC32MX3XX/4XX.

The WDT, when enabled, operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are some of the key features of the WDT module:

- Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle

FIGURE 26-1: WATCHDOG AND POWER-UP TIMER BLOCK DIAGRAM



27.0 INSTRUCTION SET

The PIC32MX3XX/4XX family instruction set complies with the MIPS32 Release 2 instruction set architecture. PIC32MX does not support the following features:

- CoreExtend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Table 27-1 provides a summary of the instructions that are implemented by the PIC32MX3XX/4XX family core.

Note: Refer to “MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set” at www.mips.com for more information.

TABLE 27-1: MIPS32® INSTRUCTION SET

Instruction	Description	Function
ADD	Integer Add	$Rd = Rs + Rt$
ADDI	Integer Add Immediate	$Rt = Rs + \text{Immed}$
ADDIU	Unsigned Integer Add Immediate	$Rt = Rs +_U \text{Immed}$
ADDU	Unsigned Integer Add	$Rd = Rs +_U Rt$
AND	Logical AND	$Rd = Rs \& Rt$
ANDI	Logical AND Immediate	$Rt = Rs \& (0_{16} \parallel \text{Immed})$
B	Unconditional Branch (Assembler idiom for: BEQ r0, r0, offset)	$PC += (\text{int})\text{offset}$
BAL	Branch and Link (Assembler idiom for: BGEZAL r0, offset)	$GPR[31] = PC + 8$ $PC += (\text{int})\text{offset}$
BEQ	Branch on Equal	if $Rs == Rt$ $PC += (\text{int})\text{offset}$
BEQL	Branch on Equal Likely ⁽¹⁾	if $Rs == Rt$ $PC += (\text{int})\text{offset}$ else Ignore Next Instruction
BGEZ	Branch on Greater Than or Equal to Zero	if $!Rs[31]$ $PC += (\text{int})\text{offset}$
BGEZAL	Branch on Greater Than or Equal to Zero and Link	$GPR[31] = PC + 8$ if $!Rs[31]$ $PC += (\text{int})\text{offset}$
BGEZALL	Branch on Greater Than or Equal to Zero and Link Likely ⁽¹⁾	$GPR[31] = PC + 8$ if $!Rs[31]$ $PC += (\text{int})\text{offset}$ else Ignore Next Instruction
BGEZL	Branch on Greater Than or Equal to Zero Likely ⁽¹⁾	if $!Rs[31]$ $PC += (\text{int})\text{offset}$ else Ignore Next Instruction
BGTZ	Branch on Greater Than Zero	if $!Rs[31] \&\& Rs \neq 0$ $PC += (\text{int})\text{offset}$
BGTZL	Branch on Greater Than Zero Likely ⁽¹⁾	if $!Rs[31] \&\& Rs \neq 0$ $PC += (\text{int})\text{offset}$ else Ignore Next Instruction
BLEZ	Branch on Less Than or Equal to Zero	if $Rs[31] \parallel Rs == 0$ $PC += (\text{int})\text{offset}$

Note 1: This instruction is deprecated and should not be used.

TABLE 27-1: MIPS32® INSTRUCTION SET (CONTINUED)

Instruction	Description	Function
TGE	Trap if Greater Than or Equal	if (int)Rs >= (int)Rt TrapException
TGEI	Trap if Greater Than or Equal Immediate	if (int)Rs >= (int)Immed TrapException
TGEIU	Trap if Greater Than or Equal Immediate Unsigned	if (uns)Rs >= (uns)Immed TrapException
TGEU	Trap if Greater Than or Equal Unsigned	if (uns)Rs >= (uns)Rt TrapException
TLT	Trap if Less Than	if (int)Rs < (int)Rt TrapException
TLTI	Trap if Less Than Immediate	if (int)Rs < (int)Immed TrapException
TLTIU	Trap if Less Than Immediate Unsigned	if (uns)Rs < (uns)Immed TrapException
TLTU	Trap if Less Than Unsigned	if (uns)Rs < (uns)Rt TrapException
TNE	Trap if Not Equal	if Rs != Rt TrapException
TNEI	Trap if Not Equal Immediate	if Rs != (int)Immed TrapException
WAIT	Wait for Interrupt	Go to a low power mode and stall until interrupt occurs
WRPGPR	Write to GPR in Previous Shadow Set	SGPR[SRSCtl _{PSS} , Rd] = Rt
WSBH	Word Swap Bytes Within Halfwords	Rd = Rt _{23..16} Rt _{31..24} Rt _{7..0} Rt _{15..8}
XOR	Exclusive OR	Rd = Rs ^ Rt
XORI	Exclusive OR Immediate	Rt = Rs ^ (uns)Immed

Note 1: This instruction is deprecated and should not be used.

28.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB C Compiler for Various Device Families
 - HI-TECH C for Various Device Families
 - MPASM™ Assembler
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
 - MPLAB ICD 3
 - PICKit™ 3 Debug Express
- Device Programmers
 - PICKit™ 2 Programmer
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

28.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
 - Simulator
 - Programmer (sold separately)
 - In-Circuit Emulator (sold separately)
 - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
 - Source files (C or assembly)
 - Mixed C and assembly
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

29.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of PIC32MX3XX/4XX electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MX3XX/4XX are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings (Note 1)

Ambient temperature under bias.....	-40°C to +105°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to VSS	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to VSS (Note 3).....	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 2.3V (Note 3).....	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to VSS when VDD < 2.3V (Note 3).....	-0.3V to +3.6V
Voltage on VCORE with respect to VSS	-0.3V to 2.0V
Voltage on VBUS with respect to VSS	-0.3V to +5.5V
Maximum current out of VSS pin(s).....	300 mA
Maximum current into VDD pin(s) (Note 2).....	300 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports (Note 2).....	200 mA

Note 1: Stresses above those listed under “**Absolute Maximum Ratings**” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 29-2).

3: See the “**Pin Diagrams**” section for the 5V tolerant pins.

PIC32MX3XX/4XX

TABLE 29-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD}) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp			
Parameter No.	Typical ⁽²⁾	Max.	Units	Conditions		
Module Differential Current (Continued)						
DC43	—	1100	μA	-40°C	2.5V	ADC: ΔIADC (Notes 3, 4, 6)
DC43a	—	1100	μA	+25°C		
DC43b	—	1000	μA	+85°C		
DC43h	—	1200	μA	+105°C		
DC43c	880	—	μA	—	—	ADC: ΔIADC (Notes 3, 4)
DC43e	—	1100	μA	-40°C	3.6V	ADC: ΔIADC (Notes 3, 4)
DC43f	—	1100	μA	+25°C		
DC43g	—	1000	μA	+85°C		
DC43i	—	1200	μA	+105°C		

- Note 1:** Base I_{PD} is measured with all digital peripheral modules disabled. All I/Os are configured as inputs and pulled low. WDT and FSCM are disabled.
- 2:** Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.
- 4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.
- 5:** Data is characterized at +70°C and not tested. Parameter is for design guidance only.
- 6:** This parameter is characterized, but not tested in manufacturing.

PIC32MX3XX/4XX

TABLE 29-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
DO10 DO16	VOL	Output Low Voltage I/O Ports	—	—	0.4	V	IO _L = 7 mA, V _{DD} = 3.6V
			—	—	0.4	V	IO _L = 6 mA, V _{DD} = 2.3V
		OSC2/CLKO	—	—	0.4	V	IO _L = 3.5 mA, V _{DD} = 3.6V
			—	—	0.4	V	IO _L = 2.5 mA, V _{DD} = 2.3V
DO20 DO26	VOH	Output High Voltage I/O Ports	2.4	—	—	V	IO _H = -12 mA, V _{DD} = 3.6V
			1.4	—	—	V	IO _H = -12 mA, V _{DD} = 2.3V
		OSC2/CLKO	2.4	—	—	V	IO _H = -12 mA, V _{DD} = 3.6V
			1.4	—	—	V	IO _H = -12 mA, V _{DD} = 2.3V

TABLE 29-10: ELECTRICAL CHARACTERISTICS: BROWN-OUT RESET (BOR)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
BO10	VBOR	BOR Event on V _{DD} transition high-to-low	2.0	—	2.3	V	—

PIC32MX3XX/4XX

FIGURE 29-21: PARALLEL MASTER PORT READ TIMING DIAGRAM

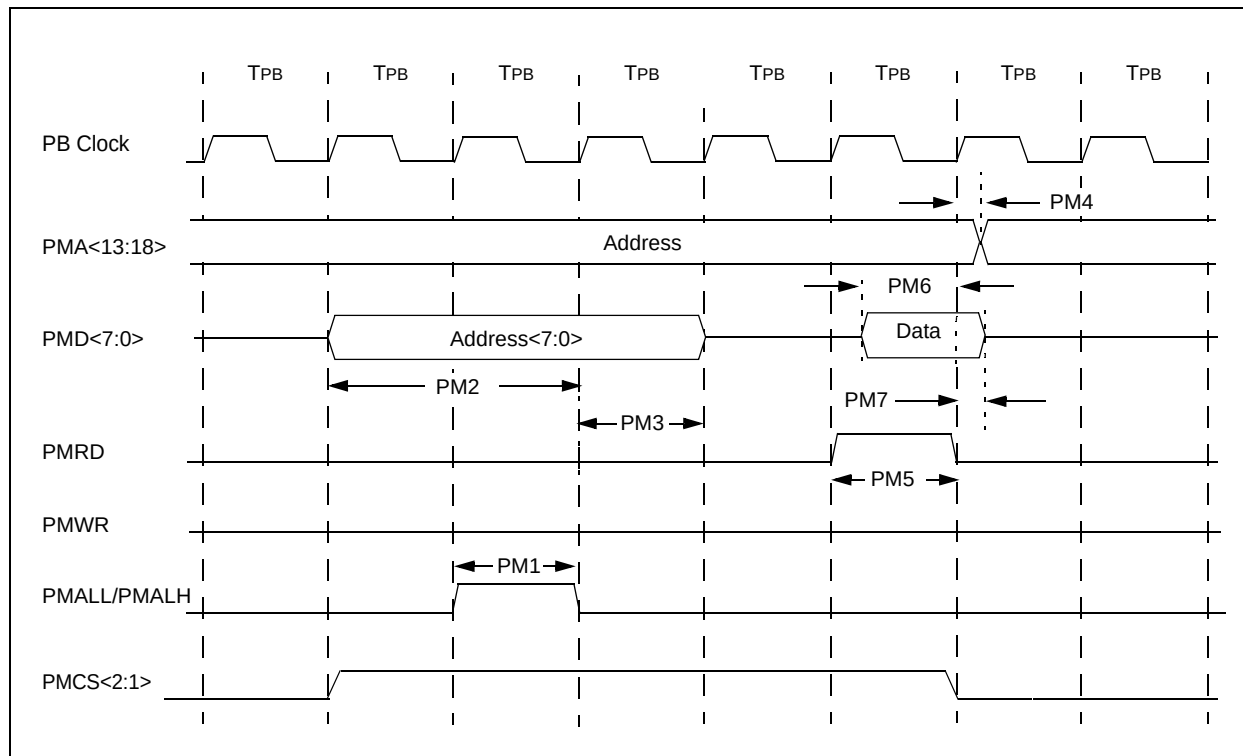


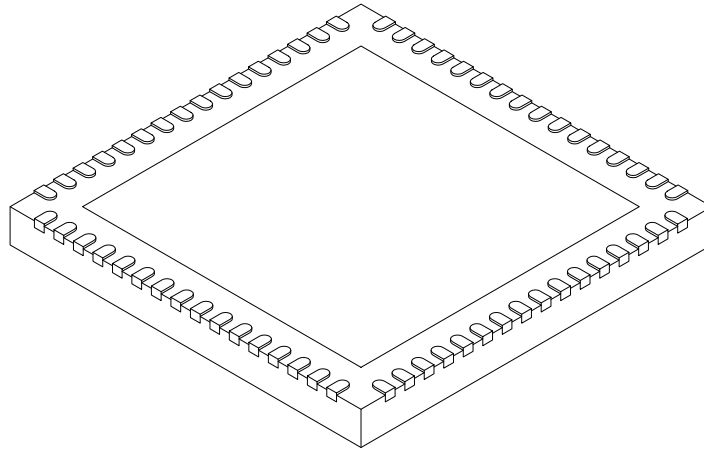
TABLE 29-38: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical	Max.	Units	Conditions
PM1	TLAT	PMALL/PMALH Pulse Width	—	1 TPB	—	—	—
PM2	TDSU	Address Out Valid to PMALL/PMALH Invalid (address setup time)	—	2 TPB	—	—	—
PM3	TADHOLD	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	1 TPB	—	—	—
PM4	TAHOLD	PMRD Inactive to Address Out Invalid (address hold time)	5	—	—	ns	—
PM5	TRD	PMRD Pulse Width	—	1 TPB	—	—	—
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	15	—	—	ns	—
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)	—	80	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.15 x 7.15 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	64		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	9.00 BSC		
Exposed Pad Width	E2	7.05	7.15	7.50
Overall Length	D	9.00 BSC		
Exposed Pad Length	D2	7.05	7.15	7.50
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

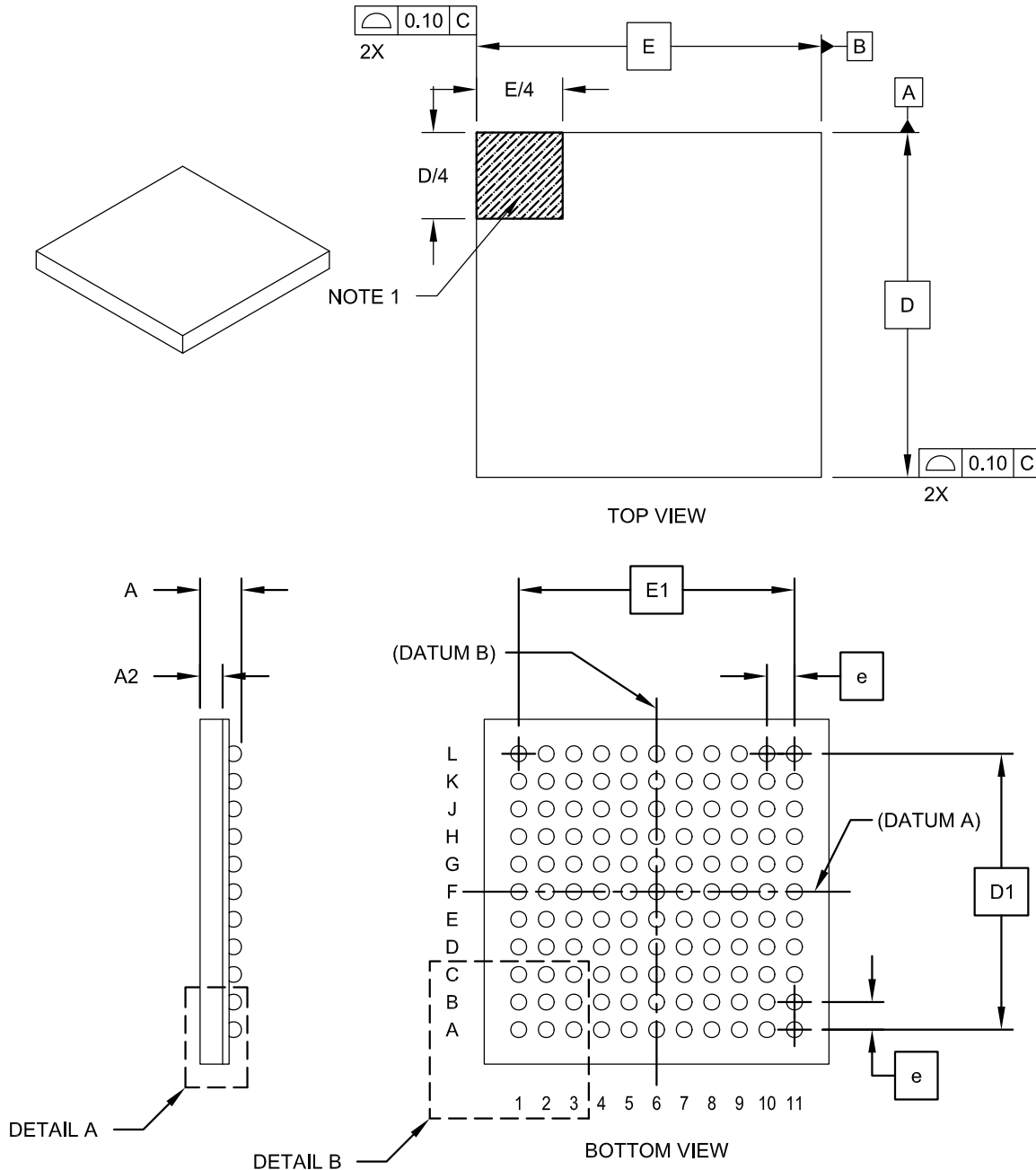
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-149C Sheet 2 of 2

121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [XBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-148B Sheet 1 of 2

PIC32MX3XX/4XX

TABLE A-3: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 29.0 “Electrical Characteristics”	Added the new V-Temp temperature range (-40°C to +105°C) to the heading of all specification tables. Updated the Ambient temperature under bias, updated the Voltage on any 5V tolerant pin with respect to V_{SS} when V_{DD} < 2.3V, and added Voltage on V_{BUS} with respect to V_{SS} in Absolute Maximum Ratings. Added the characteristic, DC5a to Operating MIPS vs. Voltage (see Table 29-1). Updated or added the following parameters to the Operating Current (I_{DD}) DC Characteristics: DC20, DC23, DC24c, DC25d, DC26c (see Table 29-5). Added the following parameters to the Idle Current (I_{IDLE}) DC Characteristics: DC30c, DC31c, DC32c, DS33c, DC34c, DC35c, and DC36c (see Table 29-6). Added the following parameters to the Power-down Current (I_{PD}) DC Characteristics: DC40g, DC40h, DC40i, DC41g, DC41h, DC42g, DC42h, DC42i, DC43h, and DC43i (see Table 29-7). Added the Brown-out Reset (BOR) Electrical Characteristics (see Table 29-10). Removed all Conditions from the Program Memory DC Characteristics (see Table 29-11). Removed the AC Characteristics voltage reference table (Table 29-15). Added Note 2 to the PLL Clock Timing Specifications (see Table 29-18). Updated the OC/PWM Module Timing Characteristics (see Figure 29-9). Added parameter IM51 and Note 3 to the I2Cx Bus Data Timing Requirements (Master Mode) (see Table 29-32). Added parameter numbers (AD13, AD14, and AD15) to the ADC Module Specifications (see Table 29-34). Updated the 10-bit ADC Conversion Rate Parameters (see Table 29-35). Updated parameter AD57 (TSAMP) in the Analog-to-Digital Conversion Timing Requirements (see Table 29-36). Updated the Conditions for parameters USB313, USB318, and USB319 in the OTG Electrical Specifications (see Table 29-40).
Section 30.0 “Packaging Information”	Updated the 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] packing diagram.
Product Identification System	Added the new V-Temp (V) temperature information.

PIC32MX3XX/4XX

W

Watchdog Timer

Operation	137
WWW Address.....	209
WWW, On-Line Support.....	19