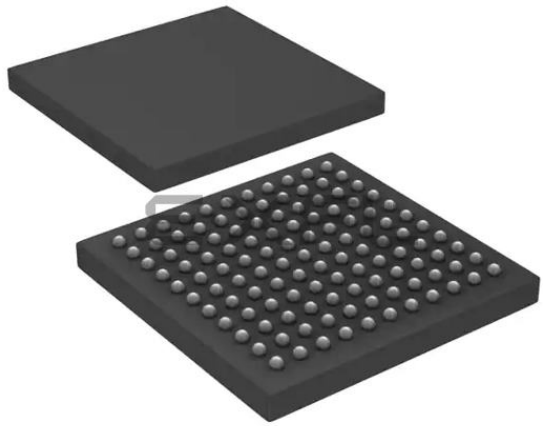
Microchip Technology - PIC32MX340F128LT-80I/BG Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

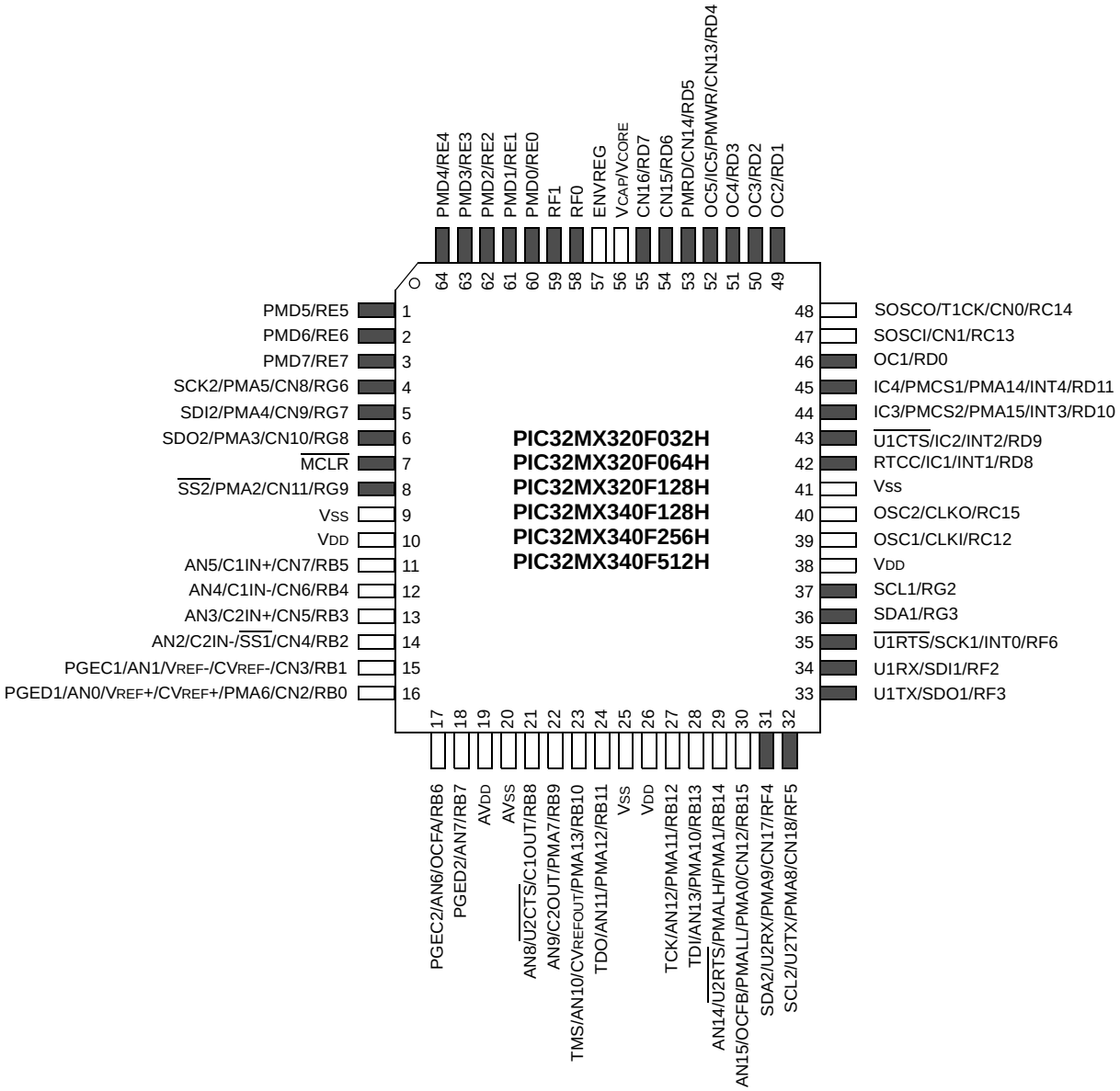
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx340f128lt-80i-bg

Pin Diagrams (Continued)

64-Pin TQFP (General Purpose)

= Pins are up to 5V tolerant



1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

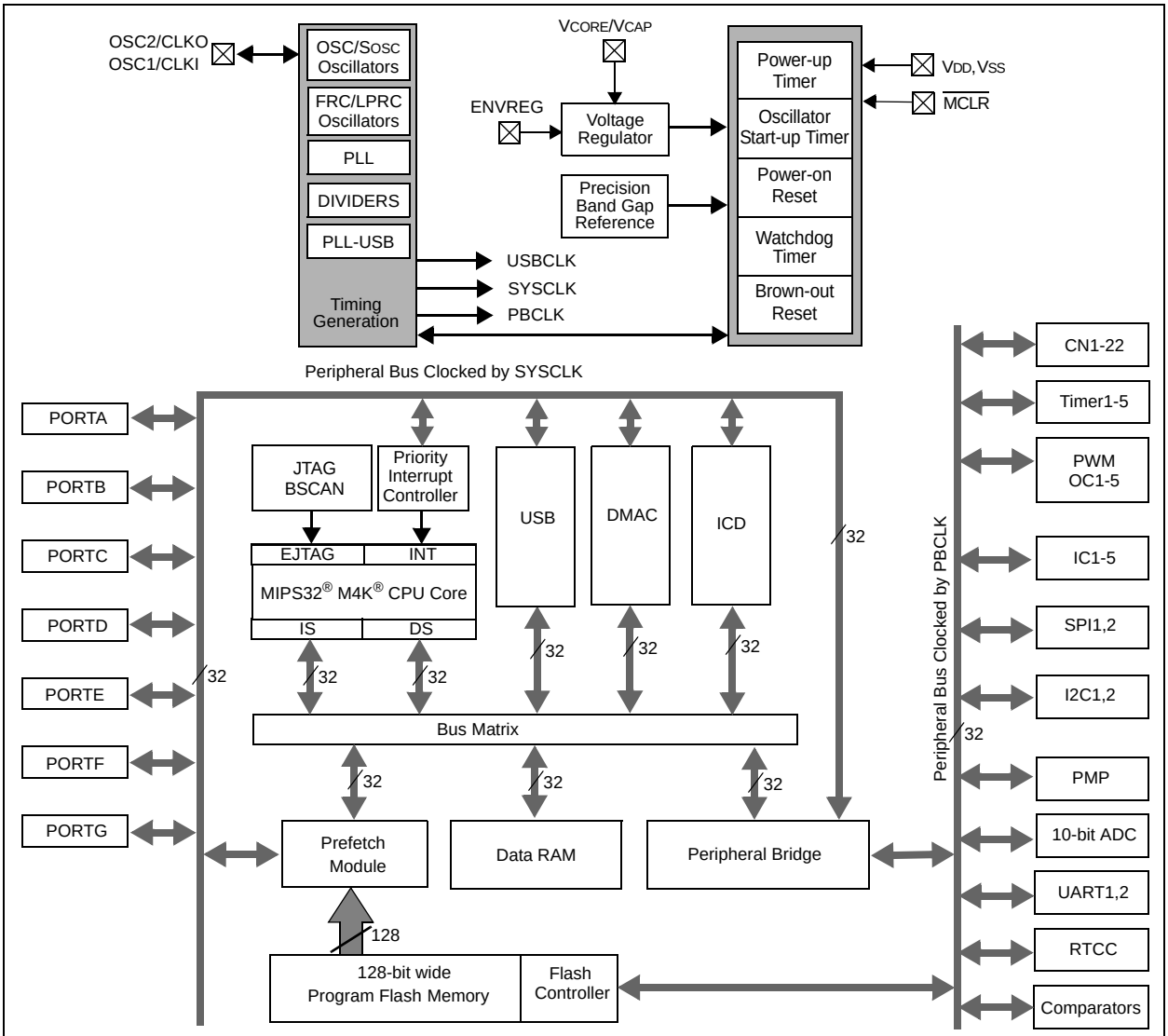
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the PIC32MX3XX/4XX devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX3XX/4XX family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: BLOCK DIAGRAM(1,2)



Note 1: Some features are not available on all device variants.
2: BOR functionality is provided when the on-board voltage regulator is enabled.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number(1)			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
TMS	23	17	G3	I	ST	JTAG Test mode select pin.
TCK	27	38	J6	I	ST	JTAG test clock input pin.
TDI	28	60	G11	I	ST	JTAG test data input pin.
TDO	24	61	G9	O	—	JTAG test data output pin.
RTCC	42	68	E9	O	—	Real-Time Clock Alarm Output.
CVREF-	15	28	L2	I	Analog	Comparator Voltage Reference (low).
CVREF+	16	29	K3	I	Analog	Comparator Voltage Reference (high).
CVREFOUT	23	34	L5	O	Analog	Comparator Voltage Reference Output.
C1IN-	12	21	H2	I	Analog	Comparator 1 Negative Input.
C1IN+	11	20	H1	I	Analog	Comparator 1 Positive Input.
C1OUT	21	32	K4	O	—	Comparator 1 Output.
C2IN-	14	23	J2	I	Analog	Comparator 2 Negative Input.
C2IN+	13	22	J1	I	Analog	Comparator 2 Positive Input.
C2OUT	22	33	L4	O	—	Comparator 2 Output.
PMA0	30	44	L8	I/O	TTL/ST	Parallel Master Port Address Bit 0 Input (Buffered Slave modes) and Output (Master modes).
PMA1	29	43	K7	I/O	TTL/ST	Parallel Master Port Address Bit 1 Input (Buffered Slave modes) and Output (Master modes).
PMA2	8	14	F3	O	—	Parallel Master Port Address (De-multiplexed Master Modes).
PMA3	6	12	F2	O	—	
PMA4	5	11	F4	O	—	
PMA5	4	10	E3	O	—	
PMA6	16	29	K3	O	—	
PMA7	22	28	L2	O	—	
PMA8	32	50	L11	O	—	
PMA9	31	49	L10	O	—	
PMA10	28	42	L7	O	—	
PMA11	27	41	J7	O	—	
PMA12	24	35	J5	O	—	
PMA13	23	34	L5	O	—	
PMA14	45	71	C11	O	—	
PMA15	44	70	D11	O	—	
PMCS1	45	71	C11	O	—	Parallel Master Port Chip Select 1 Strobe.
PMCS2	44	70	D11	O	—	Parallel Master Port Chip Select 2 Strobe.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

4.0 MEMORY ORGANIZATION

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 3. "Memory Organization"** (DS61115) of the *"PIC32 Family Reference Manual",* which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX3XX/4XX microcontrollers provide 4 GB of unified virtual memory address space. All memory regions including program, data memory, SFRs and Configuration registers reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX3XX/4XX to execute from data memory.

4.1 Key Features

- 32-bit native data width
- Separate User and Kernel mode address space
- Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable and non-cacheable address regions

4.2 PIC32MX3XX/4XX Memory Layout

PIC32MX3XX/4XX microcontrollers implement two address spaces: Virtual and Physical. All hardware resources such as program memory, data memory and peripherals are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by peripherals such as DMA and Flash controller that access memory independently of CPU.

TABLE 4-9: OUTPUT COMPARE1-5 REGISTERS MAP(1)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	OC1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3010	OC1R	31:16	OC1R<31:0>																xxxx
		15:0																	xxxx
3020	OC1RS	31:16	OC1RS<31:0>																xxxx
		15:0																	xxxx
3200	OC2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3210	OC2R	31:16	OC2R<31:0>																xxxx
		15:0																	xxxx
3220	OC2RS	31:16 15:0	OC2RS<31:0>																xxxx
																			xxxx
3400	OC3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3410	OC3R	31:16	OC3R<31:0>																xxxx
		15:0																	xxxx
3420	OC3RS	31:16 15:0	OC3RS<31:0>																xxxx
																			xxxx
3600	OC4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3610	OC4R	31:16	OC4R<31:0>																xxxx
		15:0																	xxxx
3620	OC4RS	31:16 15:0	OC4RS<31:0>																xxxx
																			xxxx
3800	OC5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
3810	OC5R	31:16	OC5R<31:0>																xxxx
		15:0																	xxxx
3820	OC5RS	31:16	OC5RS<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-13: ADC REGISTERS MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9000	AD1CON1(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	FORM<2:0>			SSRC<2:0>			CLRASAM	—	ASAM	SAMP	DONE	0000
9010	AD1CON2(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	VCFG2	VCFG1	VCFG0	OFFCAL	—	CSCNA	—	—	BUFS	—	SMPI<3:0>				BUFM	ALTS	0000
9020	AD1CON3(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ADRC	—	—	SAMC<4:0>					ADCS<7:0>								0000
9040	AD1CHS(1)	31:16	CH0NB	—	—	—	CH0SB<3:0>				CH0NA	—	—	—	CH0SA<3:0>				0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9060	AD1PCFG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PCFG15	PCFG14	PCFG13	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000
9050	AD1CSSL(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0	0000
9070	ADC1BUF0	31:16	ADC Result Word 0 (ADC1BUF0<31:0>)																0000
		15:0																	0000
9080	ADC1BUF1	31:16	ADC Result Word 1 (ADC1BUF1<31:0>)																0000
		15:0																	0000
9090	ADC1BUF2	31:16	ADC Result Word 2 (ADC1BUF2<31:0>)																0000
		15:0																	0000
90A0	ADC1BUF3	31:16	ADC Result Word 3 (ADC1BUF3<31:0>)																0000
		15:0																	0000
90B0	ADC1BUF4	31:16	ADC Result Word 4 (ADC1BUF4<31:0>)																0000
		15:0																	0000
90C0	ADC1BUF5	31:16	ADC Result Word 5 (ADC1BUF5<31:0>)																0000
		15:0																	0000
90D0	ADC1BUF6	31:16	ADC Result Word 6 (ADC1BUF6<31:0>)																0000
		15:0																	0000
90E0	ADC1BUF7	31:16	ADC Result Word 7 (ADC1BUF7<31:0>)																0000
		15:0																	0000
90F0	ADC1BUF8	31:16	ADC Result Word 8 (ADC1BUF8<31:0>)																0000
		15:0																	0000
9100	ADC1BUF9	31:16	ADC Result Word 9 (ADC1BUF9<31:0>)																0000
		15:0																	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

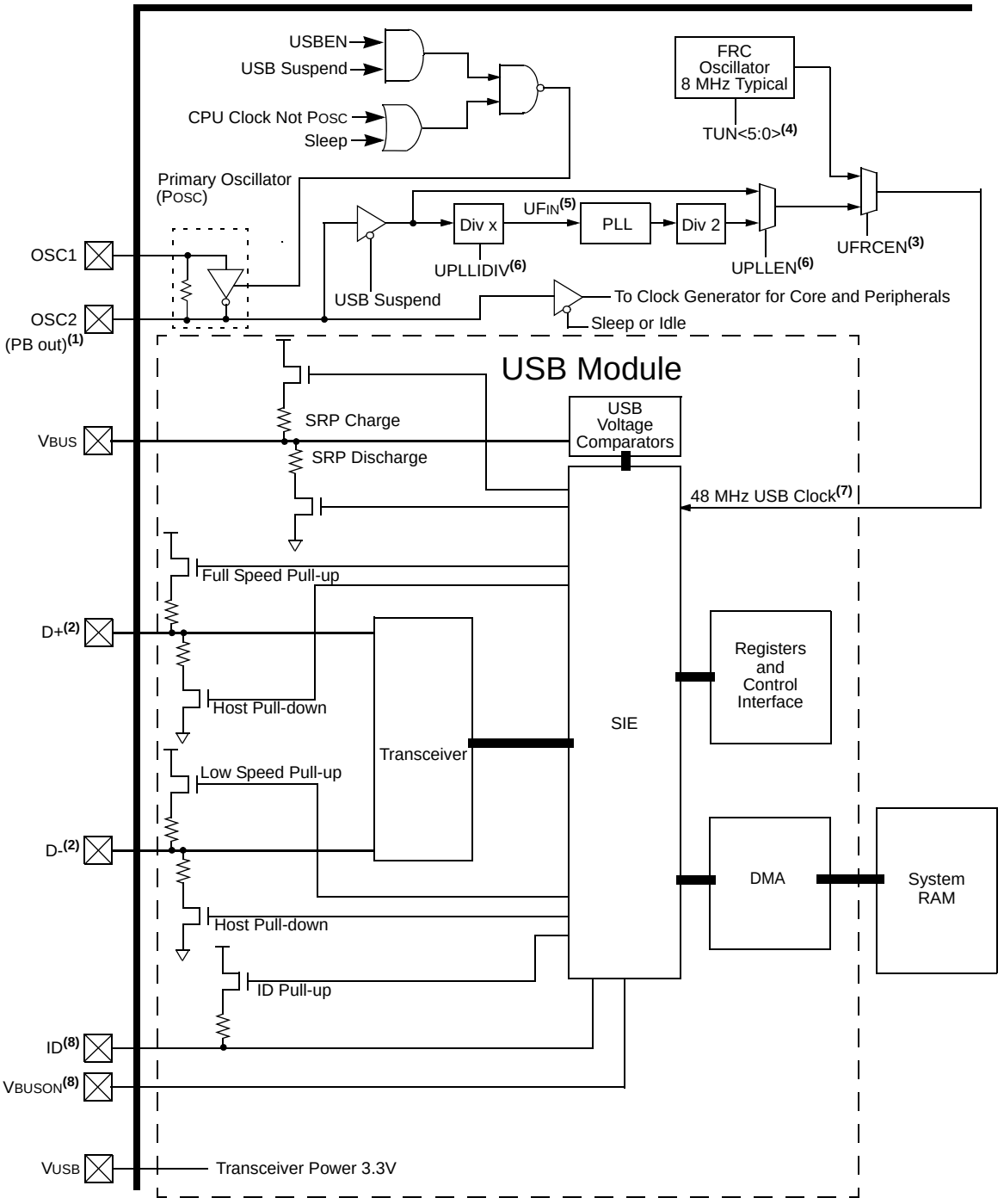
TABLE 4-13: ADC REGISTERS MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9110	ADC1BUFA	31:16	ADC Result Word A (ADC1BUFA<31:0>)																0000
		15:0																	0000
9120	ADC1BUFB	31:16	ADC Result Word B (ADC1BUFB<31:0>)																0000
		15:0																	0000
9130	ADC1BUFC	31:16	ADC Result Word C (ADC1BUFC<31:0>)																0000
		15:0																	0000
9140	ADC1BUFD	31:16	ADC Result Word D (ADC1BUFD<31:0>)																0000
		15:0																	0000
9150	ADC1BUFE	31:16	ADC Result Word E (ADC1BUFE<31:0>)																0000
		15:0																	0000
9160	ADC1BUFF	31:16	ADC Result Word F (ADC1BUFF<31:0>)																0000
		15:0																	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

FIGURE 11-1: PIC32MX3XX/4XX FAMILY USB INTERFACE DIAGRAM



Note 1: PB clock is only available on this pin for select EC modes.
2: Pins can be used as digital inputs when USB is not enabled.
3: This bit field is contained in the OSCCON register.
4: This bit field is contained in the OSCTRM register.
5: USB PLL UFIN requirements: 4 MHz.
6: This bit field is contained in the DEVCFG2 register.
7: A 48 MHz clock is required for proper USB operation.
8: Pins can be used as GPIO when the USB module is disabled.

12.0 I/O PORTS

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. "I/O Ports"** (DS61120) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

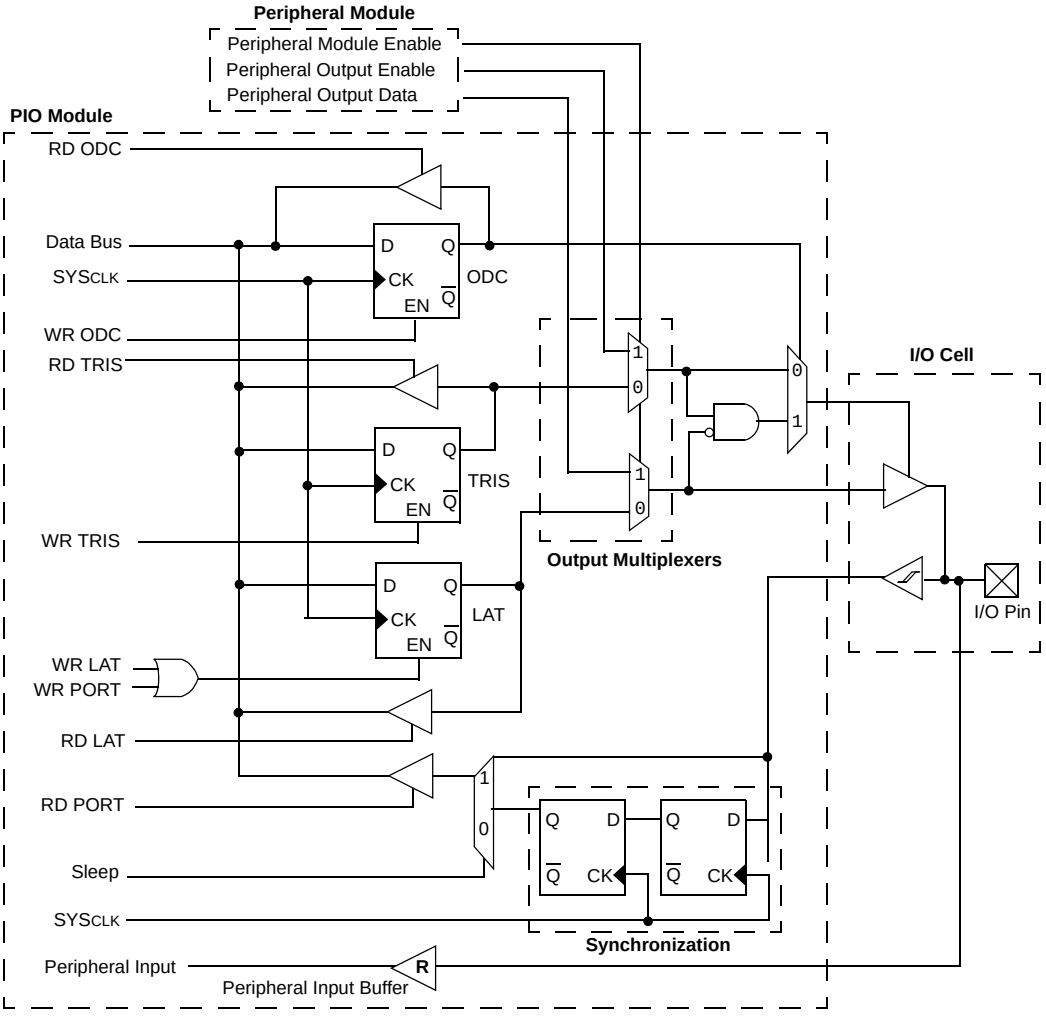
General purpose I/O pins are the simplest of peripherals. They allow the PIC® MCU to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate function(s). These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

Following are some of the key features of this module:

- Individual Output Pin Open-drain Enable/Disable
- Individual Input Pin Weak Pull-up Enable/Disable
- Monitor Selective Inputs and Generate Interrupt when Change in Pin State is Detected
- Operation during CPU Sleep and Idle modes
- Fast Bit Manipulation using CLR, SET and INV Registers

Figure 12-1 illustrates a block diagram of a typical multiplexed I/O port.

FIGURE 12-1: BLOCK DIAGRAM OF A TYPICAL MULTIPLEXED PORT STRUCTURE



Legend: R = Peripheral input buffer types may vary. Refer to Table 1-1 for peripheral details.

Note: This block diagram is a general representation of a shared port/peripheral structure for illustration purposes only. The actual structure for any specific port/peripheral combination may be different than it is shown here.

17.0 SERIAL PERIPHERAL INTERFACE (SPI)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS61106) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

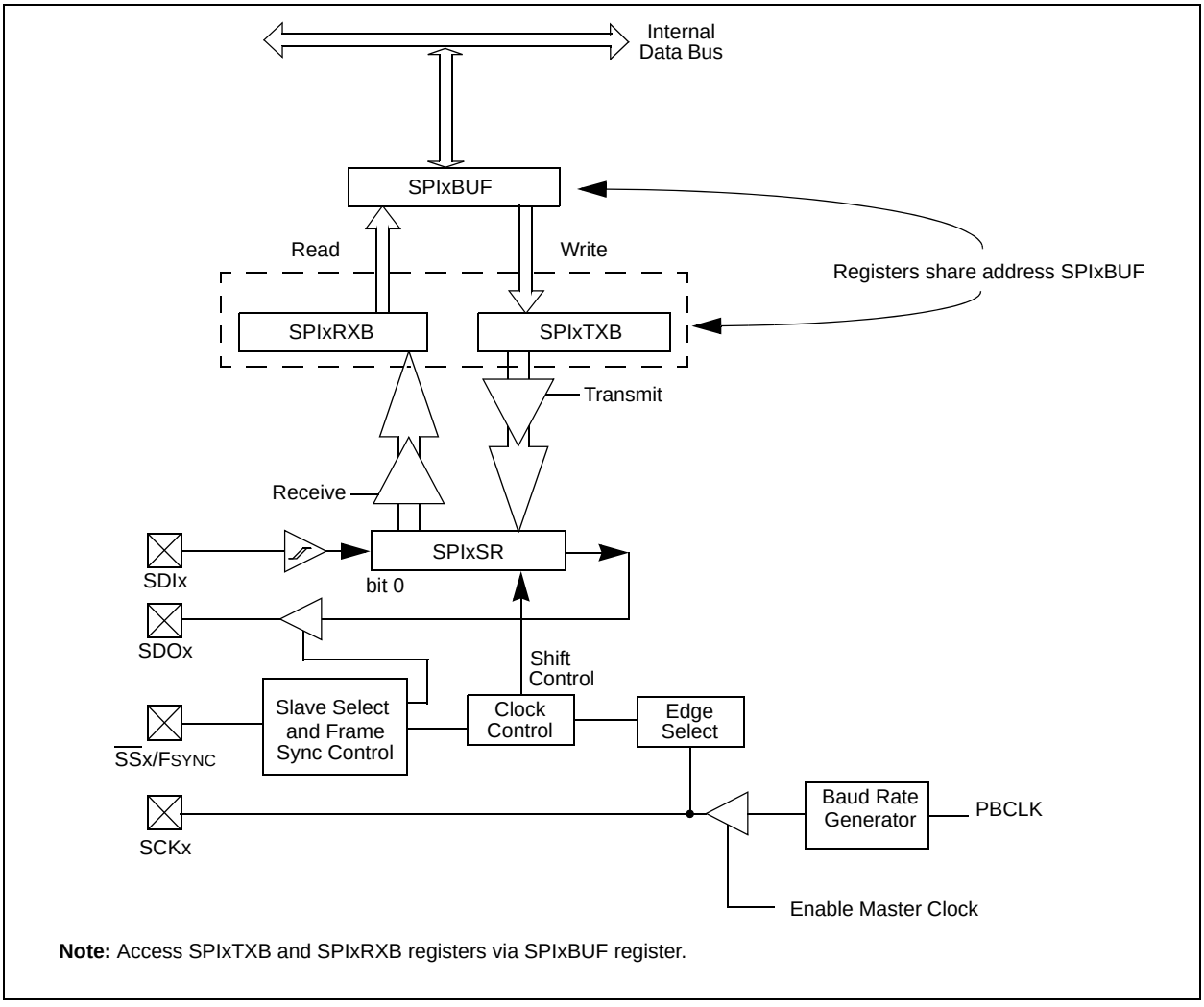
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The SPI module is a synchronous serial interface useful for communicating with external peripherals and other microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, Analog-to-Digital Converters, etc. The PIC32MX SPI module is compatible with Motorola® SPI and SIOP interfaces.

Following are some of the key features of this module:

- Master and Slave Modes Support
- Four Different Clock Formats
- Framed SPI Protocol Support
- User Configurable 8-bit, 16-bit and 32-bit Data Width
- Separate SPI Data Registers for Receive and Transmit
- Programmable Interrupt Event on every 8-bit, 16-bit and 32-bit Data Transfer
- Operation during CPU Sleep and Idle Mode
- Fast Bit Manipulation using CLR, SET and INV Registers

FIGURE 17-1: SPI MODULE BLOCK DIAGRAM



Note: Access SPIxTXB and SPIxRXB registers via SPIxBUF register.

NOTES:

NOTES:

NOTES:

REGISTER 26-1: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

bit 19-12 **PWP<7:0>:** Program Flash Write-Protect bits

Prevents selected program Flash memory pages from being modified during code execution. The PWP bits represent the one's compliment of the number of write protected program Flash memory pages.

11111111 = Disabled
11111110 = 0xBD00_0FFF
11111101 = 0xBD00_1FFF
11111100 = 0xBD00_2FFF
11111011 = 0xBD00_3FFF
11111010 = 0xBD00_4FFF
11111001 = 0xBD00_5FFF
11111000 = 0xBD00_6FFF
11110111 = 0xBD00_7FFF
11110110 = 0xBD00_8FFF
11110101 = 0xBD00_9FFF
11110100 = 0xBD00_AFFF
11110011 = 0xBD00_BFFF
11110010 = 0xBD00_CFFF
11110001 = 0xBD00_DFFF
11110000 = 0xBD00_EFFF
11101111 = 0xBD00_FFFF
.
.
.
01111111 = 0xBD07_FFFF

bit 11-4 **Reserved:** Write '1'

bit 3 **ICESEL:** In-Circuit Emulator/Debugger Communication Channel Select bit

1 = PGEC2/PGED2 pair is used
0 = PGEC1/PGED1 pair is used

bit 2 **Reserved:** Write '1'

bit 1-0 **DEBUG<1:0>:** Background Debugger Enable bits (forced to '11' if code-protect is enabled)

11 = Debugger disabled
10 = Debugger enabled
01 = Reserved (same as '11' setting)
00 = Reserved (same as '11' setting)

26.2 Watchdog Timer (WDT)

This section describes the operation of the WDT and Power-Up Timer of the PIC32MX3XX/4XX.

The WDT, when enabled, operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are some of the key features of the WDT module:

- Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle

FIGURE 26-1: WATCHDOG AND POWER-UP TIMER BLOCK DIAGRAM

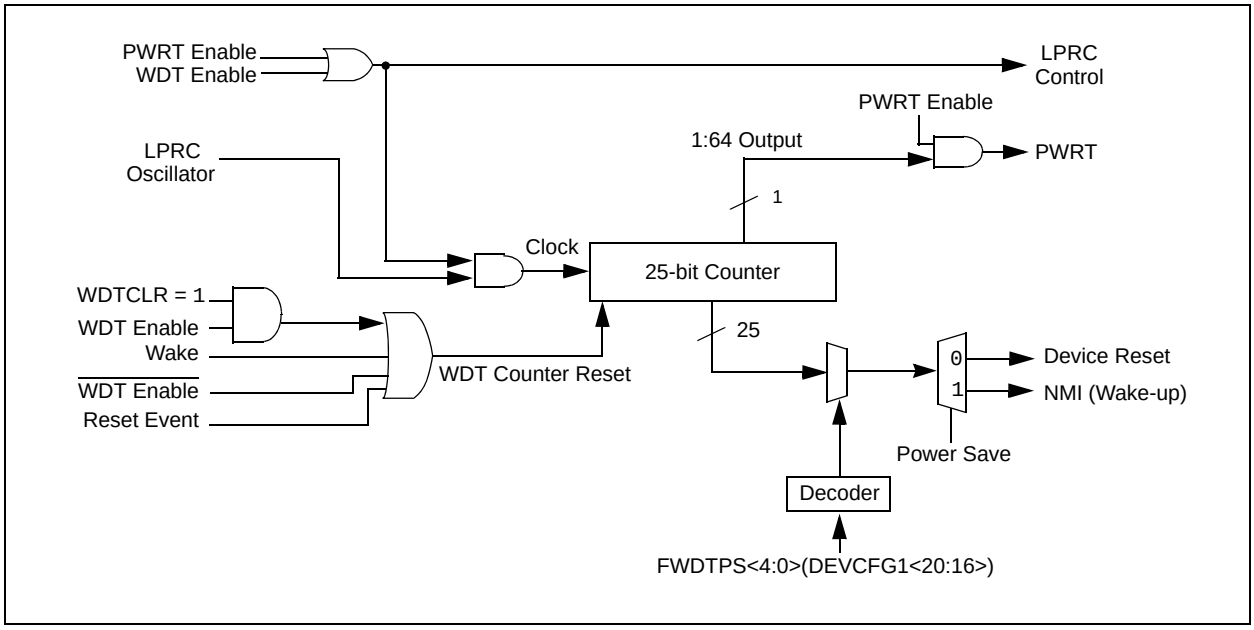


TABLE 29-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp			
Parameter No.	**Typical(2)**	**Max.**	**Units**	**Conditions**		
Power-Down Current (I_{PD})(1)						
DC40	7	30	µA	-40°C	2.3V	Base Power-Down Current **(Note 6)**
DC40a	24	30	µA	+25°C		
DC40b	205	300	µA	+85°C		
DC40h	450	900	µA	+105ºC		
DC40c	25	—	µA	+25°C	3.3V	Base Power-Down Current
DC40d	9	70	µA	-40°C	3.6V	Base Power-Down Current
DC40e	25	70	µA	+25°C		
DC40g	115	200(5)	µA	+70°C		
DC40f	200	400	µA	+85°C		
DC40i	470	1200	µA	+105ºC		
Module Differential Current						
DC41	—	10	µA	-40°C	2.3V	Watchdog Timer Current: ΔI_{WDT} **(Notes 3, 6)**
DC41a	—	10	µA	+25°C		
DC41b	—	10	µA	+85°C		
DC41g	—	12	µA	+105ºC		
DC41c	5	—	µA	+25°C	3.3V	Watchdog Timer Current: ΔI_{WDT} **(Note 3)**
DC41d	—	10	µA	-40°C	3.6V	Watchdog Timer Current: ΔI_{WDT} **(Note 3)**
DC41e	—	10	µA	+25°C		
DC41f	—	12	µA	+85°C		
DC41h	—	15	µA	+105ºC		
DC42	—	10	µA	-40°C	2.3V	RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} **(Notes 3, 6)**
DC42a	—	17	µA	+25°C		
DC42b	—	37	µA	+85°C		
DC42h	—	45	µA	+105ºC		
DC42c	23	—	µA	+25°C	3.3V	RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} **(Note 3)**
DC42e	—	10	µA	-40°C	3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} **(Note 3)**
DC42f	—	30	µA	+25°C		
DC42g	—	44	µA	+85°C		
DC42i	—	44	µA	+105ºC		

Note 1: Base I_{PD} is measured with all digital peripheral modules disabled. All I/Os are configured as inputs and pulled low. WDT and FSCM are disabled.

2: Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

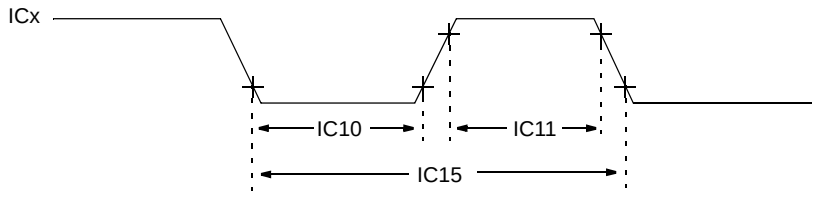
3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

4: Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

5: Data is characterized at +70°C and not tested. Parameter is for design guidance only.

6: This parameter is characterized, but not tested in manufacturing.

FIGURE 29-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS



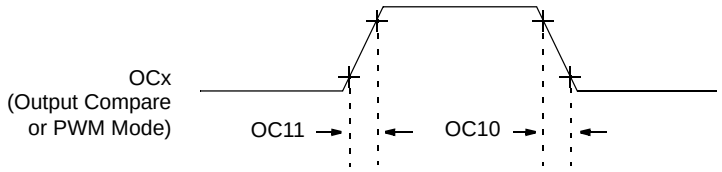
Note: Refer to Figure 29-1 for load conditions.

TABLE 29-25: INPUT CAPTURE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Max.**	**Units**	**Conditions**	
IC10	TccL	ICx Input Low Time	[(12.5 ns or 1TPB)/N] + 25 ns	—	ns	Must also meet parameter IC15.	N = prescale value (1, 4, 16)
IC11	TccH	ICx Input High Time	[(12.5 ns or 1TPB)/N] + 25 ns	—	ns	Must also meet parameter IC15.	
IC15	TccP	ICx Input Period	[(25 ns or 2TPB)/N] + 50 ns	—	ns	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 29-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS



Note: Refer to Figure 29-1 for load conditions.

TABLE 29-26: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

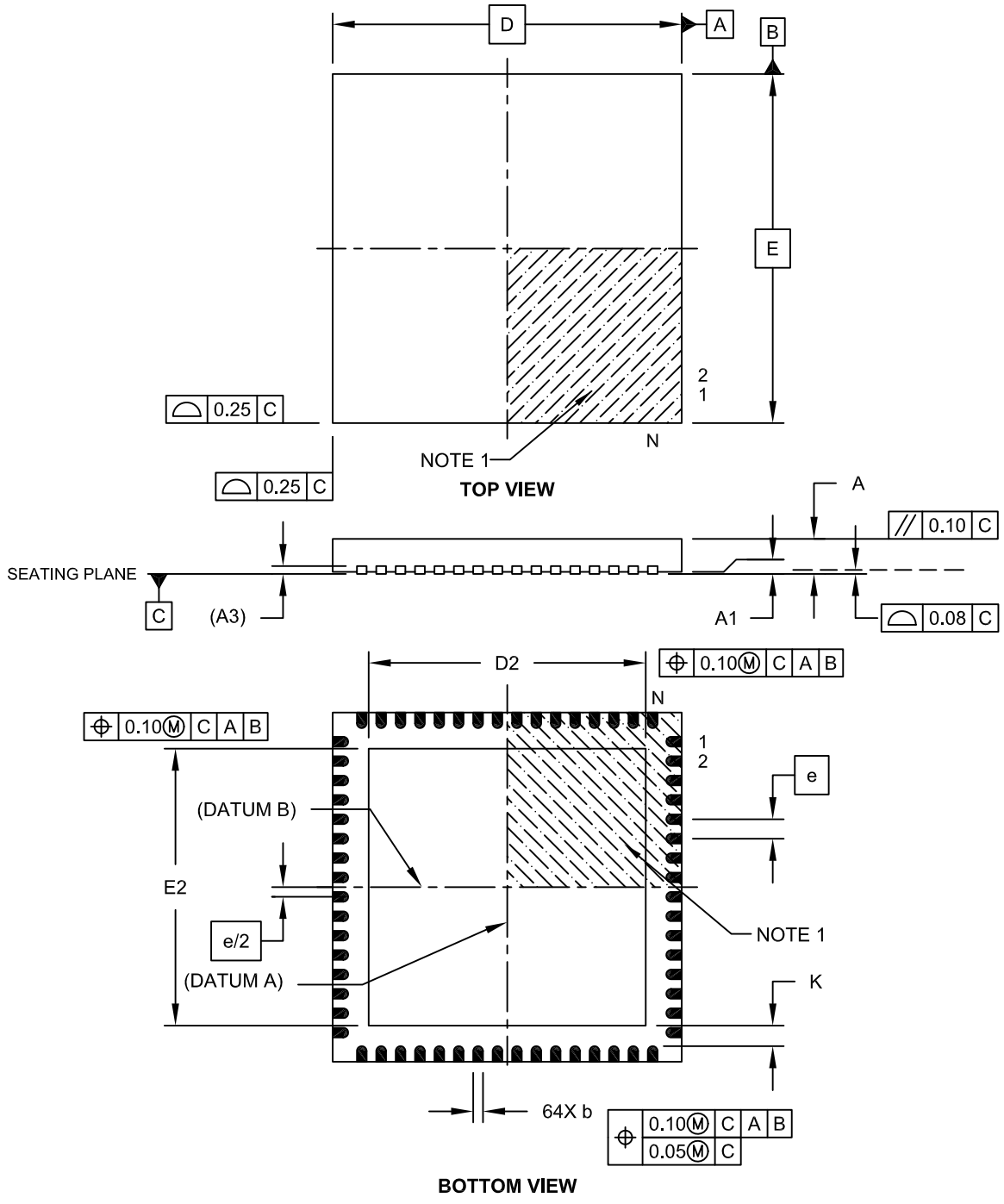
AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See parameter DO32.
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See parameter DO31.

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 7.15 x 7.15 Exposed Pad [QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-149C Sheet 1 of 2

Revision H (May 2011)

The revision includes the following global update:

- All references to VDDCORE/VCAP have been changed to: VCORE/VCAP
- Added references to the new V-Temp temperature range: -40ºC to +105ºC

This revision also includes minor typographical and formatting changes throughout the data sheet text. Major updates are referenced by their respective section in the following table.

TABLE A-3: MAJOR SECTION UPDATES

Section Name	Update Description
Section 1.0 “Device Overview”	Updated the VBUS description in **Table 1-1: “Pinout I/O Descriptions”**.
Section 4.0 “Memory Organization”	Added Note 2 and changed the RIPL<2:0> bits to SRIPL<2:0> in the Interrupt Register Map tables (see Table 4-2 through Table 4-6. Added Note 2 to the Timer1-5 Register Map (see Table 4-7). Updated the All Resets value for I2C1CON<15:0> and I2C2CON<15:0> in the I2C1 and I2C2 Register Map (see Table 4-10). Updated the All Resets value for SPI1STAT<15:0> and SPI2STAT<15:0> in the SPI1 and SPI2 Register Map (see Table 4-12). Updated the All Resets value for CM1CON<15:0> and CM2CON<15:0> in the Comparator Register Map (see Table 4-17). Renamed the RCDIV<2:0> bits to FRCDIV<2:0> and the LOCK bit to SLOCK in the OSCCON register, and added Note 3 and the SYSKEYregister to the System Control Registers Map (see Table 4-20). Updated the All Resets value for the PMSTAT register in the Parallel Master Port Register Map (see Table 4-37). Updated the All Resets value for CHECON<15:0> and CHETAG<15:0> in the Prefetch Register Map (see Table 4-39). Renamed FUPLLEN, FUPLLIDIV, and FPLLMULT in the DEVCFG2 register to: UPLLEN, UPLLIDIV, and FPLLMUL, respectively in the Device Configuration Word Summary (see Table 4-41). Added Notes 1 through 4 to the USB Register Map (see Table 4-43).
Section 5.0 “Flash Program Memory”	Added a note on Flash LVD Delay and Example 5-1.
Section 8.0 “Oscillator Configuration”	Updated the PIC32MX3XX/4XX Family Clock Diagram (see Figure 8-1).
Section 11.0 “USB On-The-Go (OTG)”	Updated the PIC32MX3XX/4XX Family USB Interface Diagram (see Figure 11-1).
Section 16.0 “Output Compare”	Updated the Output Compare Module Block Diagram (see Figure 16-1).
Section 22.0 “10-bit Analog-to-Digital Converter (ADC)”	Updated the ADC Conversion Clock Period Block Diagram (see Figure 22-2).
Section 26.0 “Special Features”	Renamed FUPLLEN, FUPLLIDIV, and FPLLMULT in the DEVCFG2 register to: UPLLEN, UPLLIDIV, and FPLLMUL, respectively (see Register 26-3).

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://microchip.com/support