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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx340f128lt-80v-pt

PIC32MX3XX/4XX

TABLE 1: PIC32MX GENERAL PURPOSE – FEATURES

GENERAL PURPOSE														
Device	Pins	Packages ⁽²⁾	MHz	Program Memory (KB)	Data Memory (KB)	Timers/Capture/Compare	Programmable DMA Channels	VREG	Trace	EUART/SPIL ² C™	10-bit ADC (ch)	Comparators	PMP/PSP	JTAG
PIC32MX320F032H	64	PT, MR	40	32 + 12 ⁽¹⁾	8	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX320F064H	64	PT, MR	80	64 + 12 ⁽¹⁾	16	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX320F128H	64	PT, MR	80	128 + 12 ⁽¹⁾	16	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX340F128H	64	PT, MR	80	128 + 12 ⁽¹⁾	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX340F256H	64	PT, MR	80	256 + 12 ⁽¹⁾	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX340F512H	64	PT, MR	80	512 + 12 ⁽¹⁾	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX320F128L	100	PT	80	128 + 12 ⁽¹⁾	16	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes
	121	BG												
PIC32MX340F128L	100	PT	80	128 + 12 ⁽¹⁾	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes
	121	BG												
PIC32MX360F256L	100	PT	80	256 + 12 ⁽¹⁾	32	5/5/5	4	Yes	Yes	2/2/2	16	2	Yes	Yes
	121	BG												
PIC32MX360F512L	100	PT	80	512 + 12 ⁽¹⁾	32	5/5/5	4	Yes	Yes	2/2/2	16	2	Yes	Yes
	121	BG												

Legend: PT = TQFP MR = QFN BG = XBGA

Note 1: This device features 12 KB Boot Flash memory.

2: See Legend for an explanation of the acronyms. See **Section 30.0 “Packaging Information”** for details.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number ⁽¹⁾			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
RD0	46	72	D9	I/O	ST	PORTD is a bidirectional I/O port.
RD1	49	76	A11	I/O	ST	
RD2	50	77	A10	I/O	ST	
RD3	51	78	B9	I/O	ST	
RD4	52	81	C8	I/O	ST	
RD5	53	82	B8	I/O	ST	
RD6	54	83	D7	I/O	ST	
RD7	55	84	C7	I/O	ST	
RD8	42	68	E9	I/O	ST	
RD9	43	69	E10	I/O	ST	
RD10	44	70	D11	I/O	ST	
RD11	45	71	C11	I/O	ST	
RD12	—	79	A9	I/O	ST	
RD13	—	80	D8	I/O	ST	
RD14	—	47	L9	I/O	ST	
RD15	—	48	K9	I/O	ST	
RE0	60	93	A4	I/O	ST	PORTE is a bidirectional I/O port.
RE1	61	94	B4	I/O	ST	
RE2	62	98	B3	I/O	ST	
RE3	63	99	A2	I/O	ST	
RE4	64	100	A1	I/O	ST	
RE5	1	3	D3	I/O	ST	
RE6	2	4	C1	I/O	ST	
RE7	3	5	D2	I/O	ST	
RE8	—	18	G1	I/O	ST	
RE9	—	19	G2	I/O	ST	
RF0	58	87	B6	I/O	ST	PORTF is a bidirectional I/O port.
RF1	59	88	A6	I/O	ST	
RF2	34	52	K11	I/O	ST	
RF3	33	51	K10	I/O	ST	
RF4	31	49	L10	I/O	ST	
RF5	32	50	L11	I/O	ST	
RF6	35	55	H9	I/O	ST	
RF7	—	54	H8	I/O	ST	
RF8	—	53	J10	I/O	ST	
RF12	—	40	K6	I/O	ST	
RF13	—	39	L6	I/O	ST	

Legend: CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = TTL input buffer

Analog = Analog input P = Power
 O = Output I = Input

Note 1: Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

3.2 Architecture Overview

The MIPS32® M4K® Processor Core contains several logic blocks working together in parallel, providing an efficient high performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CPO)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e Support
- Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The MIPS32® M4K® Processor Core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit general purpose registers used for integer operations and address calculation. One additional register file shadow set (containing thirty-two registers) is added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid stalls when executing instructions streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the CLZ and CLO instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- Shifter and Store Aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The MIPS32® M4K® Processor Core includes a multiply/divide unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the integer unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32MX core only checks the value of the latter (*rt*) operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit-wide *rs*, 15 iterations are skipped, and for a 24-bit-wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32MX core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1: MIPS® M4K® PROCESSOR CORE HIGH-PERFORMANCE INTEGER MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul <i>rt</i>) (div <i>rs</i>)	Latency	Repeat Rate
MULT/MULTU, MADD/MADDU, MSUB/MSUBU	16 bits	1	1
	32 bits	2	2
MUL	16 bits	2	1
	32 bits	3	2
DIV/DIVU	8 bits	12	11
	16 bits	19	18
	24 bits	26	25
	32 bits	33	32

The MIPS architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the general purpose register file.

In addition to the HI/LO targeted operations, the MIPS32 architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction, required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, multiply-add (MADD) and multiply-subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds

the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (kernel, user and debug), and whether interrupts are enabled or disabled. Configuration information, such as presence of options like MIPS16e, is also available by accessing the CP0 registers, listed in Table 3-2.

TABLE 3-2: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0-6	Reserved	Reserved
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers
8	BadVAddr ⁽¹⁾	Reports the address for the most recent address-related exception
9	Count ⁽¹⁾	Processor cycle count
10	Reserved	Reserved
11	Compare ⁽¹⁾	Timer interrupt control
12	Status ⁽¹⁾	Processor status and control
12	IntCtl ⁽¹⁾	Interrupt system status and control
12	SRSCtl ⁽¹⁾	Shadow register set status and control
12	SRSMap ⁽¹⁾	Provides mapping from vectored interrupt to a shadow set
13	Cause ⁽¹⁾	Cause of last general exception
14	EPC ⁽¹⁾	Program counter at last exception
15	PRId	Processor identification and revision
15	EBASE	Exception vector base register
16	Config	Configuration register
16	Config1	Configuration register 1
16	Config2	Configuration register 2
16	Config3	Configuration register 3

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TABLE 3-2: COPROCESSOR 0 REGISTERS (CONTINUED)

Register Number	Register Name	Function
17-22	Reserved	Reserved
23	Debug ⁽²⁾	Debug control and exception status
24	DEPC ⁽²⁾	Program counter at last debug exception
25-29	Reserved	Reserved
30	ErrorEPC ⁽¹⁾	Program counter at last error
31	DESAVE ⁽²⁾	Debug handler scratchpad register

Note 1: Registers used in exception processing.

2: Registers used during debug.

Coprocessor 0 also contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including alignment errors in data, external events or program errors. Table 3-3 shows the exception types in order of priority.

TABLE 3-3: PIC32MX3XX/4XX FAMILY CORE EXCEPTION TYPES

Exception	Description
Reset	Assertion $\overline{\text{MCLR}}$ or a Power-on Reset (POR)
DSS	EJTAG Debug Single Step
DINT	EJTAG Debug Interrupt. Caused by the assertion of the external <i>EJ_DINT</i> input, or by setting the <i>EjtagBrk</i> bit in the ECR register
NMI	Assertion of NMI signal
Interrupt	Assertion of unmasked hardware or software interrupt signal
DIB	EJTAG debug hardware instruction break matched
AdEL	Fetch address alignment error Fetch reference to protected address
IBE	Instruction fetch bus error
DBp	EJTAG Breakpoint (execution of SDBBP instruction)
Sys	Execution of SYSCALL instruction
Bp	Execution of BREAK instruction
RI	Execution of a Reserved Instruction
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled
CEU	Execution of a CorExtend instruction when CorExtend is not enabled
Ov	Execution of an arithmetic instruction that overflowed
Tr	Execution of a trap (when trap condition is true)
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG Data Value Break on Store (address + value)
AdEL	Load address alignment error Load reference to protected address
AdES	Store address alignment error Store to protected address
DBE	Load or store bus error
DDBL	EJTAG data hardware breakpoint matched in load data compare

4.0 MEMORY ORGANIZATION

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 3. “Memory Organization”** (DS61115) of the “*PIC32 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX3XX/4XX microcontrollers provide 4 GB of unified virtual memory address space. All memory regions including program, data memory, SFRs and Configuration registers reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX3XX/4XX to execute from data memory.

4.1 Key Features

- 32-bit native data width
- Separate User and Kernel mode address space
- Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable and non-cacheable address regions

4.2 PIC32MX3XX/4XX Memory Layout

PIC32MX3XX/4XX microcontrollers implement two address spaces: Virtual and Physical. All hardware resources such as program memory, data memory and peripherals are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by peripherals such as DMA and Flash controller that access memory independently of CPU.

6.0 RESETS

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. “Resets”** (DS61118) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

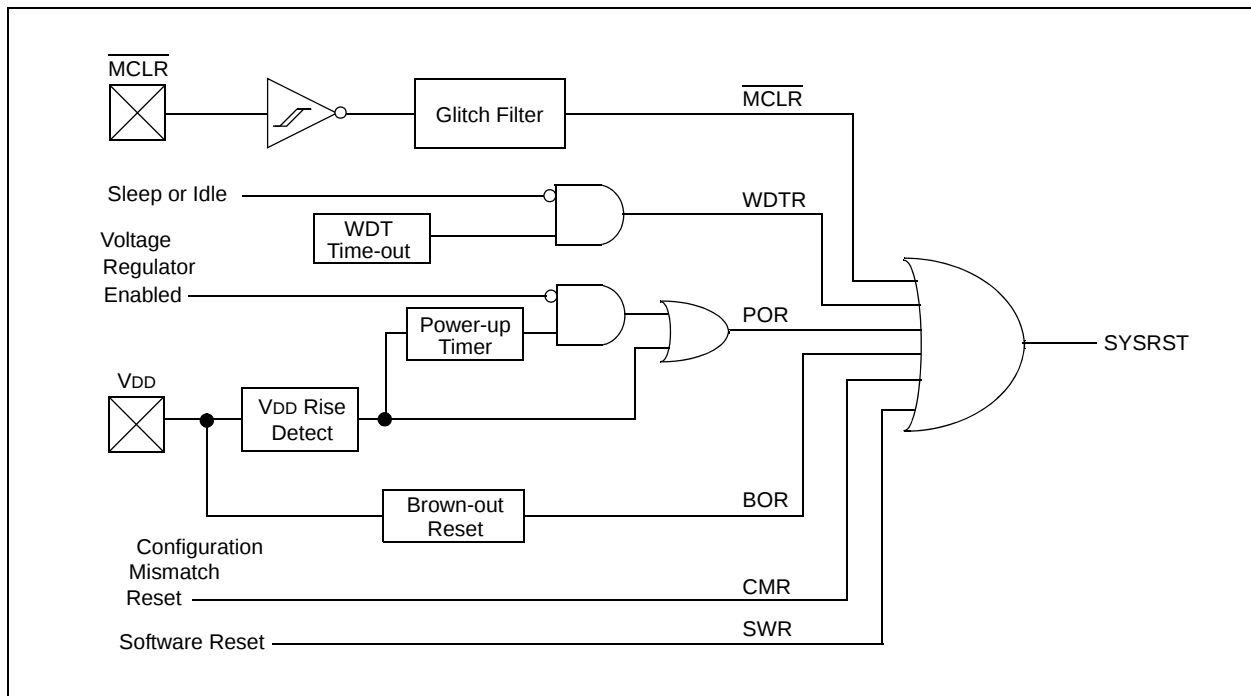
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The following is a list of device Reset sources:

- POR: Power-on Reset
- MCLR: Master Clear Reset Pin
- SWR: Software Reset
- WDTR: Watchdog Timer Reset
- BOR: Brown-out Reset
- CMR: Configuration Mismatch Reset

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM



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TABLE 7-1: INTERRUPT IRQ AND VECTOR LOCATION

Interrupt Source ⁽¹⁾	IRQ	Vector Number	Interrupt Bit Location			
Highest Natural Order Priority			Flag	Enable	Priority	Subpriority
CT – Core Timer Interrupt	0	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>
CS0 – Core Software Interrupt 0	1	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>
CS1 – Core Software Interrupt 1	2	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>
INT0 – External Interrupt 0	3	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>
T1 – Timer1	4	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>
IC1 – Input Capture 1	5	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>
OC1 – Output Compare 1	6	6	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>
INT1 – External Interrupt 1	7	7	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>
T2 – Timer2	8	8	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>
IC2 – Input Capture 2	9	9	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>
OC2 – Output Compare 2	10	10	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>
INT2 – External Interrupt 2	11	11	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>
T3 – Timer3	12	12	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>
IC3 – Input Capture 3	13	13	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>
OC3 – Output Compare 3	14	14	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>
INT3 – External Interrupt 3	15	15	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>
T4 – Timer4	16	16	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>
IC4 – Input Capture 4	17	17	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>
OC4 – Output Compare 4	18	18	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>
INT4 – External Interrupt 4	19	19	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>
T5 – Timer5	20	20	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>
IC5 – Input Capture 5	21	21	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>
OC5 – Output Compare 5	22	22	IFS0<22>	IEC0<22>	IPC5<20:18>	IPC5<17:16>
SPI1E – SPI1 Fault	23	23	IFS0<23>	IEC0<23>	IPC5<28:26>	IPC5<25:24>
SPI1TX – SPI1 Transfer Done	24	23	IFS0<24>	IEC0<24>	IPC5<28:26>	IPC5<25:24>
SPI1RX – SPI1 Receive Done	25	23	IFS0<25>	IEC0<25>	IPC5<28:26>	IPC5<25:24>
U1E – UART1 Error	26	24	IFS0<26>	IEC0<26>	IPC6<4:2>	IPC6<1:0>
U1RX – UART1 Receiver	27	24	IFS0<27>	IEC0<27>	IPC6<4:2>	IPC6<1:0>
U1TX – UART1 Transmitter	28	24	IFS0<28>	IEC0<28>	IPC6<4:2>	IPC6<1:0>
I2C1B – I2C1 Bus Collision Event	29	25	IFS0<29>	IEC0<29>	IPC6<12:10>	IPC6<9:8>
I2C1S – I2C1 Slave Event	30	25	IFS0<30>	IEC0<30>	IPC6<12:10>	IPC6<9:8>
I2C1M – I2C1 Master Event	31	25	IFS0<31>	IEC0<31>	IPC6<12:10>	IPC6<9:8>
CN – Input Change Interrupt	32	26	IFS1<0>	IEC1<0>	IPC6<20:18>	IPC6<17:16>
AD1 – ADC1 Convert Done	33	27	IFS1<1>	IEC1<1>	IPC6<28:26>	IPC6<25:24>
PMP – Parallel Master Port	34	28	IFS1<2>	IEC1<2>	IPC7<4:2>	IPC7<1:0>
CMP1 – Comparator Interrupt	35	29	IFS1<3>	IEC1<3>	IPC7<12:10>	IPC7<9:8>
CMP2 – Comparator Interrupt	36	30	IFS1<4>	IEC1<4>	IPC7<20:18>	IPC7<17:16>

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MX General Purpose – Features”** and **TABLE 2: “PIC32MX USB – Features”** for available peripherals.

PIC32MX3XX/4XX

NOTES:

FIGURE 19-4: UART RECEPTION

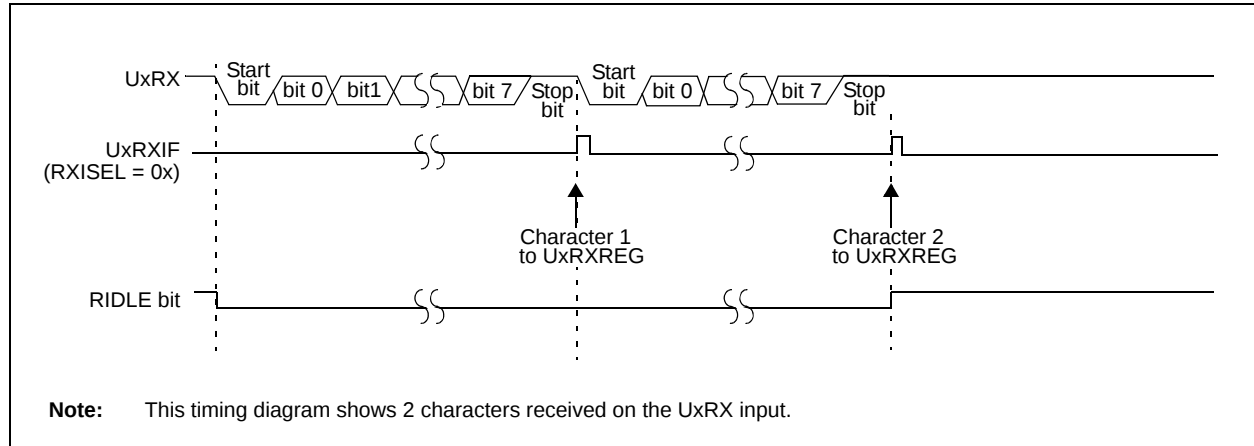
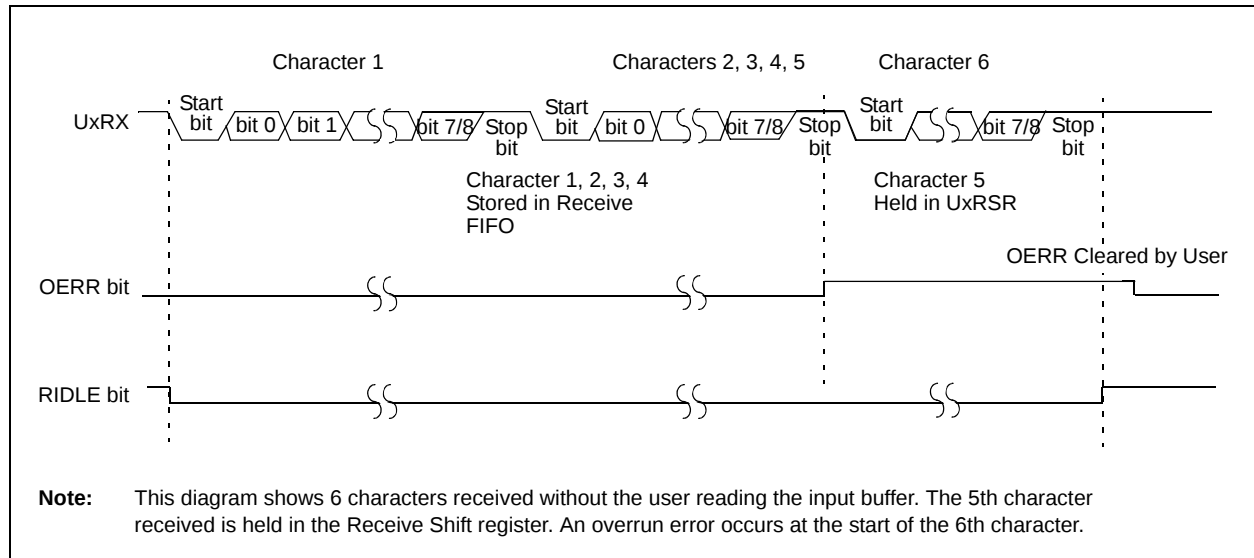


FIGURE 19-5: UART RECEPTION WITH RECEIVE OVERRUN



20.0 PARALLEL MASTER PORT (PMP)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. “Parallel Master Port (PMP)”** (DS61128) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The PMP is a parallel 8-bit/16-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable.

Key features of the PMP module include:

- 8-bit,16-bit interface
- Up to 16 programmable address lines
- Up to two Chip Select lines
- Programmable strobe options
 - Individual read and write strobes, or
 - Read/write strobe with enable strobe
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- Parallel Slave Port support
 - Legacy addressable
 - Address support
 - 4-byte deep auto-incrementing buffer
- Programmable Wait states
- Operate during CPU Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers
- Freeze option for in-circuit debugging

Note: On 64-pin devices, data pins PMD<15:8> are not available.

FIGURE 20-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES

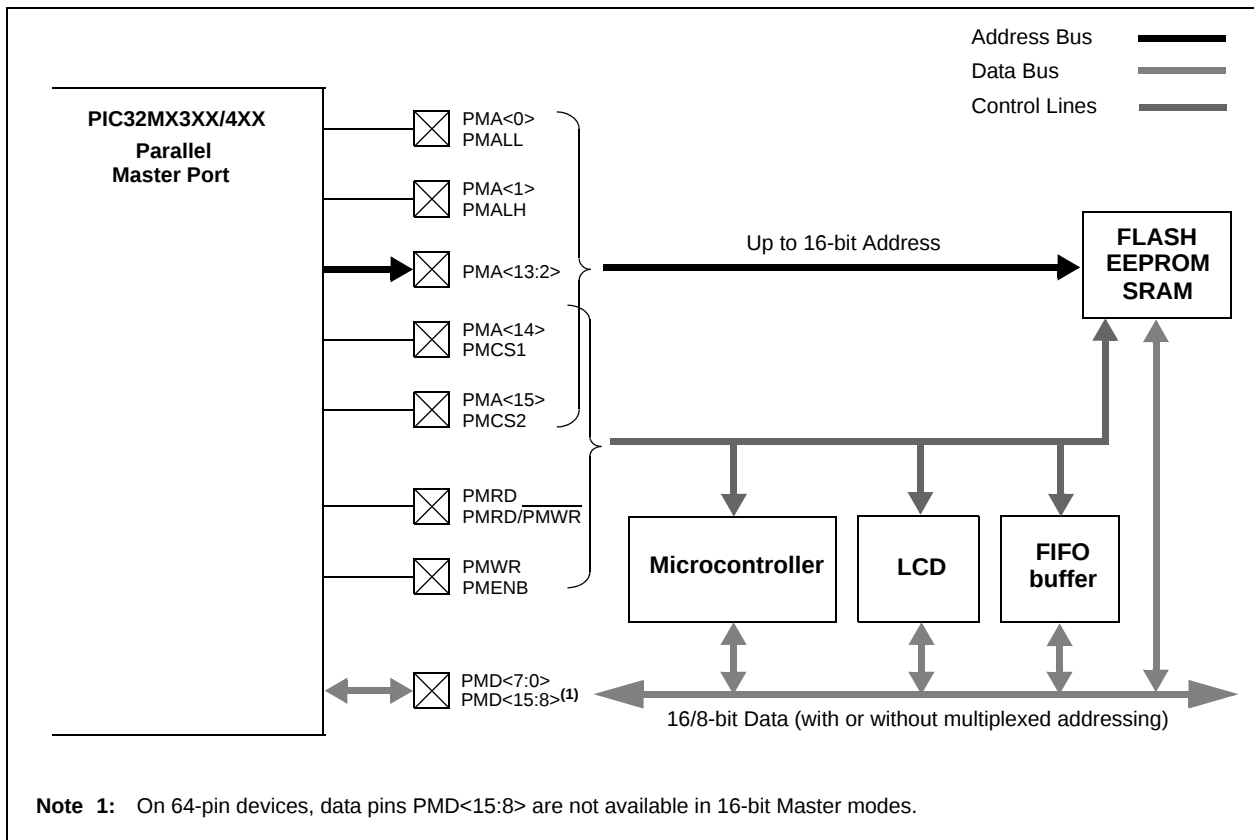


TABLE 29-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)		
			Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp		
Parameter No.	Typical ⁽²⁾	Max.	Units	Conditions	
Power-Down Current (IPD) ⁽¹⁾					
DC40	7	30	μA	-40°C	2.3V Base Power-Down Current (Note 6)
DC40a	24	30	μA	+25°C	
DC40b	205	300	μA	+85°C	
DC40h	450	900	μA	+105°C	
DC40c	25	—	μA	+25°C	3.3V Base Power-Down Current
DC40d	9	70	μA	-40°C	3.6V Base Power-Down Current
DC40e	25	70	μA	+25°C	
DC40g	115	200 ⁽⁵⁾	μA	+70°C	
DC40f	200	400	μA	+85°C	
DC40i	470	1200	μA	+105°C	
Module Differential Current					
DC41	—	10	μA	-40°C	2.3V Watchdog Timer Current: ΔI _{WDT} (Notes 3, 6)
DC41a	—	10	μA	+25°C	
DC41b	—	10	μA	+85°C	
DC41g	—	12	μA	+105°C	
DC41c	5	—	μA	+25°C	3.3V Watchdog Timer Current: ΔI _{WDT} (Note 3)
DC41d	—	10	μA	-40°C	3.6V Watchdog Timer Current: ΔI _{WDT} (Note 3)
DC41e	—	10	μA	+25°C	
DC41f	—	12	μA	+85°C	
DC41h	—	15	μA	+105°C	
DC42	—	10	μA	-40°C	2.3V RTCC + Timer1 w/32 kHz Crystal: ΔI _{RTCC} (Notes 3, 6)
DC42a	—	17	μA	+25°C	
DC42b	—	37	μA	+85°C	
DC42h	—	45	μA	+105°C	
DC42c	23	—	μA	+25°C	3.3V RTCC + Timer1 w/32 kHz Crystal: ΔI _{RTCC} (Note 3)
DC42e	—	10	μA	-40°C	3.6V RTCC + Timer1 w/32 kHz Crystal: ΔI _{RTCC} (Note 3)
DC42f	—	30	μA	+25°C	
DC42g	—	44	μA	+85°C	
DC42i	—	44	μA	+105°C	

- Note 1:** Base IPD is measured with all digital peripheral modules disabled. All I/Os are configured as inputs and pulled low. WDT and FSCM are disabled.
- 2:** Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.
- 4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.
- 5:** Data is characterized at +70°C and not tested. Parameter is for design guidance only.
- 6:** This parameter is characterized, but not tested in manufacturing.

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TABLE 29-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
DO10 DO16	VOL	Output Low Voltage I/O Ports	—	—	0.4	V	IO _L = 7 mA, V _{DD} = 3.6V
			—	—	0.4	V	IO _L = 6 mA, V _{DD} = 2.3V
		OSC2/CLKO	—	—	0.4	V	IO _L = 3.5 mA, V _{DD} = 3.6V
			—	—	0.4	V	IO _L = 2.5 mA, V _{DD} = 2.3V
DO20 DO26	VOH	Output High Voltage I/O Ports	2.4	—	—	V	IO _H = -12 mA, V _{DD} = 3.6V
			1.4	—	—	V	IO _H = -12 mA, V _{DD} = 2.3V
		OSC2/CLKO	2.4	—	—	V	IO _H = -12 mA, V _{DD} = 3.6V
			1.4	—	—	V	IO _H = -12 mA, V _{DD} = 2.3V

TABLE 29-10: ELECTRICAL CHARACTERISTICS: BROWN-OUT RESET (BOR)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
BO10	VBOR	BOR Event on V _{DD} transition high-to-low	2.0	—	2.3	V	—

TABLE 29-18: PLL CLOCK TIMING SPECIFICATIONS (V_{DD} = 2.3V TO 3.6V)

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤T _A ≤+85°C for Industrial -40°C ≤T _A ≤+105°C for V-Temp					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical	Max.	Units	Conditions
OS50	FPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	4	—	5	MHz	ECPLL, HSPLL, XTPLL, FRCPLL modes
OS51	FSYS	On-Chip VCO System Frequency	60	—	120	MHz	—
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	2	ms	—
OS53	DCLK	CLKO Stability ⁽²⁾ (Period Jitter or Cumulative)	-0.25	—	+0.25	%	Measured over 100 ms period

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{SYSCLK}{CommunicationClock}}}$$

For example, if SYSCLK = 80 MHz and SPI bit rate = 20 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{80}{20}}} = \frac{D_{CLK}}{2}$$

TABLE 29-19: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤T _A ≤+85°C for Industrial -40°C ≤T _A ≤+105°C for V-Temp				
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions
Internal FRC Accuracy @ 8.00 MHz ⁽¹⁾						
F20	FRC	-2	—	+2	%	—

Note 1: Frequency calibrated at 25°C and 3.3V. TUN bits can be used to compensate for temperature drift.

TABLE 29-20: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤T _A ≤+85°C for Industrial -40°C ≤T _A ≤+105°C for V-Temp				
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions
LPRC @ 31.25 kHz ⁽¹⁾						
F21	LPRC	-15	—	+15	%	—

Note 1: Change of LPRC frequency as V_{DD} changes.

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TABLE 29-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	μs	PBCLK must operate at a minimum of 800 KHz.
			400 kHz mode	1.3	—	μs	PBCLK must operate at a minimum of 3.2 MHz.
			1 MHz mode ⁽¹⁾	0.5	—	μs	—
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μs	PBCLK must operate at a minimum of 800 KHz.
			400 kHz mode	0.6	—	μs	PBCLK must operate at a minimum of 3.2 MHz.
			1 MHz mode ⁽¹⁾	0.5	—	μs	—
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF.
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode ⁽¹⁾	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF.
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode ⁽¹⁾	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode ⁽¹⁾	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	—
			400 kHz mode	0	0.9	μs	
			1 MHz mode ⁽¹⁾	0	0.3	μs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4700	—	ns	Only relevant for Repeated Start condition.
			400 kHz mode	600	—	ns	
			1 MHz mode ⁽¹⁾	250	—	ns	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated.
			400 kHz mode	600	—	ns	
			1 MHz mode ⁽¹⁾	250	—	ns	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
			1 MHz mode ⁽¹⁾	600	—	ns	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
			1 MHz mode ⁽¹⁾	250	—	ns	
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	ns	—
			400 kHz mode	0	1000	ns	
			1 MHz mode ⁽¹⁾	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus must be free before a new transmission can start.
			400 kHz mode	1.3	—	μs	
			1 MHz mode ⁽¹⁾	0.5	—	μs	
IS50	Cb	Bus Capacitive Loading		—	400	pF	—

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

FIGURE 29-22: PARALLEL MASTER PORT WRITE TIMING DIAGRAM

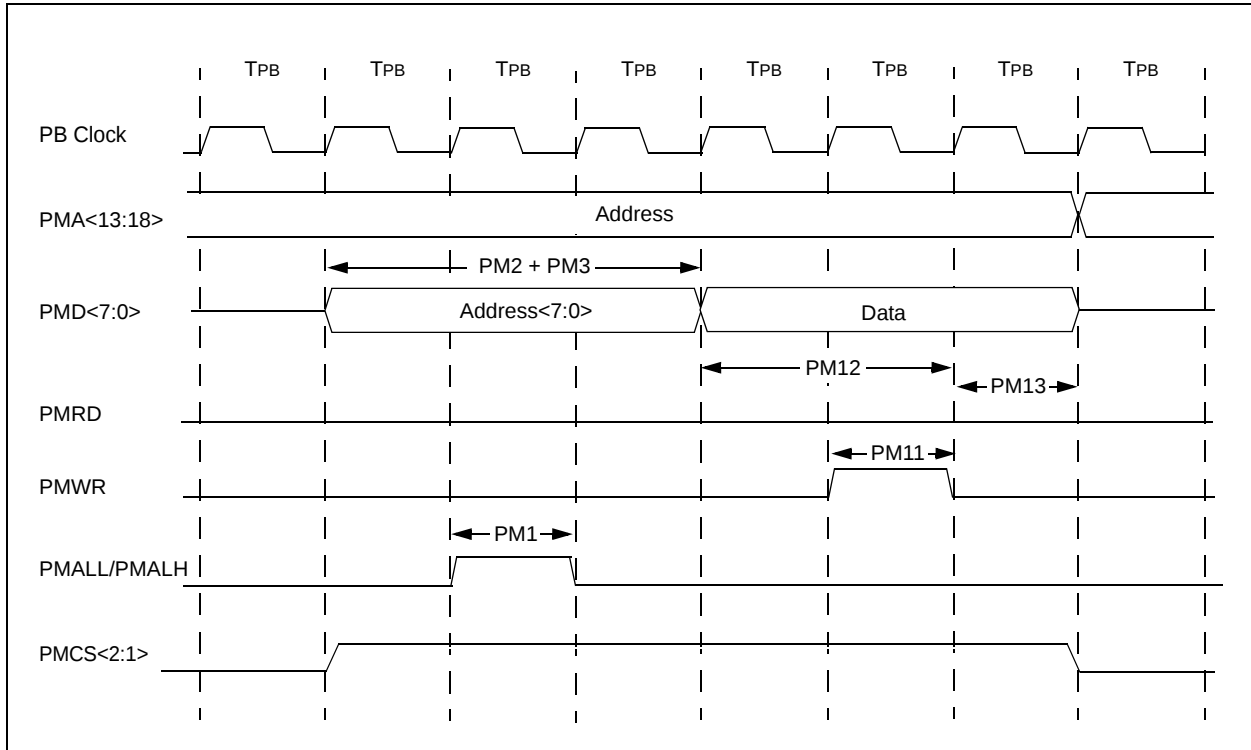


TABLE 29-39: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical	Max.	Units	Conditions
PM11	TWR	PMWR Pulse Width	—	1 TPB	—	—	—
PM12	TDVSU	Data Out Valid before PMWR or PMENB goes Inactive (data setup time)	—	2 TPB	—	—	—
PM13	TDVHOLD	PMWR or PMEMB Invalid to Data Out Invalid (data hold time)	—	1 TPB	—	—	—

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 29-23: EJTAG TIMING CHARACTERISTICS

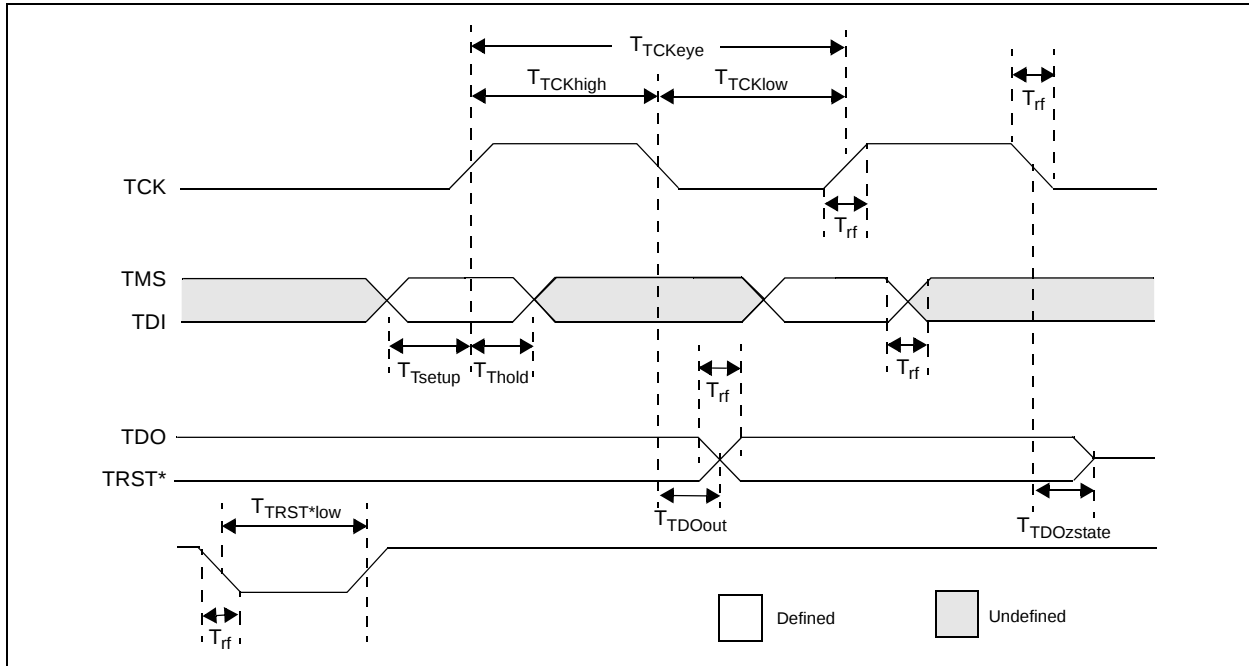


TABLE 29-41: EJTAG TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp		
Param. No.	Symbol	Description ⁽¹⁾	Min.	Max.	Units	Conditions
EJ1	TTCKCYC	TCK Cycle Time	25	—	ns	—
EJ2	TTCKHIGH	TCK High Time	10	—	ns	—
EJ3	TTCKLOW	TCK Low Time	10	—	ns	—
EJ4	TTSETUP	TAP Signals Setup Time Before Rising TCK	5	—	ns	—
EJ5	TTHOLD	TAP Signals Hold Time After Rising TCK	3	—	ns	—
EJ6	TTDOOUT	TDO Output Delay Time from Falling TCK	—	5	ns	—
EJ7	TTDOZSTATE	TDO 3-State Delay Time from Falling TCK	—	5	ns	—
EJ8	TTRSTLOW	TRST Low Time	25	—	ns	—
EJ9	TRF	TAP Signals Rise/Fall Time, All Input and Output	—	—	ns	—

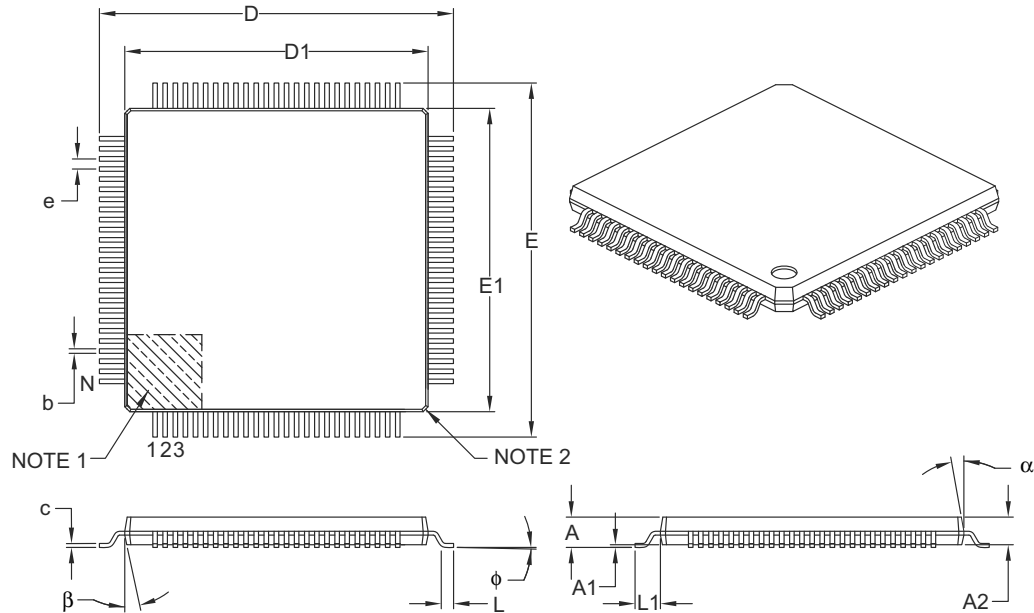
Note 1: These parameters are characterized, but not tested in manufacturing.

PIC32MX3XX/4XX

NOTES:

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	100		
Lead Pitch	e	0.40 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	14.00 BSC		
Overall Length	D	14.00 BSC		
Molded Package Width	E1	12.00 BSC		
Molded Package Length	D1	12.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.13	0.18	0.23
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

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