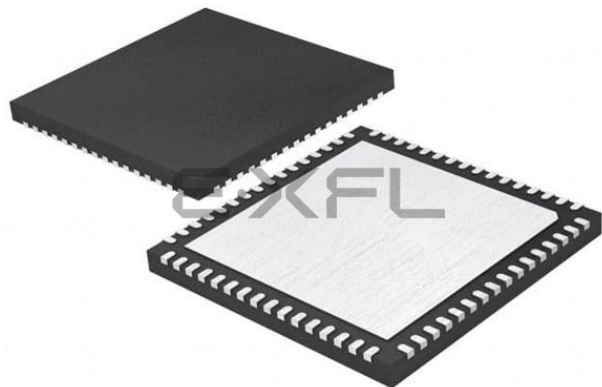




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx340f256h-80v-mr

PIC32MX3XX/4XX

High-Performance, General Purpose and USB 32-bit Flash Microcontrollers

High-Performance 32-bit RISC CPU:

- MIPS32® M4K® 32-bit core with 5-stage pipeline
- 80 MHz maximum frequency
- 1.56 DMIPS/MHz (Dhrystone 2.1) performance at 0 wait state Flash access
- Single-cycle multiply and high-performance divide unit
- MIPS16e® mode for up to 40% smaller code size
- Two sets of 32 core register files (32-bit) to reduce interrupt latency
- Prefetch Cache module to speed execution from Flash

Microcontroller Features:

- Operating temperature range of -40°C to +105°C
- Operating voltage range of 2.3V to 3.6V
- 32K to 512K Flash memory (plus an additional 12 KB of boot Flash)
- 8K to 32K SRAM memory
- Pin-compatible with most PIC24/dsPIC® DSC devices
- Multiple power management modes
- Multiple interrupt vectors with individually programmable priority
- Fail-Safe Clock Monitor Mode
- Configurable Watchdog Timer with on-chip Low-Power RC Oscillator for reliable operation

Peripheral Features:

- Atomic SET, CLEAR and INVERT operation on select peripheral registers
- Up to 4-channel hardware DMA with automatic data size detection
- USB 2.0-compliant full-speed device and On-The-Go (OTG) controller
- USB has a dedicated DMA channel
- 3 MHz to 25 MHz crystal oscillator
- Internal 8 MHz and 32 kHz oscillators

- Separate PLLs for CPU and USB clocks
- Two I²C™ modules
- Two UART modules with:
 - RS-232, RS-485 and LIN support
 - IrDA® with on-chip hardware encoder and decoder
- Up to two SPI modules
- Parallel Master and Slave Port (PMP/PSP) with 8-bit and 16-bit data and up to 16 address lines
- Hardware Real-Time Clock and Calendar (RTCC)
- Five 16-bit Timers/Counters (two 16-bit pairs combine to create two 32-bit timers)
- Five capture inputs
- Five compare/PWM outputs
- Five external interrupt pins
- High-Speed I/O pins capable of toggling at up to 80 MHz
- High-current sink/source (18 mA/18 mA) on all I/O pins
- Configurable open-drain output on digital I/O pins

Debug Features:

- Two programming and debugging Interfaces:
 - 2-wire interface with unintrusive access and real-time data exchange with application
 - 4-wire MIPS® standard enhanced JTAG interface
- Unintrusive hardware-based instruction trace
- IEEE Standard 1149.2-compatible (JTAG) boundary scan

Analog Features:

- Up to 16-channel 10-bit Analog-to-Digital Converter:
 - 1000 ksps conversion rate
 - Conversion available during Sleep, Idle
- Two Analog Comparators

Pin Diagrams (Continued)

64-Pin TQFP (General Purpose)

■ = Pins are up to 5V tolerant

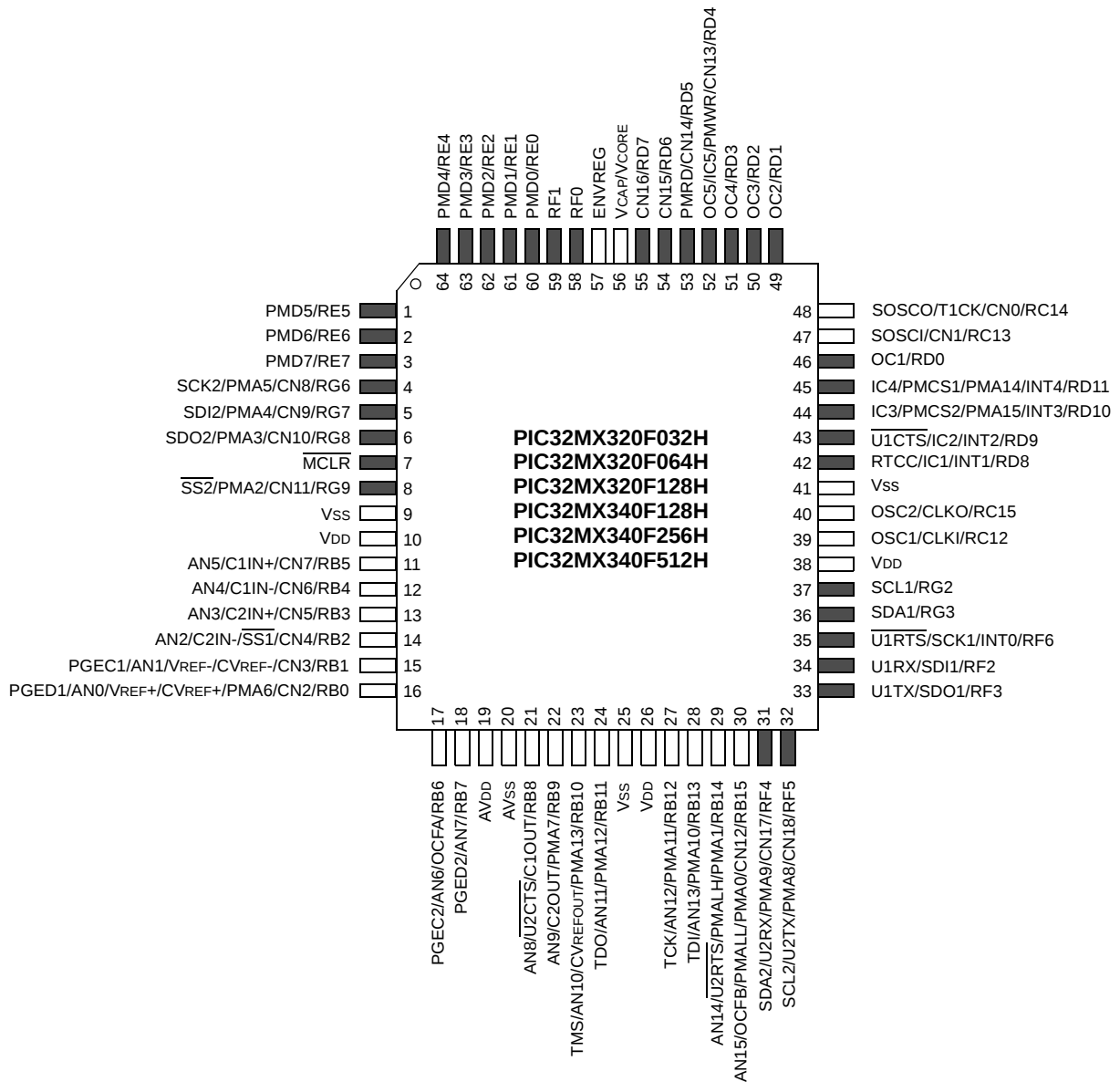


TABLE 4: PIN NAMES: PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES (CONTINUED)

Pin Number	Full Pin Name
K4	AN8/C1OUT/RB8
K5	No Connect (NC)
K6	U2CTS/RF12
K7	AN14/PMALH/PMA1/RB14
K8	VDD
K9	U1RTS/CN21/RD15
K10	USBID/RF3
K11	U1RX/RF2
L1	PGEC2/AN6/OCFA/RB6
L2	VREF-/CVREF-/PMA7/RA9

Pin Number	Full Pin Name
L3	AVSS
L4	AN9/C2OUT/RB9
L5	AN10/CVREFOUT/PMA13/RB10
L6	U2RTS/RF13
L7	AN13/PMA10/RB13
L8	AN15/OCFB/PMALL/PMA0/CN12/RB15
L9	U1CTS/CN20/RD14
L10	U2RX/PMA9/CN17/RF4
L11	U2TX/PMA8/CN18/RF5

PIC32MX3XX/4XX

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number ⁽¹⁾			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
RG0	—	90	A5	I/O	ST	PORTG is a bidirectional I/O port.
RG1	—	89	E6	I/O	ST	
RG6	4	10	E3	I/O	ST	
RG7	5	11	F4	I/O	ST	
RG8	6	12	F2	I/O	ST	
RG9	8	14	F3	I/O	ST	
RG12	—	96	C3	I/O	ST	
RG13	—	97	A3	I/O	ST	
RG14	—	95	C4	I/O	ST	
RG15	—	1	B2	I/O	ST	
RG2	37	57	H10	I	ST	PORTG input pins.
RG3	36	56	J11	I	ST	
T1CK	48	74	B11	I	ST	Timer1 external clock input.
T2CK	—	6	D1	I	ST	Timer2 external clock input.
T3CK	—	7	E4	I	ST	Timer3 external clock input.
T4CK	—	8	E2	I	ST	Timer4 external clock input.
T5CK	—	9	E1	I	ST	Timer5 external clock input.
U1CTS	43	47	L9	I	ST	UART1 clear to send.
U1RTS	35, 49	48	K9	O	—	UART1 ready to send.
U1RX	34, 50	52	K11	I	ST	UART1 receive.
U1TX	33, 51	51, 53	J10, K10	O	—	UART1 transmit.
U2CTS	21	40	K6	I	ST	UART2 clear to send.
U2RTS	29	39	L6	O	—	UART2 ready to send.
U2RX	31	49	L10	I	ST	UART2 receive.
U2TX	32	50	L11	O	—	UART2 transmit.
SCK1	35	55, 70	D11, H9	I/O	ST	Synchronous serial clock input/output for SPI1.
SDI1	34	9, 54	E1, H8	I	ST	SPI1 data in.
SDO1	33	53, 72	D9, J10	O	—	SPI1 data out.
SS1	14	23, 69	E10, J2	I/O	ST	SPI1 slave synchronization or frame pulse I/O.
SCK2	4	10	E3	I/O	ST	Synchronous serial clock input/output for SPI2.
SDI2	5	11	F4	I	ST	SPI2 data in.
SDO2	6	12	F2	O	—	SPI2 data out.
SS2	8	14	F3	I/O	ST	SPI2 slave synchronization or frame pulse I/O.
SCL1	37, 44	57, 66	E11, H10	I/O	ST	Synchronous serial clock input/output for I2C1.
SDA1	36, 43	56, 67	E8, J11	I/O	ST	Synchronous serial data input/output for I2C1.
SCL2	32	58	H11	I/O	ST	Synchronous serial clock input/output for I2C2.
SDA2	31	59	G10	I/O	ST	Synchronous serial data input/output for I2C2.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = TTL input buffer

Note 1: Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

PIC32MX3XX/4XX

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number ⁽¹⁾			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
PMD0	60	93	A4	I/O	TTL/ST	Parallel Master Port Data (De-multiplexed Master mode) or Address/Data (Multiplexed Master modes).
PMD1	61	94	B4	I/O	TTL/ST	
PMD2	62	98	B3	I/O	TTL/ST	
PMD3	63	99	A2	I/O	TTL/ST	
PMD4	64	100	A1	I/O	TTL/ST	
PMD5	1	3	D3	I/O	TTL/ST	
PMD6	2	4	C1	I/O	TTL/ST	
PMD7	3	5	D2	I/O	TTL/ST	
PMD8	—	90	A5	I/O	TTL/ST	
PMD9	—	89	E6	I/O	TTL/ST	
PMD10	—	88	A6	I/O	TTL/ST	
PMD11	—	87	B6	I/O	TTL/ST	
PMD12	—	79	A9	I/O	TTL/ST	
PMD13	—	80	D8	I/O	TTL/ST	
PMD14	—	83	D7	I/O	TTL/ST	
PMD15	—	84	C7	I/O	TTL/ST	
PMRD	53	82	B8	O	—	Parallel Master Port Read Strobe.
PMWR	52	81	C8	O	—	Parallel Master Port Write Strobe.
PMALL	30	44	L8	O	—	Parallel Master Port Address Latch Enable low-byte (Multiplexed Master modes).
PMALH	29	43	K7	O	—	Parallel Master Port Address Latch Enable high-byte (Multiplexed Master modes).
VBUS	34	54	H8	I	Analog	USB Bus Power Monitor.
VUSB	35	55	H9	P	—	USB Internal Transceiver Supply. If the USB module is <i>not</i> used, this pin must be connected to VDD.
VBUSON	11	20	H1	O	—	USB Host and OTG Bus Power Control Output.
D+	37	57	H10	I/O	Analog	USB D+.
D-	36	56	J11	I/O	Analog	USB D-.
USBID	33	51	K10	I	ST	USB OTG ID Detect.
ENVREG	57	86	A7	I	ST	Enable for On-Chip Voltage Regulator.
TRCLK	—	91	C5	O	—	Trace Clock.
TRD0	—	97	A3	O	—	Trace Data Bits 0-3.
TRD1	—	96	C3	O	—	
TRD2	—	95	C4	O	—	
TRD3	—	92	B5	O	—	
PGED1	16	25	K2	I/O	ST	Data I/O pin for programming/debugging communication channel 1.
PGEC1	15	24	K1	I	ST	Clock input pin for programming/debugging communication channel 1.

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer

Analog = Analog input
O = Output

P = Power
I = Input

Note 1: Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

3.3 Power Management

The MIPS32® M4K® Processor Core offers a number of power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or halting the clocks, which reduces system power consumption during idle periods.

3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking power-down mode is through execution of the WAIT instruction. For more information on power management, see **Section 25.0 “Power-Saving Features”**.

3.3.2 LOCAL CLOCK GATING

The majority of the power consumed by the PIC32MX3XX/4XX family core is in the clock tree and clocking registers. The PIC32MX family uses extensive use of local gated-clocks to reduce this dynamic power consumption.

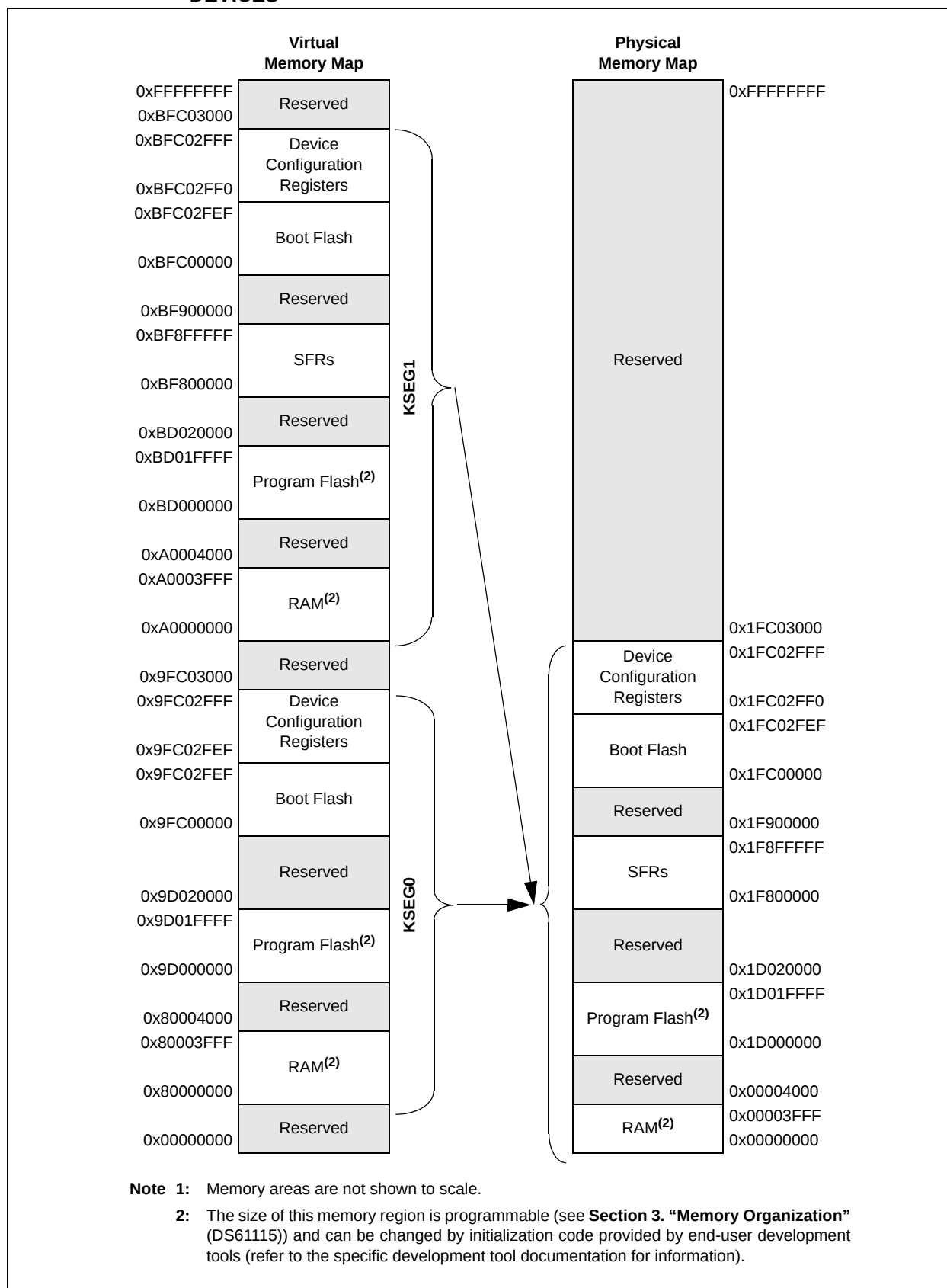
3.4 EJTAG Debug Support

The MIPS32® M4K® Processor Core provides for an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard user mode and kernel modes of operation, the core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a debug exception return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define what registers are selected and how they are used.

PIC32MX3XX/4XX

FIGURE 4-3: MEMORY MAP ON RESET FOR PIC32MX320F128H AND PIC32MX320F128L DEVICES⁽¹⁾



Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 4-16: DMA CHANNELS 0-3 REGISTERS MAP FOR PIC32MX340FXXX/360FXXX/440FXXX/460XXX DEVICES ONLY⁽¹⁾ (CONTINUED)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3160	DCH1DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
3170	DCH1SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	CHSSIZ<7:0>								0000	
3180	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	CHDSIZ<7:0>								0000	
3190	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	CHSPTR<7:0>								0000	
31A0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	CHDPTR<7:0>								0000	
31B0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	CHCSIZ<7:0>								0000	
31C0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	CHCPTR<7:0>								0000	
31D0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	CHPDAT<7:0>								0000	
31E0	DCH2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	0000	
31F0	DCH2ECON	31:16	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF	
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
3200	DCH2INT	31:16	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000	
		15:0	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000	
3210	DCH2SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
3220	DCH2DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
3230	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	CHSSIZ<7:0>								0000	
3240	DCH2DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	CHDSIZ<7:0>								0000	
3250	DCH2SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	CHSPTR<7:0>								0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers except DCHxSPTR, DCHxDPTR and DCHxCPTR have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-23: PORTC REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L, PIC32MX360F512L, PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY⁽¹⁾

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6080	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	TRISC4	TRISC3	TRISC2	TRISC1	—	F01E
6090	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	RC4	RC3	RC2	RC1	—	xxxx
60A0	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	LATC4	LATC3	LATC2	LATC1	—	xxxx
60B0	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	ODCC4	ODCC3	ODCC2	ODCC1	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 4-24: PORTC REGISTERS MAP FOR PIC32MX320F032H, PIC32MX320F064H, PIC32MX320F128H, PIC32MX340F128H, PIC32MX340F256H, PIC32MX340F512H, PIC32MX420F032H, PIC32MX440F128H, PIC32MX440F256H AND PIC32MX440F512H DEVICES ONLY⁽¹⁾

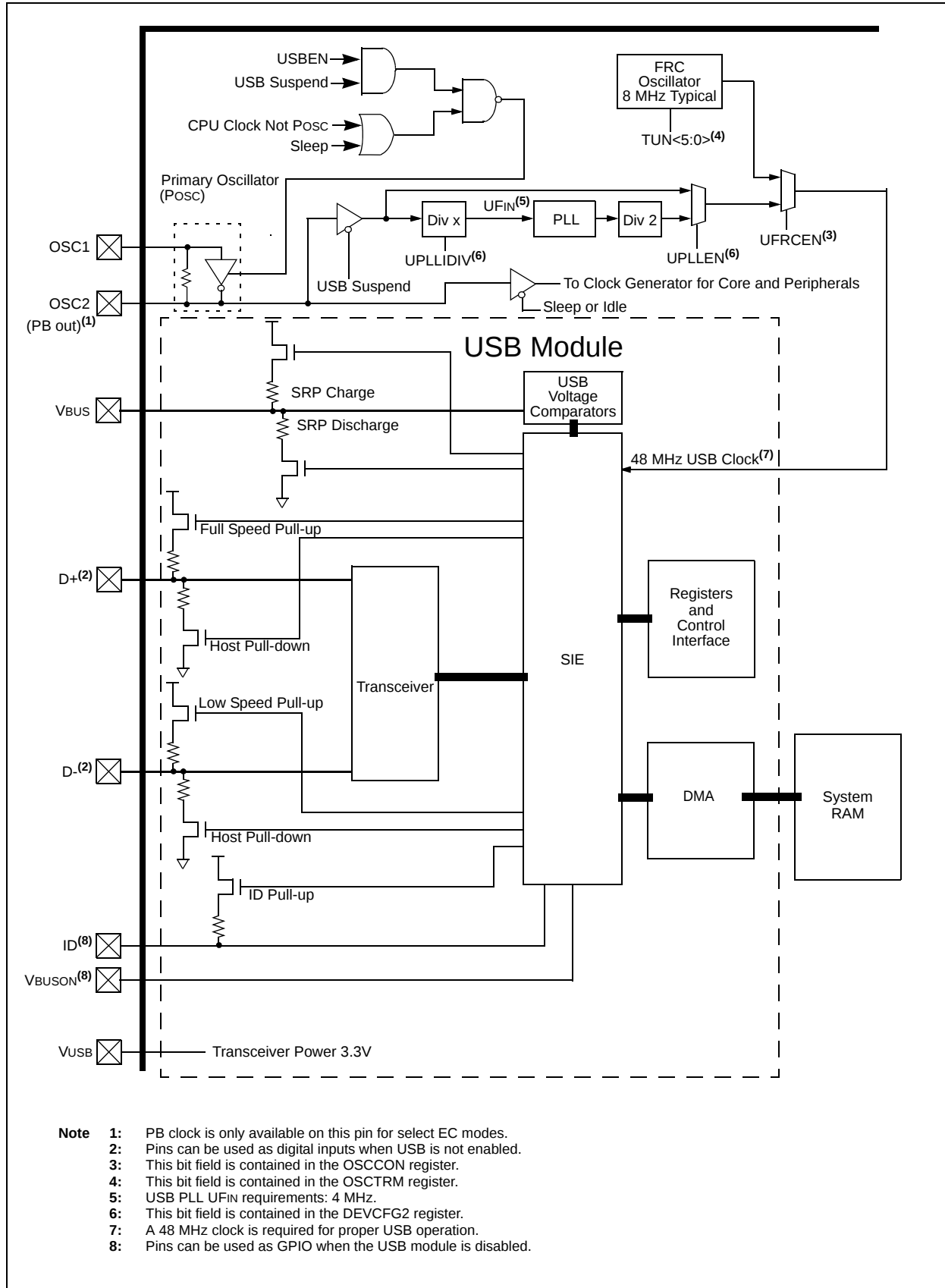
Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6080	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	—	—	—	—	—	F000
6090	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
60A0	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
60B0	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

PIC32MX3XX/4XX

FIGURE 11-1: PIC32MX3XX/4XX FAMILY USB INTERFACE DIAGRAM



19.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. “Universal Asynchronous Receiver Transmitter (UART)”** (DS61107) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

Note 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

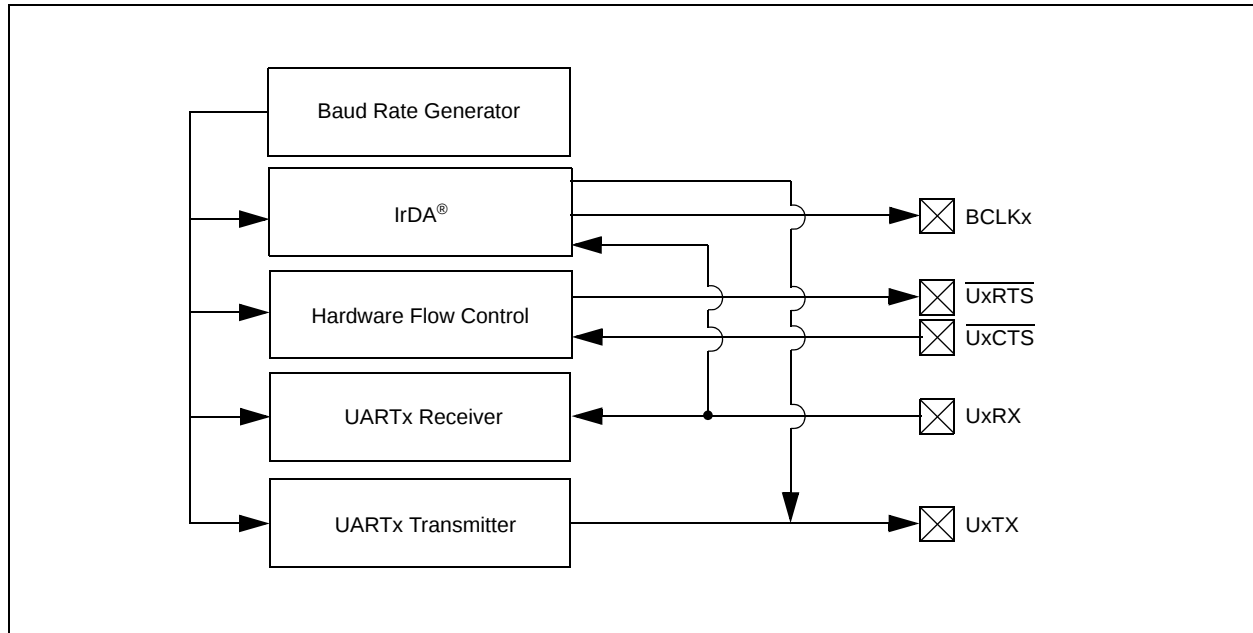
The UART module is one of the serial I/O modules available in PIC32MX3XX/4XX family devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols such as RS-232, RS-485, LIN 1.2 and IrDA®. The module also supports the hardware flow control option, with UxCTS and UxRTS pins, and also includes an IrDA encoder and decoder.

The primary features of the UART module are:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, odd or no parity options (for 8-bit data)
- One or two Stop bits
- Hardware auto-baud feature
- Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 76 bps to 20 Mbps at 80 MHz
- 4-level-deep First-In-First-Out (FIFO) Transmit Data Buffer
- 4-level-deep FIFO Receive Data Buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt only on address detect (9th bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support

Figure 19-1 illustrates a simplified block diagram of the UART.

FIGURE 19-1: UART SIMPLIFIED BLOCK DIAGRAM



PIC32MX3XX/4XX

NOTES:

TABLE 27-1: MIPS32® INSTRUCTION SET (CONTINUED)

Instruction	Description	Function
JAL	Jump and Link	$GPR[31] = PC + 8$ $PC = PC[31:28] \parallel offset \ll 2$
JALR	Jump and Link Register	$Rd = PC + 8$ $PC = Rs$
JALR.HB	Jump and Link Register with Hazard Barrier	Like JALR, but also clears execution and instruction hazards
JR	Jump Register	$PC = Rs$
JR.HB	Jump Register with Hazard Barrier	Like JR, but also clears execution and instruction hazards
LB	Load Byte	$Rt = (\text{byte})Mem[Rs+offset]$
LBU	Unsigned Load Byte	$Rt = (\text{ubyte})Mem[Rs+offset]$
LH	Load Halfword	$Rt = (\text{half})Mem[Rs+offset]$
LHU	Unsigned Load Halfword	$Rt = (\text{uhalf})Mem[Rs+offset]$
LL	Load Linked Word	$Rt = Mem[Rs+offset]$ $LL_{bit} = 1$ $LLAdr = Rs + offset$
LUI	Load Upper Immediate	$Rt = \text{immediate} \ll 16$
LW	Load Word	$Rt = Mem[Rs+offset]$
LWPC	Load Word, PC relative	$Rt = Mem[PC+offset]$
LWL	Load Word Left	$Re = Re \text{ MERGE } Mem[Rs+offset]$
LWR	Load Word Right	$Re = Re \text{ MERGE } Mem[Rs+offset]$
MADD	Multiply-Add	$HI \mid LO += (\text{int})Rs * (\text{int})Rt$
MADDU	Multiply-Add Unsigned	$HI \mid LO += (\text{uns})Rs * (\text{uns})Rt$
MFC0	Move from Coprocessor 0	$Rt = CPR[0, Rd, sel]$
MFHI	Move from HI	$Rd = HI$
MFLO	Move from LO	$Rd = LO$
MOVN	Move Conditional on Not Zero	if $Rt \neq 0$ then $Rd = Rs$
MOVZ	Move Conditional on Zero	if $Rt = 0$ then $Rd = Rs$
MSUB	Multiply-Subtract	$HI \mid LO -= (\text{int})Rs * (\text{int})Rt$
MSUBU	Multiply-Subtract Unsigned	$HI \mid LO -= (\text{uns})Rs * (\text{uns})Rt$
MTC0	Move to Coprocessor 0	$CPR[0, n, Sel] = Rt$
MTHI	Move to HI	$HI = Rs$
MTLO	Move to LO	$LO = Rs$
MUL	Multiply with register write	$HI \mid LO = \text{Unpredictable}$ $Rd = ((\text{int})Rs * (\text{int})Rt)_{31..0}$
MULT	Integer Multiply	$HI \mid LO = (\text{int})Rs * (\text{int})Rd$
MULTU	Unsigned Multiply	$HI \mid LO = (\text{uns})Rs * (\text{uns})Rd$
NOP	No Operation (Assembler idiom for: SLL r0, r0, r0)	
NOR	Logical NOR	$Rd = \sim(Rs \mid Rt)$
OR	Logical OR	$Rd = Rs \mid Rt$
ORI	Logical OR Immediate	$Rt = Rs \mid \text{Immed}$
RDHWR	Read Hardware Register (if enabled by HWRE _{na} Register)	$Re = HWR[Rd]$

Note 1: This instruction is deprecated and should not be used.

28.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

28.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

28.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

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TABLE 29-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
DO10 DO16	VOL	Output Low Voltage I/O Ports	—	—	0.4	V	IO _L = 7 mA, V _{DD} = 3.6V
			—	—	0.4	V	IO _L = 6 mA, V _{DD} = 2.3V
		OSC2/CLKO	—	—	0.4	V	IO _L = 3.5 mA, V _{DD} = 3.6V
			—	—	0.4	V	IO _L = 2.5 mA, V _{DD} = 2.3V
DO20 DO26	VOH	Output High Voltage I/O Ports	2.4	—	—	V	IO _H = -12 mA, V _{DD} = 3.6V
			1.4	—	—	V	IO _H = -12 mA, V _{DD} = 2.3V
		OSC2/CLKO	2.4	—	—	V	IO _H = -12 mA, V _{DD} = 3.6V
			1.4	—	—	V	IO _H = -12 mA, V _{DD} = 2.3V

TABLE 29-10: ELECTRICAL CHARACTERISTICS: BROWN-OUT RESET (BOR)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
BO10	VBOR	BOR Event on V _{DD} transition high-to-low	2.0	—	2.3	V	—

FIGURE 29-6: TIMER1, 2, 3, 4, 5 EXTERNAL CLOCK TIMING CHARACTERISTICS

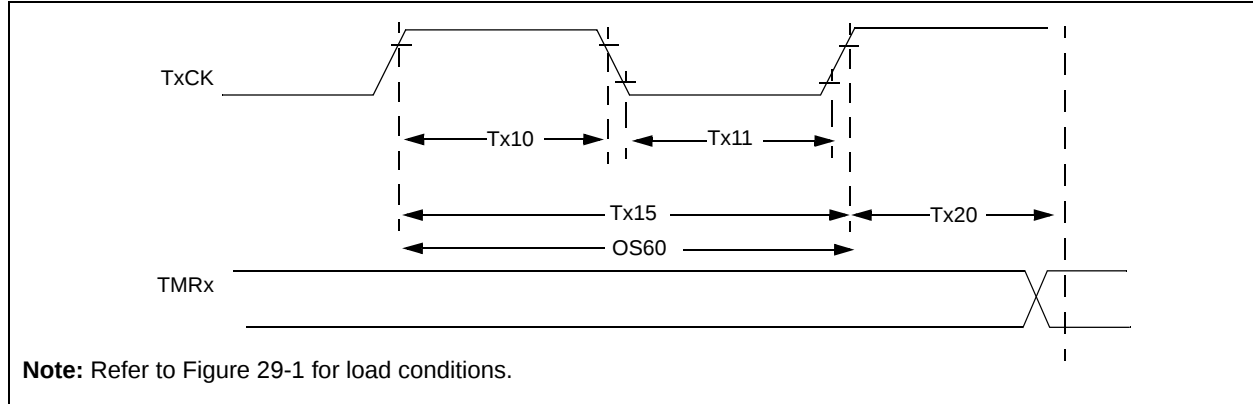


TABLE 29-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS⁽¹⁾

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	Symbol	Characteristics ⁽²⁾		Min.	Typical	Max.	Units	Conditions
TA10	TtxH	TxCK High Time	Synchronous, with prescaler	[(12.5 ns or 1TPB)/N] + 25 ns	—	—	ns	Must also meet parameter TA15.
			Asynchronous, with prescaler	10	—	—	ns	—
TA11	TtxL	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1TPB)/N] + 25 ns	—	—	ns	Must also meet parameter TA15.
			Asynchronous, with prescaler	10	—	—	ns	—
TA15	TtxP	TxCK Input Period	Synchronous, with prescaler	[(Greater of 25 ns or 2TPB)/N] + 30 ns	—	—	ns	VDD > 2.7V
				[(Greater of 25 ns or 2TPB)/N] + 50 ns	—	—	ns	VDD < 2.7V
			Asynchronous, with prescaler	20	—	—	ns	VDD > 2.7V (Note 3)
				50	—	—	ns	VDD < 2.7V (Note 3)
OS60	Ft1	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting TCS bit (T1CON<1>))		32	—	100	kHz	—
TA20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—		1	TPB	—

Note 1: Timer1 is a Type A.

2: This parameter is characterized, but not tested in manufacturing.

3: N = prescale value (1, 8, 64, 256)

TABLE 29-35: 10-BIT ADC CONVERSION RATE PARAMETERS⁽²⁾

Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-Temp					
ADC Speed	TAD Minimum	Sampling Time Min	Rs Max	VDD	ADC Channels Configuration
1 MIPS to 400 ksp ⁽¹⁾	65 ns	132 ns	500Ω	3.0V to 3.6V	
Up to 400 ksp	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	
Up to 300 ksp	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	

Note 1: External VREF- and VREF+ pins must be used for correct operation.

2: These parameters are characterized, but not tested in manufacturing.

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TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 29.0 “Electrical Characteristics”	Updated the Absolute Maximum Ratings and added Note 3. Added Thermal Packaging Characteristics for the 121-pin XBGA package (see Table 29-3). Updated the conditions for parameters DC20, DC21, DC22 and DC23 in Table 29-5. Updated the comments for parameter D321 (CEFC) in Table 29-15. Updated the SPIx Module Slave Mode (CKE = 1) Timing Characteristics, changing SP52 to SP35 between the MSb and Bit 14 on SDOx (see Figure 29-13).
Section 30.0 “Packaging Information”	Added the 121-pin XBGA package marking information and package details.
“Product Identification System”	Added the definition for BG (121-lead 10x10x1.1 mm, XBGA). Added the definition for Speed.

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TABLE A-3: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 29.0 “Electrical Characteristics”	Added the new V-Temp temperature range (-40°C to +105°C) to the heading of all specification tables. Updated the Ambient temperature under bias, updated the Voltage on any 5V tolerant pin with respect to V_{SS} when V_{DD} < 2.3V, and added Voltage on V_{BUS} with respect to V_{SS} in Absolute Maximum Ratings. Added the characteristic, DC5a to Operating MIPS vs. Voltage (see Table 29-1). Updated or added the following parameters to the Operating Current (I_{DD}) DC Characteristics: DC20, DC23, DC24c, DC25d, DC26c (see Table 29-5). Added the following parameters to the Idle Current (I_{IDLE}) DC Characteristics: DC30c, DC31c, DC32c, DS33c, DC34c, DC35c, and DC36c (see Table 29-6). Added the following parameters to the Power-down Current (I_{PD}) DC Characteristics: DC40g, DC40h, DC40i, DC41g, DC41h, DC42g, DC42h, DC42i, DC43h, and DC43i (see Table 29-7). Added the Brown-out Reset (BOR) Electrical Characteristics (see Table 29-10). Removed all Conditions from the Program Memory DC Characteristics (see Table 29-11). Removed the AC Characteristics voltage reference table (Table 29-15). Added Note 2 to the PLL Clock Timing Specifications (see Table 29-18). Updated the OC/PWM Module Timing Characteristics (see Figure 29-9). Added parameter IM51 and Note 3 to the I2Cx Bus Data Timing Requirements (Master Mode) (see Table 29-32). Added parameter numbers (AD13, AD14, and AD15) to the ADC Module Specifications (see Table 29-34). Updated the 10-bit ADC Conversion Rate Parameters (see Table 29-35). Updated parameter AD57 (T_{SAMP}) in the Analog-to-Digital Conversion Timing Requirements (see Table 29-36). Updated the Conditions for parameters USB313, USB318, and USB319 in the OTG Electrical Specifications (see Table 29-40).
Section 30.0 “Packaging Information”	Updated the 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] packing diagram.
Product Identification System	Added the new V-Temp (V) temperature information.