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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx340f256ht-80i-pt

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number ⁽¹⁾			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
RD0	46	72	D9	I/O	ST	PORTD is a bidirectional I/O port.
RD1	49	76	A11	I/O	ST	
RD2	50	77	A10	I/O	ST	
RD3	51	78	B9	I/O	ST	
RD4	52	81	C8	I/O	ST	
RD5	53	82	B8	I/O	ST	
RD6	54	83	D7	I/O	ST	
RD7	55	84	C7	I/O	ST	
RD8	42	68	E9	I/O	ST	
RD9	43	69	E10	I/O	ST	
RD10	44	70	D11	I/O	ST	
RD11	45	71	C11	I/O	ST	
RD12	—	79	A9	I/O	ST	
RD13	—	80	D8	I/O	ST	
RD14	—	47	L9	I/O	ST	
RD15	—	48	K9	I/O	ST	
RE0	60	93	A4	I/O	ST	PORTE is a bidirectional I/O port.
RE1	61	94	B4	I/O	ST	
RE2	62	98	B3	I/O	ST	
RE3	63	99	A2	I/O	ST	
RE4	64	100	A1	I/O	ST	
RE5	1	3	D3	I/O	ST	
RE6	2	4	C1	I/O	ST	
RE7	3	5	D2	I/O	ST	
RE8	—	18	G1	I/O	ST	
RE9	—	19	G2	I/O	ST	
RF0	58	87	B6	I/O	ST	PORTF is a bidirectional I/O port.
RF1	59	88	A6	I/O	ST	
RF2	34	52	K11	I/O	ST	
RF3	33	51	K10	I/O	ST	
RF4	31	49	L10	I/O	ST	
RF5	32	50	L11	I/O	ST	
RF6	35	55	H9	I/O	ST	
RF7	—	54	H8	I/O	ST	
RF8	—	53	J10	I/O	ST	
RF12	—	40	K6	I/O	ST	
RF13	—	39	L6	I/O	ST	

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer

Analog = Analog input P = Power
O = Output I = Input

Note 1: Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

FIGURE 4-6: MEMORY MAP ON RESET FOR PIC32MX340F512H, PIC32MX360F512L, PIC32MX440F512H AND PIC32MX460F512L DEVICES⁽¹⁾

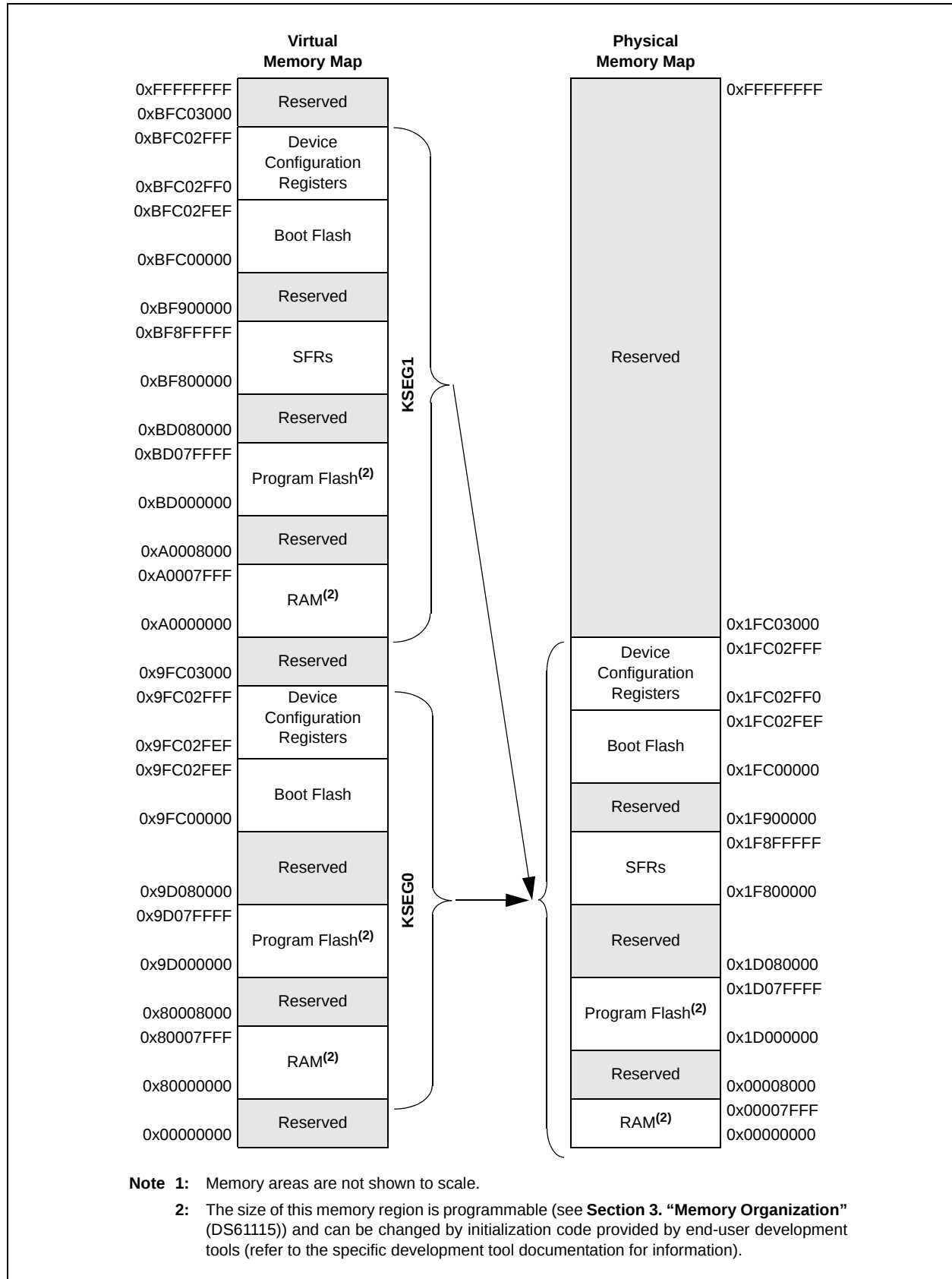


TABLE 4-3: INTERRUPT REGISTERS MAP FOR PIC32MX340F128H, PIC32MX340F256H, PIC32MX340F512H, PIC32MX340F128L, PIC32MX360F256L AND PIC32MX360F512L DEVICES ONLY⁽¹⁾

Virtual Address (BF88..#)	Register Name	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000	
		15:0	—	—	—	MVEC	—	TPC<2:0>				—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	SRIPL<2:0>				—	—	VEC<5:0>					0000	
1020	IPTMR	31:16	IPTMR<31:0>																0000	
		15:0																	0000	
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	SPI1RXIF	SPI1TXIF	SPI1EIF	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000	
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000	
1040	IFS1	31:16	—	—	—	—	—	—	—	FCEIF	—	—	—	—	DMA3IF	DMA2IF	DMA1IF	DMA0IF	0000	
		15:0	RTCCIF	FSCMIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF	SPI2RXIF	SPI2TXIF	SPI2EIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000	
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	SPI1RXIE	SPI1TXIE	SPI1EIE	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000	
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000	
1070	IEC1	31:16	—	—	—	—	—	—	—	FCEIE	—	—	—	—	DMA3IE	DMA2IE	DMA1IE	DMA0IE	0000	
		15:0	RTCCIE	FSCMIE	I2C2MIE	—	—	—	—	—	SPI2RXIE	SPI2TXIE	SPI2EIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000	
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>			—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>			—	—	—	CTIP<2:0>			CTIS<1:0>		0000
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>			—	—	—	OC1IP<2:0>			OC1IS<1:0>		0000
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>			—	—	—	T1IP<2:0>			T1IS<1:0>		0000
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>			—	—	—	OC2IP<2:0>			OC2IS<1:0>		0000
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>			—	—	—	T2IP<2:0>			T2IS<1:0>		0000
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>			—	—	—	OC3IP<2:0>			OC3IS<1:0>		0000
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>			—	—	—	T3IP<2:0>			T3IS<1:0>		0000
10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>			—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>			—	—	—	T4IP<2:0>			T4IS<1:0>		0000
10E0	IPC5	31:16	—	—	—	SPI1IP<2:0>			SPI1IS<1:0>			—	—	—	OC5IP<2:0>			OC5IS<1:0>		0000
		15:0	—	—	—	IC5IP<2:0>			IC5IS<1:0>			—	—	—	T5IP<2:0>			T5IS<1:0>		0000
10F0	IPC6	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>			—	—	—	CNIP<2:0>			CNIS<1:0>		0000
		15:0	—	—	—	I2C1IP<2:0>			I2C1IS<1:0>			—	—	—	U1IP<2:0>			U1IS<1:0>		0000
1100	IPC7	31:16	—	—	—	SPI2IP<2:0>			SPI2IS<1:0>			—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		0000
		15:0	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>			—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000
1110	IPC8	31:16	—	—	—	RTCCIP<2:0>			RTCCIS<1:0>			—	—	—	FSCMIP<2:0>			FSCMIS<1:0>		0000
		15:0	—	—	—	I2C2IP<2:0>			I2C2IS<1:0>			—	—	—	U2IP<2:0>			U2IS<1:0>		0000
1120	IPC9	31:16	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>			—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000
		15:0	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>			—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000
1140	IPC11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	FCEIP<2:0>			FCEIS<1:0>		0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
- 2:** This register does not have associated CLR, SET, and INV registers.

TABLE 4-7: TIMER1-5 REGISTERS MAP⁽¹⁾

Virtual Address (BF80-#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	T1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	TWDIS	TWIP	—	—	—	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—	0000
0610	TMR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR1<15:0>																0000
0620	PR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR1<15:0>																FFFF
0800	T2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>		—	T32	—	TCS ⁽²⁾	—	0000
0810	TMR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR2<15:0>																0000
0820	PR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR2<15:0>																FFFF
0A00	T3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>		—	—	—	TCS ⁽²⁾	—	0000
0A10	TMR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR3<15:0>																0000
0A20	PR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR3<15:0>																FFFF
0C00	T4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>		—	T32	—	TCS ⁽²⁾	—	0000
0C10	TMR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR4<15:0>																0000
0C20	PR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR4<15:0>																FFFF
0E00	T5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>		—	—	—	TCS ⁽²⁾	—	0000
0E10	TMR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR5<15:0>																0000
0E20	PR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR5<15:0>																FFFF

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
- 2:** This bit is not available on 64-pin devices.

TABLE 4-12: SPI1-2 REGISTERS MAP^(1,2)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5800	SPI1CON	31:16	FRMEN	FRMSYNC	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	SPIFE	—	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	—	—	—	—	0000
5810	SPI1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	SPIBUSY	—	—	—	—	SPIROV	—	—	SPITBE	—	—	SPIRBF	0008
5820	SPI1BUF	31:16	DATA<31:0>																0000
		15:0	DATA<31:0>																0000
5830	SPI1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>								0000	
5A00	SPI2CON	31:16	FRMEN	FRMSYNC	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	SPIFE	—	0008
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	—	—	—	—	—	0000
5A10	SPI2STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	SPIBUSY	—	—	—	—	SPIROV	—	—	SPITBE	—	—	SPIRBF	0008
5A20	SPI2BUF	31:16	DATA<31:0>																0000
		15:0	DATA<31:0>																0000
5A30	SPI2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>								0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** All registers in this table except SPIxBUF have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.
- Note 2:** SPI2 Module is not present on PIC32MX420FXXXX/440FXXXX devices.

TABLE 4-27: PORTE REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L, PIC32MX360F512L, PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY⁽¹⁾

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6100	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISE9	TRISE8	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	03FF
6110	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RE9	RE8	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
6120	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATE9	LATE8	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
6130	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCE9	ODCE8	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

TABLE 4-28: PORTE REGISTERS MAP FOR PIC32MX320F032H, PIC32MX320F064H, PIC32MX320F128H, PIC32MX340F128H, PIC32MX340F256H, PIC32MX340F512H, PIC32MX420F032H, PIC32MX440F128H, PIC32MX440F256H AND PIC32MX440F512H DEVICES ONLY⁽¹⁾

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6100	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	00FF
6110	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
6120	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
6130	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

PIC32MX3XX/4XX

TABLE 7-1: INTERRUPT IRQ AND VECTOR LOCATION

Interrupt Source ⁽¹⁾	IRQ	Vector Number	Interrupt Bit Location			
Highest Natural Order Priority			Flag	Enable	Priority	Subpriority
CT – Core Timer Interrupt	0	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>
CS0 – Core Software Interrupt 0	1	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>
CS1 – Core Software Interrupt 1	2	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>
INT0 – External Interrupt 0	3	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>
T1 – Timer1	4	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>
IC1 – Input Capture 1	5	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>
OC1 – Output Compare 1	6	6	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>
INT1 – External Interrupt 1	7	7	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>
T2 – Timer2	8	8	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>
IC2 – Input Capture 2	9	9	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>
OC2 – Output Compare 2	10	10	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>
INT2 – External Interrupt 2	11	11	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>
T3 – Timer3	12	12	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>
IC3 – Input Capture 3	13	13	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>
OC3 – Output Compare 3	14	14	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>
INT3 – External Interrupt 3	15	15	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>
T4 – Timer4	16	16	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>
IC4 – Input Capture 4	17	17	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>
OC4 – Output Compare 4	18	18	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>
INT4 – External Interrupt 4	19	19	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>
T5 – Timer5	20	20	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>
IC5 – Input Capture 5	21	21	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>
OC5 – Output Compare 5	22	22	IFS0<22>	IEC0<22>	IPC5<20:18>	IPC5<17:16>
SPI1E – SPI1 Fault	23	23	IFS0<23>	IEC0<23>	IPC5<28:26>	IPC5<25:24>
SPI1TX – SPI1 Transfer Done	24	23	IFS0<24>	IEC0<24>	IPC5<28:26>	IPC5<25:24>
SPI1RX – SPI1 Receive Done	25	23	IFS0<25>	IEC0<25>	IPC5<28:26>	IPC5<25:24>
U1E – UART1 Error	26	24	IFS0<26>	IEC0<26>	IPC6<4:2>	IPC6<1:0>
U1RX – UART1 Receiver	27	24	IFS0<27>	IEC0<27>	IPC6<4:2>	IPC6<1:0>
U1TX – UART1 Transmitter	28	24	IFS0<28>	IEC0<28>	IPC6<4:2>	IPC6<1:0>
I2C1B – I2C1 Bus Collision Event	29	25	IFS0<29>	IEC0<29>	IPC6<12:10>	IPC6<9:8>
I2C1S – I2C1 Slave Event	30	25	IFS0<30>	IEC0<30>	IPC6<12:10>	IPC6<9:8>
I2C1M – I2C1 Master Event	31	25	IFS0<31>	IEC0<31>	IPC6<12:10>	IPC6<9:8>
CN – Input Change Interrupt	32	26	IFS1<0>	IEC1<0>	IPC6<20:18>	IPC6<17:16>
AD1 – ADC1 Convert Done	33	27	IFS1<1>	IEC1<1>	IPC6<28:26>	IPC6<25:24>
PMP – Parallel Master Port	34	28	IFS1<2>	IEC1<2>	IPC7<4:2>	IPC7<1:0>
CMP1 – Comparator Interrupt	35	29	IFS1<3>	IEC1<3>	IPC7<12:10>	IPC7<9:8>
CMP2 – Comparator Interrupt	36	30	IFS1<4>	IEC1<4>	IPC7<20:18>	IPC7<17:16>

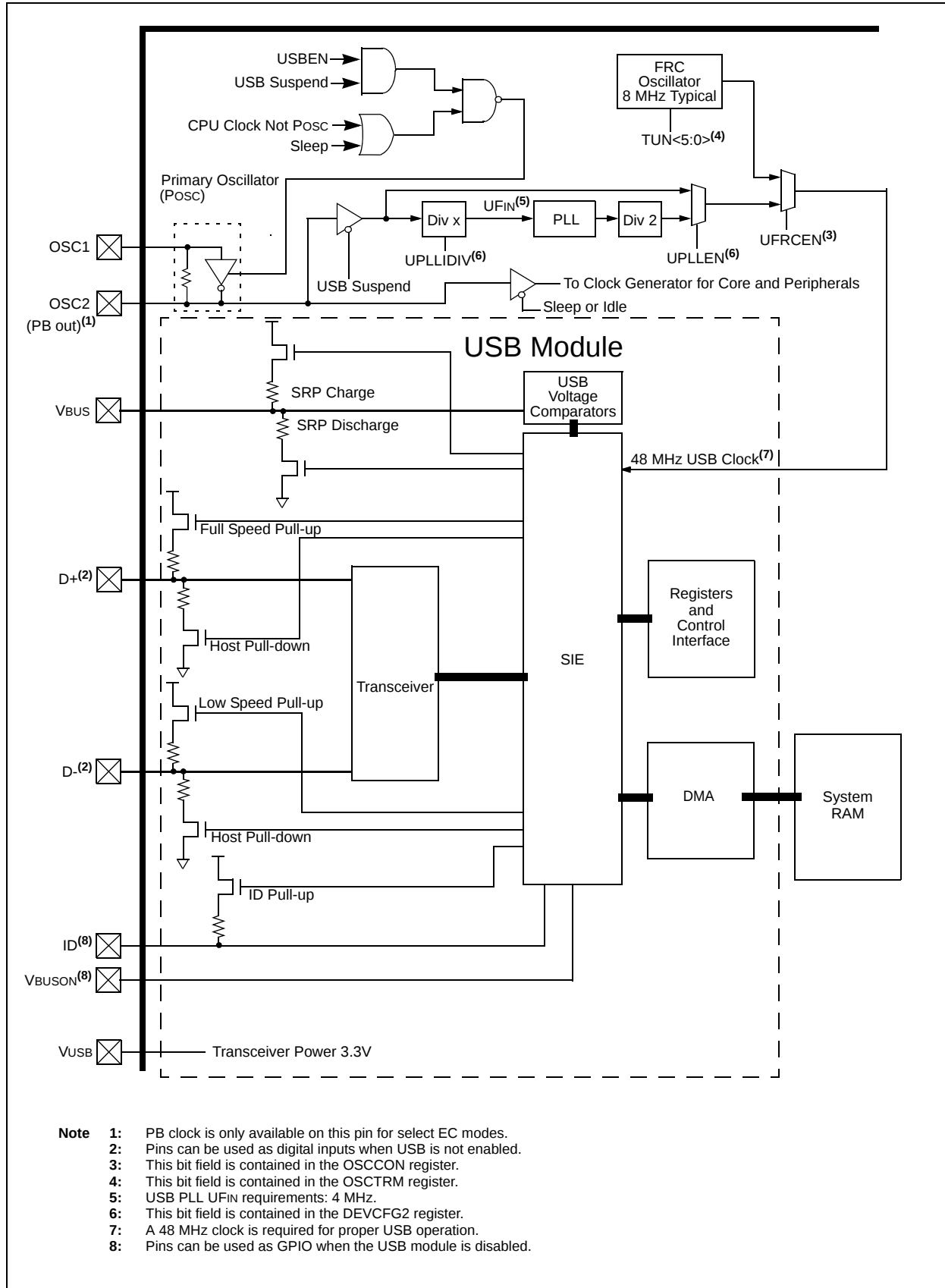
Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MX General Purpose – Features”** and **TABLE 2: “PIC32MX USB – Features”** for available peripherals.

PIC32MX3XX/4XX

NOTES:

PIC32MX3XX/4XX

FIGURE 11-1: PIC32MX3XX/4XX FAMILY USB INTERFACE DIAGRAM



15.0 INPUT CAPTURE

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. “Input Capture”** (DS61122) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement. The PIC32MX3XX/4XX devices support up to five input capture channels.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The events that cause a capture event are listed below in three categories:

1. Simple Capture Event modes
 - Capture timer value on every falling edge of input at ICx pin
 - Capture timer value on every rising edge of input at ICx pin

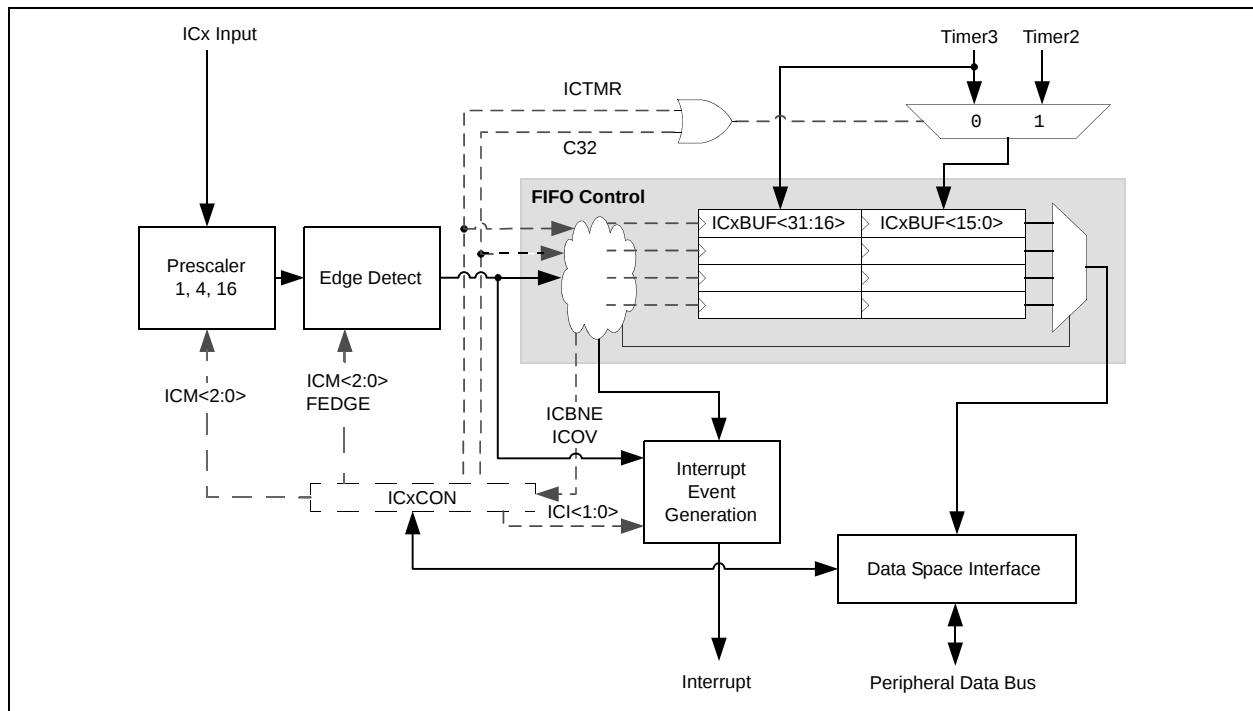
2. Capture timer value on every edge (rising and falling)
3. Capture timer value on every edge (rising and falling), specified edge first.
4. Prescaler Capture Event modes
 - Capture timer value on every 4th rising edge of input at ICx pin
 - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during CPU Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values
 - Interrupt optionally generated after 1, 2, 3 or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

FIGURE 15-1: INPUT CAPTURE BLOCK DIAGRAM



18.0 INTER-INTEGRATED CIRCUIT™ (I²C™)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. “Inter-Integrated Circuit (I²C™)”** (DS61116) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The I²C module provides complete hardware support for both Slave and Multi-Master modes of the I²C serial communication standard. Figure 18-1 illustrates the I²C module block diagram.

The PIC32MX3XX/4XX devices have up to two I²C interface modules, denoted as I2C1 and I2C2. Each I²C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I²C module, ‘I2Cx’ (x = 1 or 2), offers the following key features:

- I²C Interface Supporting both Master and Slave Operation.
- I²C Slave Mode Supports 7 and 10-bit Address.
- I²C Master Mode Supports 7 and 10-bit Address.
- I²C Port allows Bidirectional Transfers between Master and Slaves.
- Serial Clock Synchronization for I²C Port can be used as a Handshake Mechanism to Suspend and Resume Serial Transfer (SCLREL control).
- I²C Supports Multi-master Operation; Detects Bus Collision and Arbitrates Accordingly.
- Provides Support for Address Bit Masking.

PIC32MX3XX/4XX

26.3 On-Chip Voltage Regulator

All PIC32MX3XX/4XX device's core and digital logic are designed to operate at a nominal 1.8V. To simplify system designs, most devices in the PIC32MX3XX/4XX incorporate an on-chip regulator providing the required core logic voltage from VDD.

The internal 1.8V regulator is controlled by the ENVREG pin. Tying this pin to VDD enables the regulator, which in turn provides power to the core. A low ESR capacitor (such as tantalum) must be connected to the VCORE/VCAP pin (Figure 26-2). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in **Section 29.1 "DC Characteristics"**.

Note: It is important that the low ESR capacitor is placed as close as possible to the VCORE/VCAP pin.

Tying the ENVREG pin to VSS disables the regulator. In this case, separate power for the core logic at a nominal 1.8V must be supplied to the device on the VCORE/VCAP pin.

Alternatively, the VCORE/VCAP and VDD pins can be tied together to operate at a lower nominal voltage. Refer to Figure 26-2 for possible configurations.

26.3.1 ON-CHIP REGULATOR AND POR

When the voltage regulator is enabled, it takes fixed delay for it to generate output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

If the regulator is disabled, a separate Power-up Timer (PWRT) is automatically enabled. The PWRT adds a fixed delay of TPWRT at device start-up. See **Section 29.0 "Electrical Characteristics"** for more information on TPU AND TPWRT.

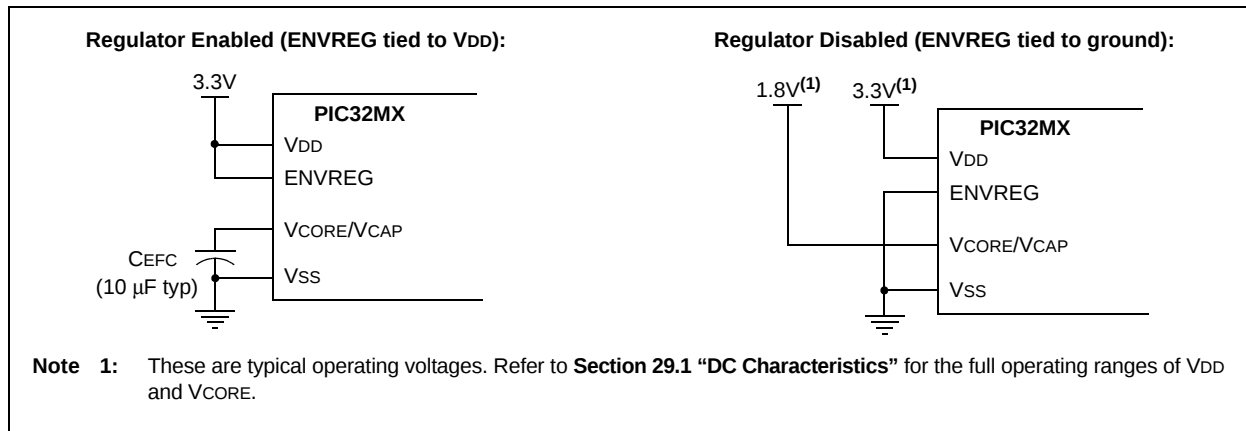
26.3.2 ON-CHIP REGULATOR AND BOR

When the on-chip regulator is enabled, PIC32MX3XX/4XX devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **Section 29.1 "DC Characteristics"**.

26.3.3 POWER-UP REQUIREMENTS

The on-chip regulator is designed to meet the power-up requirements for the device. If the application does not use the regulator, then strict power-up conditions must be adhered to. While powering up, VCORE must never exceed VDD by 0.3 volts.

FIGURE 26-2: CONNECTIONS FOR THE ON-CHIP REGULATOR



PIC32MX3XX/4XX

TABLE 29-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD}) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp			
Parameter No.	Typical ⁽²⁾	Max.	Units	Conditions		
Module Differential Current (Continued)						
DC43	—	1100	μA	-40°C	2.5V	ADC: ΔIADC (Notes 3, 4, 6)
DC43a	—	1100	μA	+25°C		
DC43b	—	1000	μA	+85°C		
DC43h	—	1200	μA	+105°C		
DC43c	880	—	μA	—	—	ADC: ΔIADC (Notes 3, 4)
DC43e	—	1100	μA	-40°C	3.6V	ADC: ΔIADC (Notes 3, 4)
DC43f	—	1100	μA	+25°C		
DC43g	—	1000	μA	+85°C		
DC43i	—	1200	μA	+105°C		

- Note 1:** Base I_{PD} is measured with all digital peripheral modules disabled. All I/Os are configured as inputs and pulled low. WDT and FSCM are disabled.
- 2:** Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.
- 4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.
- 5:** Data is characterized at +70°C and not tested. Parameter is for design guidance only.
- 6:** This parameter is characterized, but not tested in manufacturing.

29.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX3XX/4XX AC characteristics and timing parameters.

FIGURE 29-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

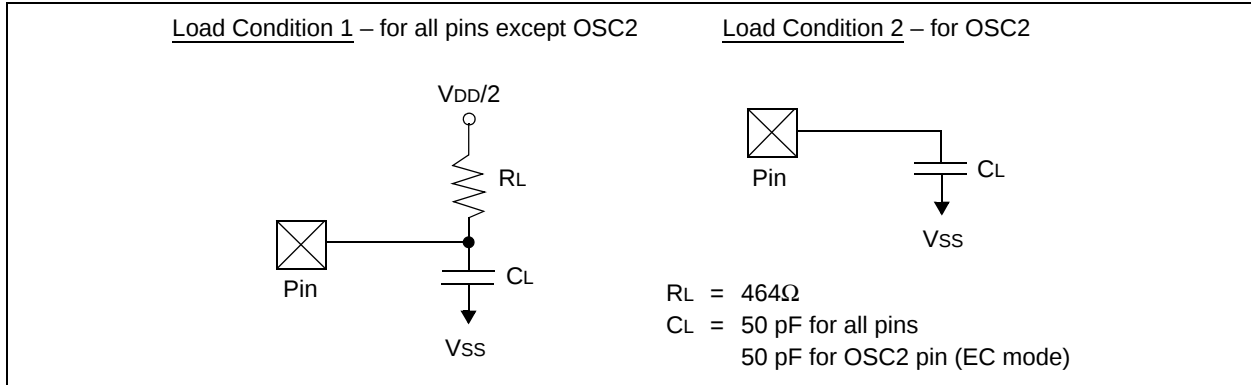
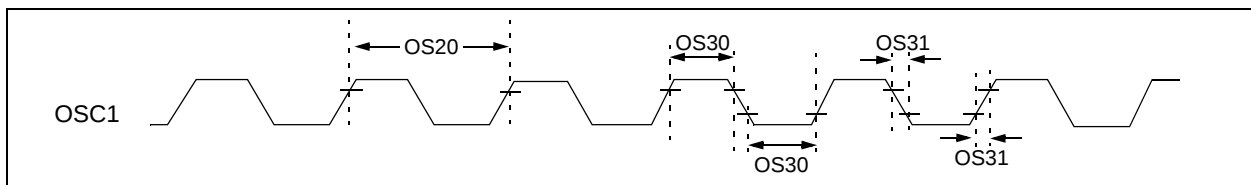


TABLE 29-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for Industrial $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$ for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
DO56	C _{IO}	All I/O pins and OSC2	—	—	50	pF	EC mode
DO58	C _B	SCLx, SDAx	—	—	400	pF	In I ² C™ mode

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 29-2: EXTERNAL CLOCK TIMING



PIC32MX3XX/4XX

TABLE 29-17: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
OS10	Fosc	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4	— —	50 ⁽³⁾ 50 ⁽⁵⁾	MHz MHz	EC (Note 5) ECPLL (Note 4)
OS11		Oscillator Crystal Frequency	3	—	10	MHz	XT (Note 5)
OS12			4	—	10	MHz	XTPLL (Notes 4, 5)
OS13			10	—	25	MHz	HS (Note 5)
OS14			10	—	25	MHz	HSPLL (Notes 4, 5)
OS15			32	32.768	100	kHz	Sosc (Note 5)
OS20	Tosc	Tosc = 1/Fosc = Tcy ⁽²⁾	—	—	—	—	See parameter OS10 for Fosc value
OS30	TosL, TosH	External Clock In (OSC1) High or Low Time	0.45 x Tosc	—	—	ns	EC (Note 5)
OS31	TosR, TosF	External Clock In (OSC1) Rise or Fall Time	—	—	0.05 x Tosc	ns	EC (Note 5)
OS40	TOST	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, XT, XTPLL and Sosc Clock Oscillator modes)	—	1024	—	Tosc	(Note 5)
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	(Note 5)
OS42	GM	External Oscillator Transconductance	—	12	—	mA/V	VDD = 3.3V TA = +25°C (Note 5)

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are characterized but are not tested.

- 2:** Instruction cycle period (Tcy) equals the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin.
- 3:** 40 MHz maximum for PIC32MX320F032H and PIC32MX420F032H devices.
- 4:** PLL input requirements: 4 MHz ≤ F_{PLLIN} ≤ 5 MHz (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.
- 5:** This parameter is characterized, but not tested in manufacturing.

FIGURE 29-20: PARALLEL SLAVE PORT TIMING

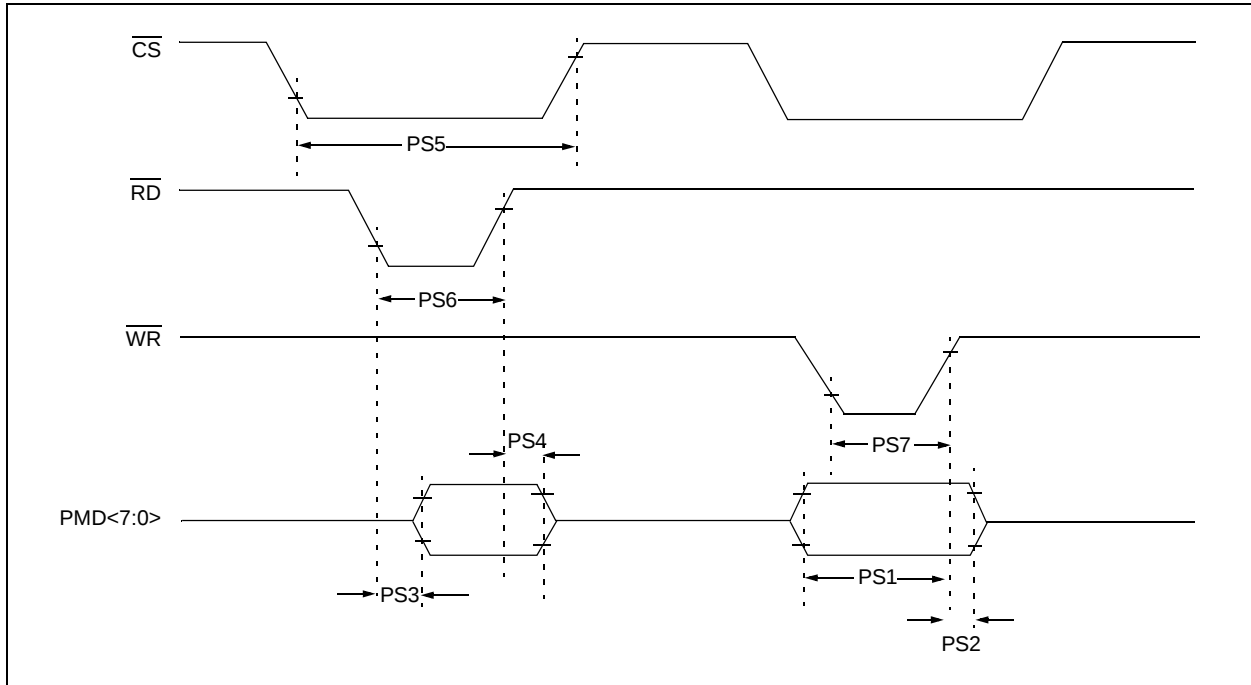


TABLE 29-37: PARALLEL SLAVE PORT REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-Temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical	Max.	Units	Conditions
PS1	TdtV2wrH	Data In Valid before $\overline{WR}$ or $\overline{CS}$ Inactive (setup time)	20	—	—	ns	—
PS2	TwrH2dtl	$\overline{WR}$ or $\overline{CS}$ Inactive to Data – In Invalid (hold time)	40	—	—	ns	—
PS3	TrdL2dtV	$\overline{RD}$ and $\overline{CS}$ Active to Data – Out Valid	—	—	60	ns	—
PS4	TrdH2dtl	$\overline{RD}$ Active or $\overline{CS}$ Inactive to Data – Out Invalid	0	—	10	ns	—
PS5	Tcs	$\overline{CS}$ Active Time	$T_{PB} + 40$	—	—	ns	—
PS6	TWR	$\overline{WR}$ Active Time	$T_{PB} + 25$	—	—	ns	—
PS7	TRD	$\overline{RD}$ Active Time	$T_{PB} + 25$	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

PIC32MX3XX/4XX

NOTES:

PIC32MX3XX/4XX

TABLE A-3: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 29.0 “Electrical Characteristics”	Added the new V-Temp temperature range (-40°C to +105°C) to the heading of all specification tables. Updated the Ambient temperature under bias, updated the Voltage on any 5V tolerant pin with respect to V_{SS} when V_{DD} < 2.3V, and added Voltage on V_{BUS} with respect to V_{SS} in Absolute Maximum Ratings. Added the characteristic, DC5a to Operating MIPS vs. Voltage (see Table 29-1). Updated or added the following parameters to the Operating Current (I_{DD}) DC Characteristics: DC20, DC23, DC24c, DC25d, DC26c (see Table 29-5). Added the following parameters to the Idle Current (I_{IDLE}) DC Characteristics: DC30c, DC31c, DC32c, DS33c, DC34c, DC35c, and DC36c (see Table 29-6). Added the following parameters to the Power-down Current (I_{PD}) DC Characteristics: DC40g, DC40h, DC40i, DC41g, DC41h, DC42g, DC42h, DC42i, DC43h, and DC43i (see Table 29-7). Added the Brown-out Reset (BOR) Electrical Characteristics (see Table 29-10). Removed all Conditions from the Program Memory DC Characteristics (see Table 29-11). Removed the AC Characteristics voltage reference table (Table 29-15). Added Note 2 to the PLL Clock Timing Specifications (see Table 29-18). Updated the OC/PWM Module Timing Characteristics (see Figure 29-9). Added parameter IM51 and Note 3 to the I2Cx Bus Data Timing Requirements (Master Mode) (see Table 29-32). Added parameter numbers (AD13, AD14, and AD15) to the ADC Module Specifications (see Table 29-34). Updated the 10-bit ADC Conversion Rate Parameters (see Table 29-35). Updated parameter AD57 (T_{SAMP}) in the Analog-to-Digital Conversion Timing Requirements (see Table 29-36). Updated the Conditions for parameters USB313, USB318, and USB319 in the OTG Electrical Specifications (see Table 29-40).
Section 30.0 “Packaging Information”	Updated the 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] packing diagram.
Product Identification System	Added the new V-Temp (V) temperature information.

PIC32MX3XX/4XX

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