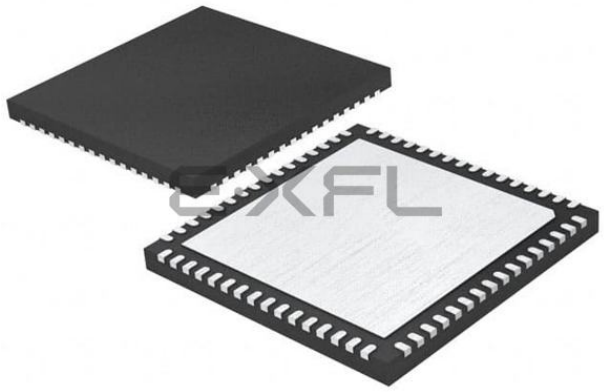
Microchip Technology - PIC32MX340F512HT-80V/MR Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx340f512ht-80v-mr

TABLE 2: PIC32MX USB – FEATURES

USB															
Device	Pins	Packages(2)	MHz	Program Memory (KB)	Data Memory (KB)	Timers/Capture/Compare	Programmable DMA Channels	Dedicated USB DMA Channels	VREG	Trace	EUART/SPI/I²C™	10-bit ADC (ch)	Comparators	PMP/PSP	JTAG
PIC32MX420F032H	64	PT, MR	40	32 + 12(1)	8	5/5/5	0	2	Yes	No	2/1/2	16	2	Yes	Yes
PIC32MX440F128H	64	PT, MR	80	128 + 12(1)	32	5/5/5	4	2	Yes	No	2/1/2	16	2	Yes	Yes
PIC32MX440F256H	64	PT, MR	80	256 + 12(1)	32	5/5/5	4	2	Yes	No	2/1/2	16	2	Yes	Yes
PIC32MX440F512H	64	PT, MR	80	512 + 12(1)	32	5/5/5	4	2	Yes	No	2/1/2	16	2	Yes	Yes
PIC32MX440F128L	100	PT	80	128 + 12(1)	32	5/5/5	4	2	Yes	No	2/2/2	16	2	Yes	Yes
	121	BG													
PIC32MX460F256L	100	PT	80	256 + 12(1)	32	5/5/5	4	2	Yes	Yes	2/2/2	16	2	Yes	Yes
	121	BG													
PIC32MX460F512L	100	PT	80	512 + 12(1)	32	5/5/5	4	2	Yes	Yes	2/2/2	16	2	Yes	Yes
	121	BG													

Legend: PT = TQFP MR = QFN BG = XBGA

Note 1: This device features 12 KB Boot Flash memory.

2: See Legend for an explanation of the acronyms. See **Section 30.0 “Packaging Information”** for details.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number(1)			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
INT3	44	66	E11	I	ST	External interrupt 3.
INT4	45	67	E8	I	ST	External interrupt 4.
RA0	—	17	G3	I/O	ST	PORTA is a bidirectional I/O port.
RA1	—	38	J6	I/O	ST	
RA2	—	58	H11	I/O	ST	
RA3	—	59	G10	I/O	ST	
RA4	—	60	G11	I/O	ST	
RA5	—	61	G9	I/O	ST	
RA6	—	91	C5	I/O	ST	
RA7	—	92	B5	I/O	ST	
RA9	—	28	L2	I/O	ST	
RA10	—	29	K3	I/O	ST	
RA14	—	66	E11	I/O	ST	
RA15	—	67	E8	I/O	ST	
RB0	16	25	K2	I/O	ST	PORTB is a bidirectional I/O port.
RB1	15	24	K1	I/O	ST	
RB2	14	23	J2	I/O	ST	
RB3	13	22	J1	I/O	ST	
RB4	12	21	H2	I/O	ST	
RB5	11	20	H1	I/O	ST	
RB6	17	26	L1	I/O	ST	
RB7	18	27	J3	I/O	ST	
RB8	21	32	K4	I/O	ST	
RB9	22	33	L4	I/O	ST	
RB10	23	34	L5	I/O	ST	
RB11	24	35	J5	I/O	ST	
RB12	27	41	J7	I/O	ST	
RB13	28	42	L7	I/O	ST	
RB14	29	43	K7	I/O	ST	
RB15	30	44	L8	I/O	ST	
RC1	—	6	D1	I/O	ST	PORTC is a bidirectional I/O port.
RC2	—	7	E4	I/O	ST	
RC3	—	8	E2	I/O	ST	
RC4	—	9	E1	I/O	ST	
RC12	39	63	F9	I/O	ST	
RC13	47	73	C10	I/O	ST	
RC14	48	74	B11	I/O	ST	
RC15	40	64	F11	I/O	ST	

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer
Analog = Analog input
O = Output
P = Power
I = Input

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

2.11 Referenced Sources

This device data sheet is based on the following individual chapters of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the PIC32MX460F512L product page on the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features, and other documentation, the resulting page provides links to the related family reference manual sections.

- **Section 1. "Introduction"** (DS61127)
- **Section 2. "CPU"** (DS61113)
- **Section 3. "Memory Organization"** (DS61115)
- **Section 4. "Prefetch Cache"** (DS61119)
- **Section 5. "Flash Program Memory"** (DS61121)
- **Section 6. "Oscillator Configuration"** (DS61112)
- **Section 7. "Resets"** (DS61118)
- **Section 8. "Interrupt Controller"** (DS61108)
- **Section 9. "Watchdog Timer and Power-up Timer"** (DS61114)
- **Section 10. "Power-Saving Features"** (DS61130)
- **Section 12. "I/O Ports"** (DS61120)
- **Section 13. "Parallel Master Port (PMP)"** (DS61128)
- **Section 14. "Timers"** (DS61105)
- **Section 15. "Input Capture"** (DS61122)
- **Section 16. "Output Compare"** (DS61111)
- **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS61104)
- **Section 19. "Comparator"** (DS61110)
- **Section 20. "Comparator Voltage Reference (CV$_{REF}$)"** (DS61109)
- **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS61107)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS61106)
- **Section 24. "Inter-Integrated Circuit™ (I^{2}C™)"** (DS61116)
- **Section 27. "USB On-The-Go (OTG)"** (DS61126)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS61125)
- **Section 31. "Direct Memory Access (DMA) Controller"** (DS61117)
- **Section 32. "Configuration"** (DS61124)
- **Section 33. "Programming and Diagnostics"** (DS61129)

NOTES:

TABLE 4-8: INPUT CAPTURE1-5 REGISTERS MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	IC1CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2010	IC1BUF	31:16	IC1BUF<31:0>																xxxx
		15:0																	xxxx
2200	IC2CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2210	IC2BUF	31:16	IC2BUF<31:0>																xxxx
		15:0																	xxxx
2400	IC3CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2410	IC3BUF	31:16	IC3BUF<31:0>																xxxx
		15:0																	xxxx
2600	IC4CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2610	IC4BUF	31:16	IC4BUF<31:0>																xxxx
		15:0																	xxxx
2800	IC5CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2810	IC5BUF	31:16	IC5BUF<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-13: ADC REGISTERS MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9000	AD1CON1(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	FORM<2:0>			SSRC<2:0>			CLRASAM	—	ASAM	SAMP	DONE	0000
9010	AD1CON2(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	VCFG2	VCFG1	VCFG0	OFFCAL	—	CSCNA	—	—	BUFS	—	SMPI<3:0>				BUFM	ALTS	0000
9020	AD1CON3(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ADRC	—	—	SAMC<4:0>					ADCS<7:0>								0000
9040	AD1CHS(1)	31:16	CH0NB	—	—	—	CH0SB<3:0>				CH0NA	—	—	—	CH0SA<3:0>				0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9060	AD1PCFG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PCFG15	PCFG14	PCFG13	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000
9050	AD1CSSL(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0	0000
9070	ADC1BUF0	31:16	ADC Result Word 0 (ADC1BUF0<31:0>)																0000
		15:0																	0000
9080	ADC1BUF1	31:16	ADC Result Word 1 (ADC1BUF1<31:0>)																0000
		15:0																	0000
9090	ADC1BUF2	31:16	ADC Result Word 2 (ADC1BUF2<31:0>)																0000
		15:0																	0000
90A0	ADC1BUF3	31:16	ADC Result Word 3 (ADC1BUF3<31:0>)																0000
		15:0																	0000
90B0	ADC1BUF4	31:16	ADC Result Word 4 (ADC1BUF4<31:0>)																0000
		15:0																	0000
90C0	ADC1BUF5	31:16	ADC Result Word 5 (ADC1BUF5<31:0>)																0000
		15:0																	0000
90D0	ADC1BUF6	31:16	ADC Result Word 6 (ADC1BUF6<31:0>)																0000
		15:0																	0000
90E0	ADC1BUF7	31:16	ADC Result Word 7 (ADC1BUF7<31:0>)																0000
		15:0																	0000
90F0	ADC1BUF8	31:16	ADC Result Word 8 (ADC1BUF8<31:0>)																0000
		15:0																	0000
9100	ADC1BUF9	31:16	ADC Result Word 9 (ADC1BUF9<31:0>)																0000
		15:0																	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-37: PARALLEL MASTER PORT REGISTERS MAP(1)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7000	PMCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN	CSF<1:0>		ALP	CS2P	CS1P	—	WRSP	RDSP	0000
7010	PMMODE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>		WAITB<1:0>		WAITM<3:0>				WAITE<1:0>		0000
7020	PMADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CS2EN/A15	CS1EN/A14	ADDR<13:0>														0000
7030	PMDOUT	31:16	DATAOUT<31:0>																0000
		15:0																	0000
7040	PMDIN	31:16	DATAIN<31:0>																0000
		15:0																	0000
7050	PMAEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PTEN<15:0>																0000
7060	PMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-38: PROGRAMMING AND DIAGNOSTICS REGISTERS MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F200	DDPCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	JTAGEN	TROEN	—	—	0008

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-43: USB REGISTERS MAP(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5040	U1OTGIR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	—	—	—	—	—	—	—	—	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF	0000
5050	U1OTGIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE	0000
5060	U1OTGSTAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD	0000
5070	U1OTGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
5080	U1PWRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UACTPND(4)	—	—	USLPGRD	—	—	USUSPEND	USBPWR	0000
5200	U1IR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF	0000
																		DETACHIF	0000
5210	U1IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE	0000
																		DETACHIE	0000
5220	U1EIR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF	PIDEF	0000
																	EOFEF		0000
5230	U1EIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE	PIDEE	0000
																	EOFEE		0000
5240	U1STAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ENDPT<3:0>(4)				DIR	PPBI	—	—	0000
5250	U1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	JSTATE(4)	SE0(4)	PKTDIS	USBRST	HOSTEN	RESUME	PPBRST	USBEN	0000
													TOKBUSY					SOFEN	0000
5260	U1ADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPDEN	DEVADDR<6:0>							0000
5270	U1BDTP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRL<7:1>							—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

2: This register does not have associated CLR, SET, and INV registers.

3: All bits in this register are read-only; therefore, CLR, SET, and INV registers are not supported.

4: The reset value for this bit is undefined.

TABLE 7-1: INTERRUPT IRQ AND VECTOR LOCATION

Interrupt Source(1)	IRQ	Vector Number	Interrupt Bit Location			
Highest Natural Order Priority			Flag	Enable	Priority	Subpriority
CT – Core Timer Interrupt	0	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>
CS0 – Core Software Interrupt 0	1	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>
CS1 – Core Software Interrupt 1	2	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>
INT0 – External Interrupt 0	3	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>
T1 – Timer1	4	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>
IC1 – Input Capture 1	5	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>
OC1 – Output Compare 1	6	6	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>
INT1 – External Interrupt 1	7	7	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>
T2 – Timer2	8	8	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>
IC2 – Input Capture 2	9	9	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>
OC2 – Output Compare 2	10	10	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>
INT2 – External Interrupt 2	11	11	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>
T3 – Timer3	12	12	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>
IC3 – Input Capture 3	13	13	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>
OC3 – Output Compare 3	14	14	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>
INT3 – External Interrupt 3	15	15	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>
T4 – Timer4	16	16	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>
IC4 – Input Capture 4	17	17	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>
OC4 – Output Compare 4	18	18	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>
INT4 – External Interrupt 4	19	19	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>
T5 – Timer5	20	20	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>
IC5 – Input Capture 5	21	21	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>
OC5 – Output Compare 5	22	22	IFS0<22>	IEC0<22>	IPC5<20:18>	IPC5<17:16>
SPI1E – SPI1 Fault	23	23	IFS0<23>	IEC0<23>	IPC5<28:26>	IPC5<25:24>
SPI1TX – SPI1 Transfer Done	24	23	IFS0<24>	IEC0<24>	IPC5<28:26>	IPC5<25:24>
SPI1RX – SPI1 Receive Done	25	23	IFS0<25>	IEC0<25>	IPC5<28:26>	IPC5<25:24>
U1E – UART1 Error	26	24	IFS0<26>	IEC0<26>	IPC6<4:2>	IPC6<1:0>
U1RX – UART1 Receiver	27	24	IFS0<27>	IEC0<27>	IPC6<4:2>	IPC6<1:0>
U1TX – UART1 Transmitter	28	24	IFS0<28>	IEC0<28>	IPC6<4:2>	IPC6<1:0>
I2C1B – I2C1 Bus Collision Event	29	25	IFS0<29>	IEC0<29>	IPC6<12:10>	IPC6<9:8>
I2C1S – I2C1 Slave Event	30	25	IFS0<30>	IEC0<30>	IPC6<12:10>	IPC6<9:8>
I2C1M – I2C1 Master Event	31	25	IFS0<31>	IEC0<31>	IPC6<12:10>	IPC6<9:8>
CN – Input Change Interrupt	32	26	IFS1<0>	IEC1<0>	IPC6<20:18>	IPC6<17:16>
AD1 – ADC1 Convert Done	33	27	IFS1<1>	IEC1<1>	IPC6<28:26>	IPC6<25:24>
PMP – Parallel Master Port	34	28	IFS1<2>	IEC1<2>	IPC7<4:2>	IPC7<1:0>
CMP1 – Comparator Interrupt	35	29	IFS1<3>	IEC1<3>	IPC7<12:10>	IPC7<9:8>
CMP2 – Comparator Interrupt	36	30	IFS1<4>	IEC1<4>	IPC7<20:18>	IPC7<17:16>

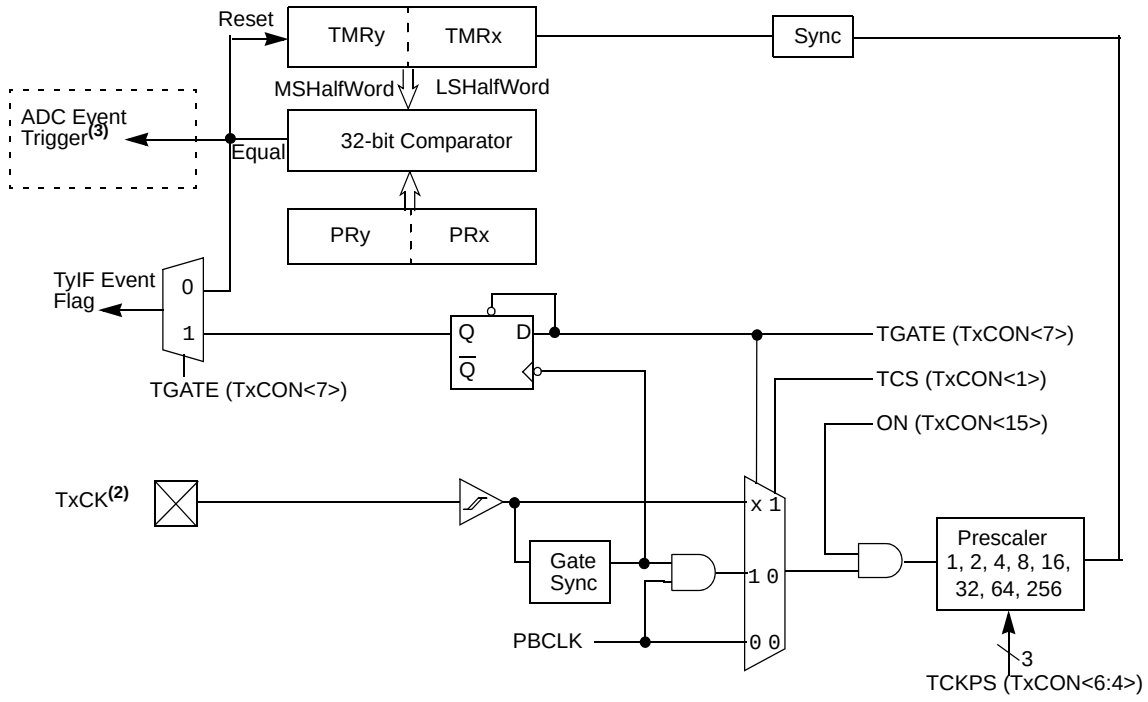
Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MX General Purpose – Features"** and **TABLE 2: "PIC32MX USB – Features"** for available peripherals.

TABLE 7-1: INTERRUPT IRQ AND VECTOR LOCATION (CONTINUED)

Interrupt Source(1)	IRQ	Vector Number	Interrupt Bit Location			
Highest Natural Order Priority			Flag	Enable	Priority	Subpriority
SPI2E – SPI2 Fault	37	31	IFS1<5>	IEC1<5>	IPC7<28:26>	IPC7<25:24>
SPI2TX – SPI2 Transfer Done	38	31	IFS1<6>	IEC1<6>	IPC7<28:26>	IPC7<25:24>
SPI2RX – SPI2 Receive Done	39	31	IFS1<7>	IEC1<7>	IPC7<28:26>	IPC7<25:24>
U2E – UART2 Error	40	32	IFS1<8>	IEC1<8>	IPC8<4:2>	IPC8<1:0>
U2RX – UART2 Receiver	41	32	IFS1<9>	IEC1<9>	IPC8<4:2>	IPC8<1:0>
U2TX – UART2 Transmitter	42	32	IFS1<10>	IEC1<10>	IPC8<4:2>	IPC8<1:0>
I2C2B – I2C2 Bus Collision Event	43	33	IFS1<11>	IEC1<11>	IPC8<12:10>	IPC8<9:8>
I2C2S – I2C2 Slave Event	44	33	IFS1<12>	IEC1<12>	IPC8<12:10>	IPC8<9:8>
I2C2M – I2C2 Master Event	45	33	IFS1<13>	IEC1<13>	IPC8<12:10>	IPC8<9:8>
FSCM – Fail-Safe Clock Monitor	46	34	IFS1<14>	IEC1<14>	IPC8<20:18>	IPC8<17:16>
RTCC – Real-Time Clock and Calendar	47	35	IFS1<15>	IEC1<15>	IPC8<28:26>	IPC8<25:24>
DMA0 – DMA Channel 0	48	36	IFS1<16>	IEC1<16>	IPC9<4:2>	IPC9<1:0>
DMA1 – DMA Channel 1	49	37	IFS1<17>	IEC1<17>	IPC9<12:10>	IPC9<9:8>
DMA2 – DMA Channel 2	50	38	IFS1<18>	IEC1<18>	IPC9<20:18>	IPC9<17:16>
DMA3 – DMA Channel 3	51	39	IFS1<19>	IEC1<19>	IPC9<28:26>	IPC9<25:24>
FCE – Flash Control Event	56	44	IFS1<24>	IEC1<24>	IPC11<4:2>	IPC11<1:0>
USB	57	45	IFS1<25>	IEC1<25>	IPC11<12:10>	IPC11<9:8>
Lowest Natural Order Priority						

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MX General Purpose – Features"** and **TABLE 2: "PIC32MX USB – Features"** for available peripherals.

FIGURE 14-2: TIMER2/3, 4/5 BLOCK DIAGRAM (32-BIT)



Note 1: In this diagram, the use of 'x' in registers TxCON, TMRx, PRx and TxCK refers to either Timer2 or Timer4; the use of 'y' in registers TyCON, TMRy, PRy and TyIF refers to either Timer3 or Timer5.

2: TxCK pins are not available on 64-pin devices.

3: ADC event trigger is available only on Timer2/3 pair.

REGISTER 26-1: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

bit 19-12 **PWP<7:0>:** Program Flash Write-Protect bits

Prevents selected program Flash memory pages from being modified during code execution. The PWP bits represent the one's compliment of the number of write protected program Flash memory pages.

11111111 = Disabled
11111110 = 0xBD00_0FFF
11111101 = 0xBD00_1FFF
11111100 = 0xBD00_2FFF
11111011 = 0xBD00_3FFF
11111010 = 0xBD00_4FFF
11111001 = 0xBD00_5FFF
11111000 = 0xBD00_6FFF
11110111 = 0xBD00_7FFF
11110110 = 0xBD00_8FFF
11110101 = 0xBD00_9FFF
11110100 = 0xBD00_AFFF
11110011 = 0xBD00_BFFF
11110010 = 0xBD00_CFFF
11110001 = 0xBD00_DFFF
11110000 = 0xBD00_EFFF
11101111 = 0xBD00_FFFF
.
.
.
01111111 = 0xBD07_FFFF

bit 11-4 **Reserved:** Write '1'

bit 3 **ICESEL:** In-Circuit Emulator/Debugger Communication Channel Select bit

1 = PGEC2/PGED2 pair is used
0 = PGEC1/PGED1 pair is used

bit 2 **Reserved:** Write '1'

bit 1-0 **DEBUG<1:0>:** Background Debugger Enable bits (forced to '11' if code-protect is enabled)

11 = Debugger disabled
10 = Debugger enabled
01 = Reserved (same as '11' setting)
00 = Reserved (same as '11' setting)

REGISTER 26-3: DEVCFG2: DEVICE CONFIGURATION WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	R/P	R/P	R/P
	—	—	—	—	—	FPLLODIV<2:0>		
15:8	R/P	r-1	r-1	r-1	r-1	R/P	R/P	R/P
	UPLLEN	—	—	—	—	UPLLIDIV<2:0>		
7:0	r-1	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	—	FPLLMUL<2:0>			—	FPLLIDIV<2:0>		

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-19 **Reserved:** Write ‘1’

bit 18-16 **FPLLODIV<2:0>:** Default Postscaler for PLL bits
- 111 = PLL output divided by 256
- 110 = PLL output divided by 64
- 101 = PLL output divided by 32
- 100 = PLL output divided by 16
- 011 = PLL output divided by 8
- 010 = PLL output divided by 4
- 001 = PLL output divided by 2
- 000 = PLL output divided by 1

bit 15 **UPLLEN:** USB PLL Enable bit
- 1 = Disable and bypass USB PLL
- 0 = Enable USB PLL

bit 14-11 **Reserved:** Write ‘1’

bit 10-8 **UPLLIDIV<2:0>:** PLL Input Divider bits
- 111 = 12x divider
- 110 = 10x divider
- 101 = 6x divider
- 100 = 5x divider
- 011 = 4x divider
- 010 = 3x divider
- 010 = 3x divider
- 001 = 2x divider
- 000 = 1x divider

bit 7 **Reserved:** Write ‘1’

bit 6-4 **FPLLMUL<2:0>:** PLL Multiplier bits
- 111 = 24x multiplier
- 110 = 21x multiplier
- 101 = 20x multiplier
- 100 = 19x multiplier
- 011 = 18x multiplier
- 010 = 17x multiplier
- 001 = 16x multiplier
- 000 = 15x multiplier

bit 3 **Reserved:** Write ‘1’

bit 2-0 **FPLLIDIV<2:0>:** PLL Input Divider bits
- 111 = 12x divider
- 110 = 10x divider
- 101 = 6x divider
- 100 = 5x divider
- 011 = 4x divider
- 010 = 3x divider
- 001 = 2x divider
- 000 = 1x divider

28.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

28.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

28.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

28.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

28.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

29.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of PIC32MX3XX/4XX electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MX3XX/4XX are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings (Note 1)

Ambient temperature under bias ..... -40°C to +105°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to V_{SS} **(Note 3)** ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq 2.3V$ **(Note 3)** ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} < 2.3V$ **(Note 3)** ..... -0.3V to +3.6V
Voltage on V_{CORE} with respect to V_{SS} ..... -0.3V to 2.0V
Voltage on V_{BUS} with respect to V_{SS} ..... -0.3V to +5.5V
Maximum current out of V_{SS} pin(s) ..... 300 mA
Maximum current into V_{DD} pin(s) **(Note 2)** ..... 300 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by all ports ..... 200 mA
Maximum current sourced by all ports **(Note 2)** ..... 200 mA

Note 1: Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 29-2).

3: See the **"Pin Diagrams"** section for the 5V tolerant pins.

TABLE 29-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
DI10		I/O pins:					
		with TTL Buffer	VSS	—	0.15 VDD	V	**(Note 4)**
		with Schmitt Trigger Buffer	VSS	—	0.2 VDD	V	**(Note 4)**
DI15		$\overline{MCLR}$	VSS	—	0.2 VDD	V	**(Note 4)**
DI16		OSC1 (XT mode)	VSS	—	0.2 VDD	V	**(Note 4)**
DI17		OSC1 (HS mode)	VSS	—	0.2 VDD	V	**(Note 4)**
DI18		SDAx, SCLx	VSS	—	0.3 VDD	V	SMBus disabled **(Note 4)**
DI19		SDAx, SCLx	VSS	—	0.8	V	SMBus enabled **(Note 4)**
	VIH	**Input High Voltage**					
DI20		I/O pins:					
		with Analog Functions	0.8 VDD	—	VDD	V	**(Note 4)**
		Digital Only	0.8 VDD	—		V	**(Note 4)**
		with TTL Buffer	0.25VDD + 0.8V	—	5.5	V	**(Note 4)**
		with Schmitt Trigger Buffer	0.8 VDD	—	5.5	V	**(Note 4)**
DI25		$\overline{MCLR}$	0.8 VDD	—	VDD	V	**(Note 4)**
DI26		OSC1 (XT mode)	0.7 VDD	—	VDD	V	**(Note 4)**
DI27		OSC1 (HS mode)	0.7 VDD	—	VDD	V	**(Note 4)**
DI28		SDAx, SCLx	0.7 VDD	—	5.5	V	SMBus disabled **(Note 4)**
DI29		SDAx, SCLx	2.1	—	5.5	V	SMBus enabled, 2.3V ≤VPIN ≤5.5 **(Note 4)**
DI30	ICNPU	**CNxx Pull up Current**	50	250	400	µA	VDD = 3.3V, VPIN = VSS
	IIL	**Input Leakage Current**					**(Note 3)**
DI50		I/O Ports	—	—	±1	µA	VSS ≤VPIN ≤VDD, Pin at high-impedance
DI51		Analog Input Pins	—	—	±1	µA	VSS ≤VPIN ≤VDD, Pin at high-impedance
DI55		$\overline{MCLR}$	—	—	±1	µA	VSS ≤VPIN ≤VDD
DI56		OSC1	—	—	±1	µA	VSS ≤VPIN ≤VDD, XT and HS modes

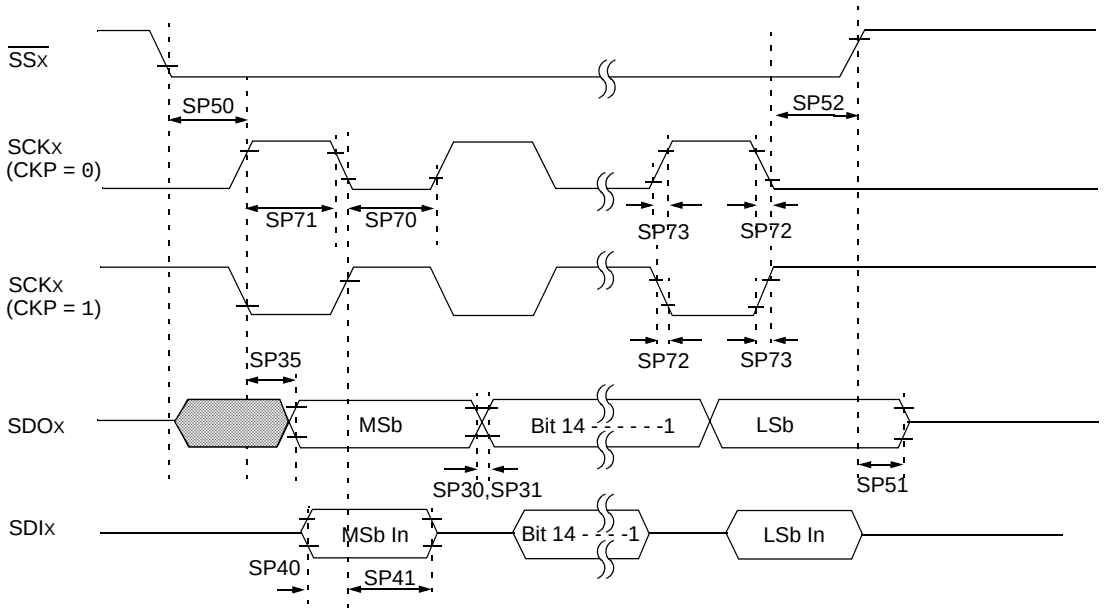
Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: This parameter is characterized, but not tested in manufacturing.

FIGURE 29-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 29-1 for load conditions.

TABLE 29-30: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time(3)	Tsck/2	—	—	ns	—
SP71	TscH	SCKx Input High Time(3)	Tsck/2	—	—	ns	—
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See parameter DO32
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx Data Output Fall Time(4)	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time(4)	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	15	ns	VDD > 2.7V
			—	—	20	ns	VDD < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓to SCKx ↑ or SCKx Input	175	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance(3)	5	—	25	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	Tsck + 20	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

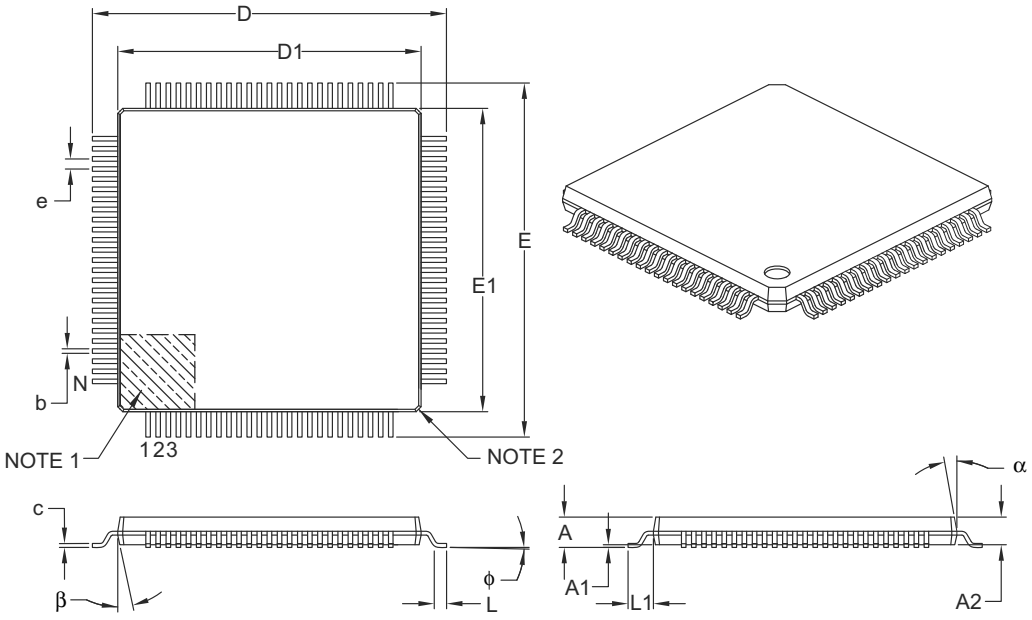
3: The minimum clock period for SCKx is 40 ns.

4: Assumes 50 pF load on all SPIx pins.

NOTES:

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		100	
Lead Pitch	e		0.40 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.13	0.18	0.23
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

TO: Technical Publications Manager
RE: Reader Response

Total Pages Sent _____

From: Name _____

Company _____

Address _____

City / State / ZIP / Country _____

Telephone: (_____) _____ - _____ FAX: (_____) _____ - _____

Application (optional):

Would you like a reply? ___ Y ___ N

Device: PIC32MX3XX/4XX Literature Number: DS61143H

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?