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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx340f512ht-80v-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx340f512ht-80v-pt</a>

# PIC32MX3XX/4XX

**TABLE 1: PIC32MX GENERAL PURPOSE – FEATURES**

GENERAL PURPOSE														
Device	Pins	Packages <sup>(2)</sup>	MHz	Program Memory (KB)	Data Memory (KB)	Timers/Capture/Compare	Programmable DMA Channels	VREG	Trace	EUART/SPI/I <sup>2</sup> C™	10-bit ADC (ch)	Comparators	PMP/PSP	JTAG
PIC32MX320F032H	64	PT, MR	40	32 + 12 <sup>(1)</sup>	8	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX320F064H	64	PT, MR	80	64 + 12 <sup>(1)</sup>	16	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX320F128H	64	PT, MR	80	128 + 12 <sup>(1)</sup>	16	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX340F128H	64	PT, MR	80	128 + 12 <sup>(1)</sup>	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX340F256H	64	PT, MR	80	256 + 12 <sup>(1)</sup>	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX340F512H	64	PT, MR	80	512 + 12 <sup>(1)</sup>	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes
PIC32MX320F128L	100	PT	80	128 + 12 <sup>(1)</sup>	16	5/5/5	0	Yes	No	2/2/2	16	2	Yes	Yes
	121	BG												
PIC32MX340F128L	100	PT	80	128 + 12 <sup>(1)</sup>	32	5/5/5	4	Yes	No	2/2/2	16	2	Yes	Yes
	121	BG												
PIC32MX360F256L	100	PT	80	256 + 12 <sup>(1)</sup>	32	5/5/5	4	Yes	Yes	2/2/2	16	2	Yes	Yes
	121	BG												
PIC32MX360F512L	100	PT	80	512 + 12 <sup>(1)</sup>	32	5/5/5	4	Yes	Yes	2/2/2	16	2	Yes	Yes
	121	BG												

**Legend:** PT = TQFP MR = QFN BG = XBGA

**Note 1:** This device features 12 KB Boot Flash memory.

**2:** See Legend for an explanation of the acronyms. See **Section 30.0 “Packaging Information”** for details.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

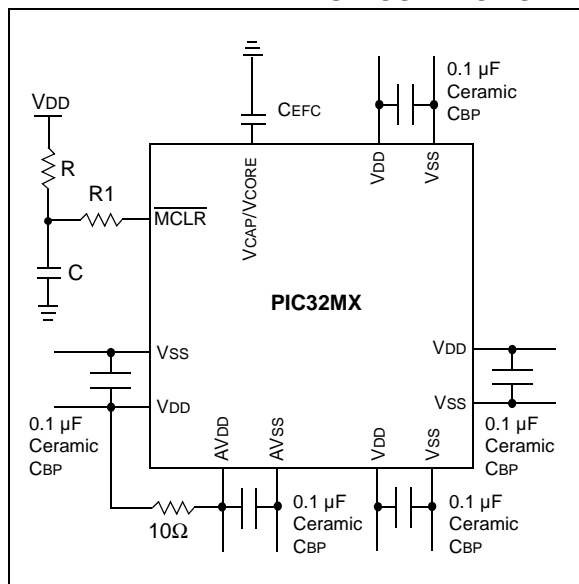
Pin Name	Pin Number <sup>(1)</sup>			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
CN0	48	74	B11	I	ST	Change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
CN1	47	73	C10	I	ST	
CN2	16	25	K2	I	ST	
CN3	15	24	K1	I	ST	
CN4	14	23	J2	I	ST	
CN5	13	22	J1	I	ST	
CN6	12	21	H2	I	ST	
CN7	11	20	H1	I	ST	
CN8	4	10	E3	I	ST	
CN9	5	11	F4	I	ST	
CN10	6	12	F2	I	ST	
CN11	8	14	F3	I	ST	
CN12	30	44	L8	I	ST	
CN13	52	81	C8	I	ST	
CN14	53	82	B8	I	ST	
CN15	54	83	D7	I	ST	
CN16	55	84	C7	I	ST	
CN17	31	49	L10	I	ST	
CN18	32	50	L11	I	ST	
CN19	—	80	D8	I	ST	
CN20	—	47	L9	I	ST	
CN21	—	48	K9	I	ST	
IC1	42	68	E9	I	ST	Capture inputs 1-5.
IC2	43	69	E10	I	ST	
IC3	44	70	D11	I	ST	
IC4	45	71	C11	I	ST	
IC5	52	79	A9	I	ST	
OCFA	17	26	L1	I	ST	Output Compare Fault A Input.
OC1	46	72	D9	O	—	Output Compare output 1.
OC2	49	76	A11	O	—	Output Compare output 2
OC3	50	77	A10	O	—	Output Compare output 3.
OC4	51	78	B9	O	—	Output Compare output 4.
OC5	52	81	C8	O	—	Output Compare output 5.
OCFB	30	44	L8	I	ST	Output Compare Fault B Input.
INT0	35,46	55,72	H9,D9	I	ST	External interrupt 0.
INT1	42	18	61	I	ST	External interrupt 1.
INT2	43	19	62	I	ST	External interrupt 2.

**Legend:** CMOS = CMOS compatible input or output      Analog = Analog input      P = Power  
ST = Schmitt Trigger input with CMOS levels      O = Output      I = Input  
TTL = TTL input buffer

**Note 1:** Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

# PIC32MX3XX/4XX

**FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION**



## 2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7  $\mu\text{F}$  to 47  $\mu\text{F}$ . This capacitor should be located as close to the device as possible.

## 2.3 Capacitor on Internal Voltage Regulator (VCAP/VCORE)

### 2.3.1 INTERNAL REGULATOR MODE

A low-ESR ( $< 1 \text{ Ohm}$ ) capacitor is required on the VCAP/VCORE pin, which is used to stabilize the internal voltage regulator output. The VCAP/VCORE pin must not be connected to VDD, and must have a CEFC capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. Refer to **Section 29.0 “Electrical Characteristics”** for additional information on CEFC specifications. This mode is enabled by connecting the ENVREG pin to VDD.

### 2.3.2 EXTERNAL REGULATOR MODE

In this mode the core voltage is supplied externally through the VCORE/VCAP pin. A low-ESR capacitor of 10  $\mu\text{F}$  is recommended on the VCAP/VCORE pin. This mode is enabled by grounding the ENVREG pin.

The placement of this capacitor should be close to the VCAP/VCORE. It is recommended that the trace length not exceed one-quarter inch (6 mm). Refer to **Section 26.3 “On-Chip Voltage Regulator”** for details.

## 2.4 Master Clear ( $\overline{\text{MCLR}}$ ) Pin

The  $\overline{\text{MCLR}}$  pin provides for two specific device functions:

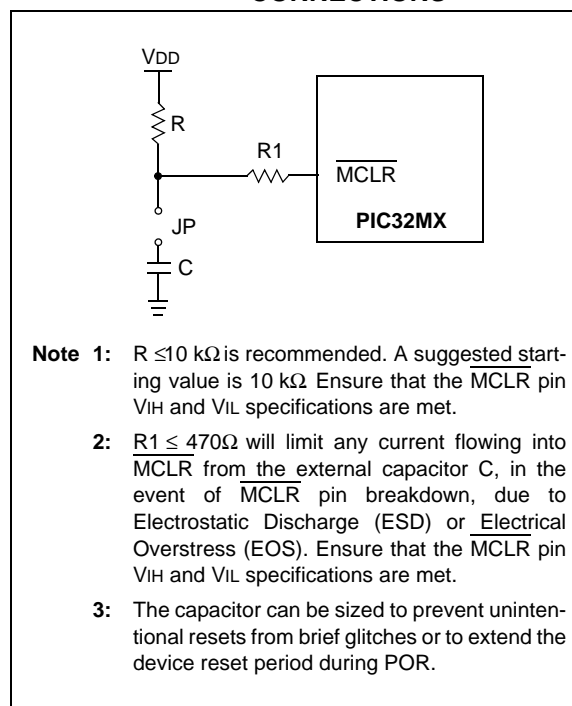
- Device Reset
- Device Programming and Debugging

Pulling The  $\overline{\text{MCLR}}$  pin low generates a device reset. Figure 2-2 illustrates a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels ( $V_{IH}$  and  $V_{IL}$ ) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C, be isolated from the  $\overline{\text{MCLR}}$  pin during programming and debugging operations.

Place the components shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

**FIGURE 2-2: EXAMPLE OF  $\overline{\text{MCLR}}$  PIN CONNECTIONS**



## 2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternately, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V<sub>IH</sub>) and input low (V<sub>IL</sub>) requirements.

Ensure that the “Communication Channel Select” (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 2, MPLAB ICD 3 or MPLAB REAL ICE™.

For more information on ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- “MPLAB® ICD 2 In-Circuit Debugger User’s Guide” DS51331
- “Using MPLAB® ICD 2” (poster) DS51265
- “MPLAB® ICD 2 Design Advisory” DS51566
- “Using MPLAB® ICD 3” (poster) DS51765
- “MPLAB® ICD 3 Design Advisory” DS51764
- “MPLAB® REAL ICE™ In-Circuit Debugger User’s Guide” DS51616
- “Using MPLAB® REAL ICE™” (poster) DS51749

## 2.6 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternately, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V<sub>IH</sub>) and input low (V<sub>IL</sub>) requirements.

## 2.7 Trace

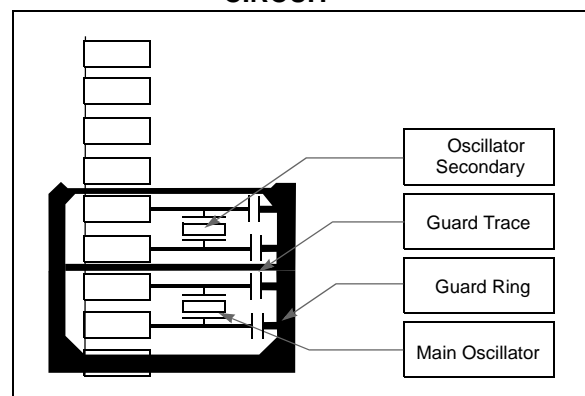
The trace pins can be connected to a hardware-trace-enabled programmer to provide a compress real time instruction trace. When used for trace the TRD3, TRD2, TRD1, TRD0 and TRCLK pins should be dedicated for this use. The trace hardware requires a 22 Ohm series resistor between the trace pins and the trace connector.

## 2.8 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 “Oscillator Configuration”** for details).

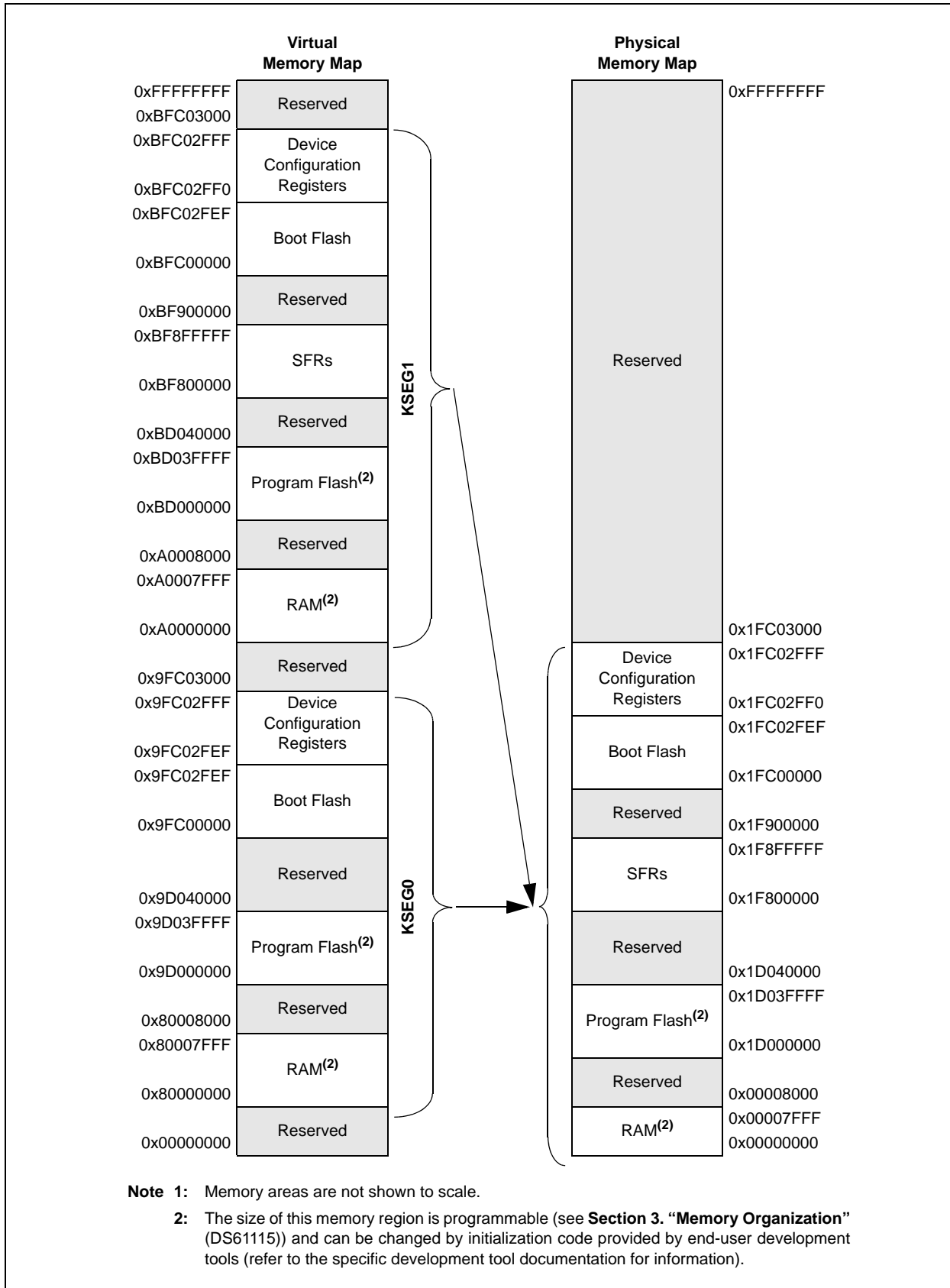
The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

**FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT**



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**FIGURE 4-5: MEMORY MAP ON RESET FOR PIC32MX340F256H, PIC32MX360F256L, PIC32MX440F256H AND PIC32MX460F256L DEVICES<sup>(1)</sup>**



**TABLE 4-14: DMA GLOBAL REGISTERS MAP FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY**

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	DMACON <sup>(1)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	ON	—	SIDL	SUSPEND	—	—	—	—	—	—	—	—	—	—	—	0000	
3010	DMASTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	RDWR	—	DMACH<1:0>		0000	
3020	DMAADDR	31:16	DMAADDR<31:0>																0000
		15:0	DMAADDR<31:0>																0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

**TABLE 4-15: DMA CRC REGISTERS MAP FOR PIC32MX340FXXXX/360FXXXX/440FXXXX/460XXXX DEVICES ONLY<sup>(1)</sup>**

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3030	DCRCCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	PLEN<3:0>				CRCEN	CRCAPP	—	—	—	—	CRCCH<1:0>		0000
3040	DCRCDATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DCRCDATA<15:0>																0000
3050	DCRCXOR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DCRCXOR<15:0>																0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

**TABLE 4-25: PORTD REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L, PIC32MX360F512L, PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY<sup>(1)</sup>**

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
60C0	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FFFF
60D0	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
60E0	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
60F0	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

**TABLE 4-26: PORTD REGISTERS MAP FOR PIC32MX320F032H, PIC32MX320F064H, PIC32MX320F128H, PIC32MX340F128H, PIC32MX340F256H, PIC32MX340F512H, PIC32MX420F032H, PIC32MX440F128H, PIC32MX440F256H AND PIC32MX440F512H DEVICES ONLY<sup>(1)</sup>**

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
60C0	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	0FFF
60D0	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
60E0	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
60F0	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.



**TABLE 4-33: PORTG REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L, PIC32MX360F512L, PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY<sup>(1)</sup>**

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6180	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISG15	TRISG14	TRISG13	TRISG12	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	TRISG3	TRISG2	TRISG1	TRISG0	F3CF
6190	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RG15	RG14	RG13	RG12	—	—	RG9	RG8	RG7	RG6	—	—	RG3	RG2	RG1	RG0	xxxx
61A0	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATG15	LATG14	LATG13	LATG12	—	—	LATG9	LATG8	LATG7	LATG6	—	—	LATG3	LATG2	LATG1	LATG0	xxxx
61B0	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCG15	ODCG14	ODCG13	ODCG12	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	ODCG3	ODCG2	ODCG1	ODCG0	0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

**TABLE 4-34: PORTG REGISTERS MAP FOR PIC32MX320F032H, PIC32MX320F064H, PIC32MX320F128H, PIC32MX340F128H, PIC32MX340F256H, PIC32MX340F512H, PIC32MX420F032H, PIC32MX440F128H, PIC32MX440F256H AND PIC32MX440F512H DEVICES ONLY<sup>(1)</sup>**

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6180	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	TRISG3	TRISG2	—	—	03cc
6190	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RG9	RG8	RG7	RG6	—	—	RG3	RG2	—	—	xxxx
61A0	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATG9	LATG8	LATG7	LATG6	—	—	LATG3	LATG2	—	—	xxxx
61B0	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	ODCG3	ODCG2	—	—	0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

# PIC32MX3XX/4XX

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NOTES:

## 11.0 USB ON-THE-GO (OTG)

**Note 1:** This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 27. “USB On-The-Go (OTG)”** (DS61126) of the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site ([www.microchip.com/PIC32](http://www.microchip.com/PIC32)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded host, full-speed device, or OTG implementation with a minimum of external components. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32MX USB OTG module is presented in Figure 11-1.

The clock generator provides the 48 MHz clock required for USB full-speed and low-speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers, and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

The PIC32MX USB module includes the following features:

- USB Full-Speed Support for Host and Device
- Low-Speed Host Support
- USB OTG Support
- Integrated Signaling Resistors
- Integrated Analog Comparators for VBUS Monitoring
- Integrated USB Transceiver
- Transaction Handshaking Performed by Hardware
- Endpoint Buffering Anywhere in System RAM
- Integrated DMA to Access System RAM and Flash

**Note:** The implementation and use of the USB specifications, as well as other third-party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

# PIC32MX3XX/4XX

## 12.1 Parallel I/O (PIO) Ports

All port pins have three registers (TRIS, LAT and PORT) that are directly associated with their operation.

TRIS is a data direction or tri-state control register that determines whether a digital pin is an input or an output. Setting a TRISx register bit = 1 configures the corresponding I/O pin as an input; setting a TRISx register bit = 0 configures the corresponding I/O pin as an output. All port I/O pins are defined as inputs after a device Reset. Certain I/O pins are shared with analog peripherals and default to analog inputs after a device Reset.

PORT is a register used to read the current state of the signal applied to the port I/O pins. Writing to a PORTx register performs a write to the port's latch, LATx register, latching the data to the port's I/O pins.

LAT is a register used to write data to the port I/O pins. The LATx latch register holds the data written to either the LATx or PORTx registers. Reading the LATx latch register reads the last value written to the corresponding port or latch register.

Not all port I/O pins are implemented on some devices, therefore, the corresponding PORTx, LATx and TRISx register bits will read as zeros.

### 12.1.1 CLR, SET AND INV REGISTERS

Every I/O module register has a corresponding CLR (clear), SET (set) and INV (invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR or INV register, the base register must be read.

**Note:** Using a PORTxINV register to toggle a bit is recommended because the operation is performed in hardware atomically, using fewer instructions as compared to the traditional read-modify-write method shown below:

```
PORTC ^= 0x0001;
```

### 12.1.2 DIGITAL INPUTS

Pins are configured as digital inputs by setting the corresponding TRIS register bits = 1. When configured as inputs, they are either TTL buffers or Schmitt Triggers. Several digital pins share functionality with analog inputs and default to the analog inputs at POR. Setting the corresponding bit in the AD1PCFG register = 1 enables the pin as a digital pin.

The maximum input voltage allowed on the input pins is the same as the maximum  $V_{IH}$  specification. Refer to **Section 29.0 "Electrical Characteristics"** for  $V_{IH}$  specification details.

**Note:** Analog levels on any pin that is defined as a digital input (including the ANx pins) may cause the input buffer to consume current that exceeds the device specifications.

### 12.1.3 ANALOG INPUTS

Certain pins can be configured as analog inputs used by the ADC and Comparator modules. Setting the corresponding bits in the AD1PCFG register = 0 enables the pin as an analog input pin and must have the corresponding TRIS bit set = 1 (input). If the TRIS bit is cleared = 0 (output), the digital output level ( $V_{OH}$  or  $V_{OL}$ ) will be converted. Any time a port I/O pin is configured as analog, its digital input is disabled and the corresponding PORTx register bit will read '0'. The AD1PCFG Register has a default value of 0x0000; therefore, all pins that share ANx functions are analog (not digital) by default.

### 12.1.4 DIGITAL OUTPUTS

Pins are configured as digital outputs by setting the corresponding TRIS register bits = 0. When configured as digital outputs, these pins are CMOS drivers or can be configured as open drain outputs by setting the corresponding bits in the ODCx Open-Drain Configuration register.

The open-drain feature allows the generation of outputs higher than  $V_{DD}$  (e.g., 5V) on any desired 5V tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum  $V_{IH}$  specification.

See the **"Pin Diagrams"** section for the available pins and their functionality.

### 12.1.5 ANALOG OUTPUTS

Certain pins can be configured as analog outputs, such as the CVREF output voltage used by the comparator module. Configuring the Comparator Reference module to provide this output will present the analog output voltage on the pin, independent of the TRIS register setting for the corresponding pin.

### 12.1.6 INPUT CHANGE NOTIFICATION

The input change notification function of the I/O ports (CNx) allows devices to generate interrupt requests in response to change of state on selected pin.

Each CNx pin also has a weak pull-up, which acts as a current source connected to the pin. The pull-ups are enabled by setting corresponding bit in CNPUE register.

# PIC32MX3XX/4XX

FIGURE 19-2: TRANSMISSION (8-BIT OR 9-BIT DATA)

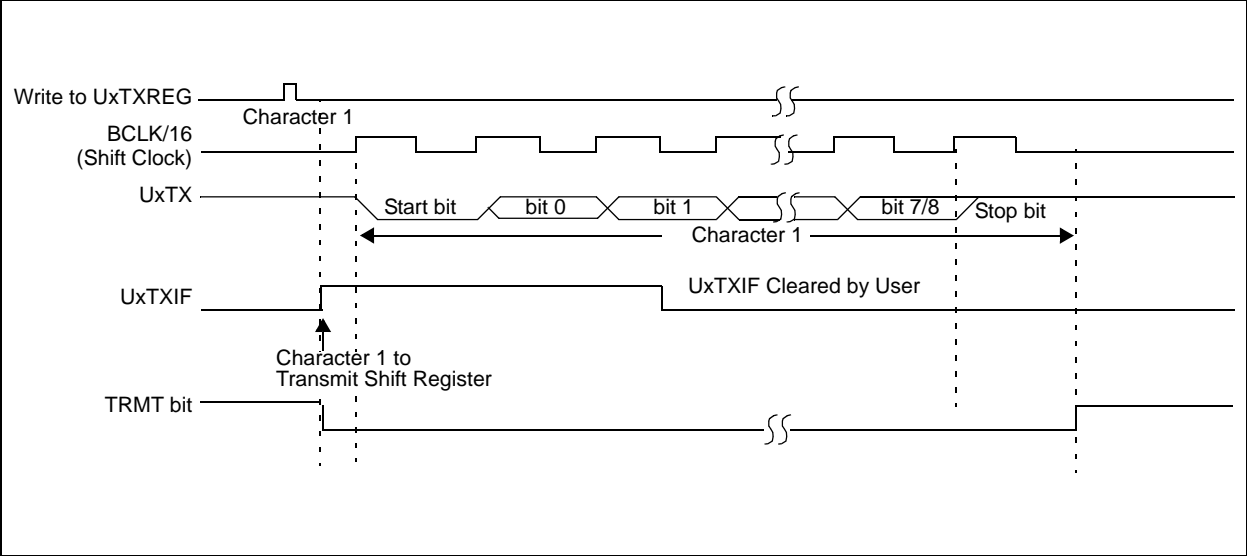
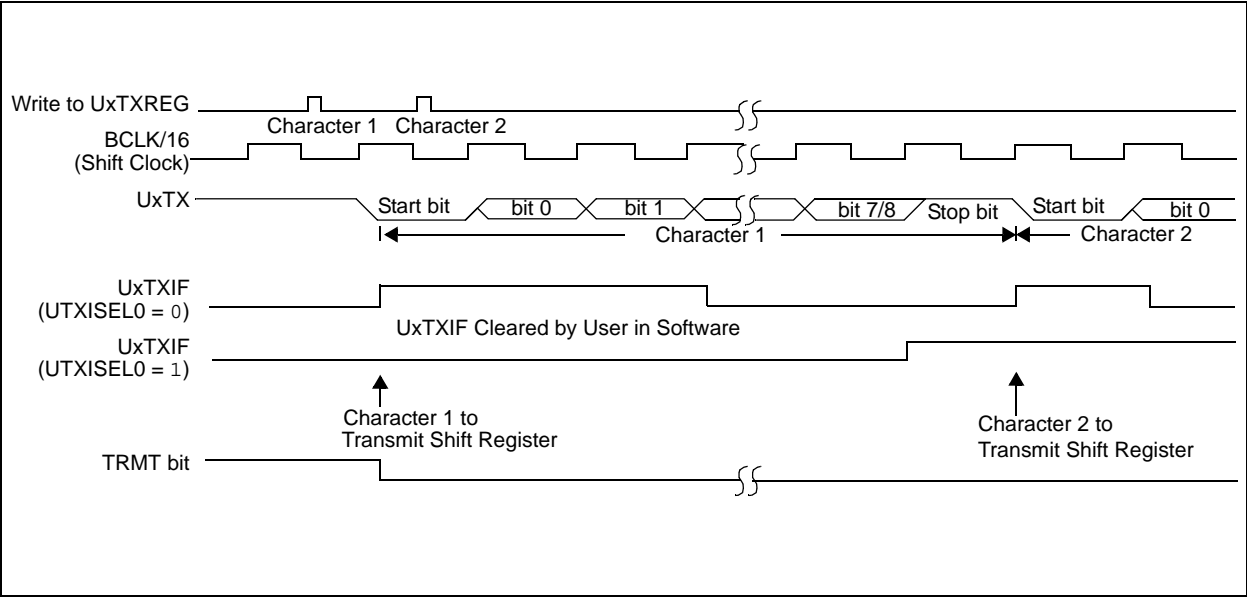


FIGURE 19-3: TWO CONSECUTIVE TRANSMISSIONS



## 20.0 PARALLEL MASTER PORT (PMP)

**Note 1:** This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. “Parallel Master Port (PMP)”** (DS61128) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com/PIC32](http://www.microchip.com/PIC32)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

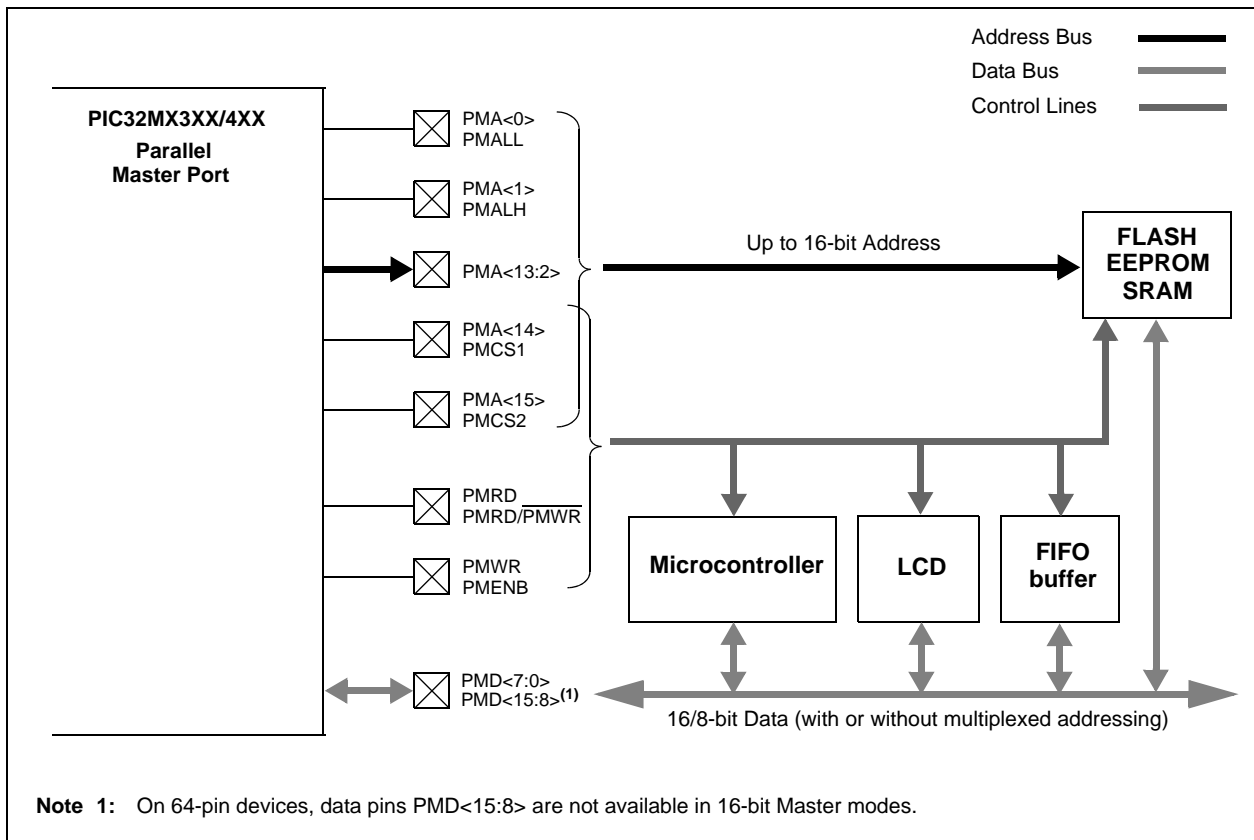
The PMP is a parallel 8-bit/16-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable.

Key features of the PMP module include:

- 8-bit, 16-bit interface
- Up to 16 programmable address lines
- Up to two Chip Select lines
- Programmable strobe options
  - Individual read and write strobes, or
  - Read/write strobe with enable strobe
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- Parallel Slave Port support
  - Legacy addressable
  - Address support
  - 4-byte deep auto-incrementing buffer
- Programmable Wait states
- Operate during CPU Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers
- Freeze option for in-circuit debugging

**Note:** On 64-pin devices, data pins PMD<15:8> are not available.

**FIGURE 20-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES**



**TABLE 27-1: MIPS32® INSTRUCTION SET (CONTINUED)**

Instruction	Description	Function
TGE	Trap if Greater Than or Equal	if (int)Rs >= (int)Rt TrapException
TGEI	Trap if Greater Than or Equal Immediate	if (int)Rs >= (int)Immed TrapException
TGEIU	Trap if Greater Than or Equal Immediate Unsigned	if (uns)Rs >= (uns)Immed TrapException
TGEU	Trap if Greater Than or Equal Unsigned	if (uns)Rs >= (uns)Rt TrapException
TLT	Trap if Less Than	if (int)Rs < (int)Rt TrapException
TLTI	Trap if Less Than Immediate	if (int)Rs < (int)Immed TrapException
TLTIU	Trap if Less Than Immediate Unsigned	if (uns)Rs < (uns)Immed TrapException
TLTU	Trap if Less Than Unsigned	if (uns)Rs < (uns)Rt TrapException
TNE	Trap if Not Equal	if Rs != Rt TrapException
TNEI	Trap if Not Equal Immediate	if Rs != (int)Immed TrapException
WAIT	Wait for Interrupt	Go to a low power mode and stall until interrupt occurs
WRPGPR	Write to GPR in Previous Shadow Set	SGPR[SRSCtl <sub>PSS</sub> , Rd] = Rt
WSBH	Word Swap Bytes Within Halfwords	Rd = Rt <sub>23..16</sub>    Rt <sub>31..24</sub>    Rt <sub>7..0</sub>    Rt <sub>15..8</sub>
XOR	Exclusive OR	Rd = Rs ^ Rt
XORI	Exclusive OR Immediate	Rt = Rs ^ (uns)Immed

**Note 1:** This instruction is deprecated and should not be used.

**TABLE 29-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

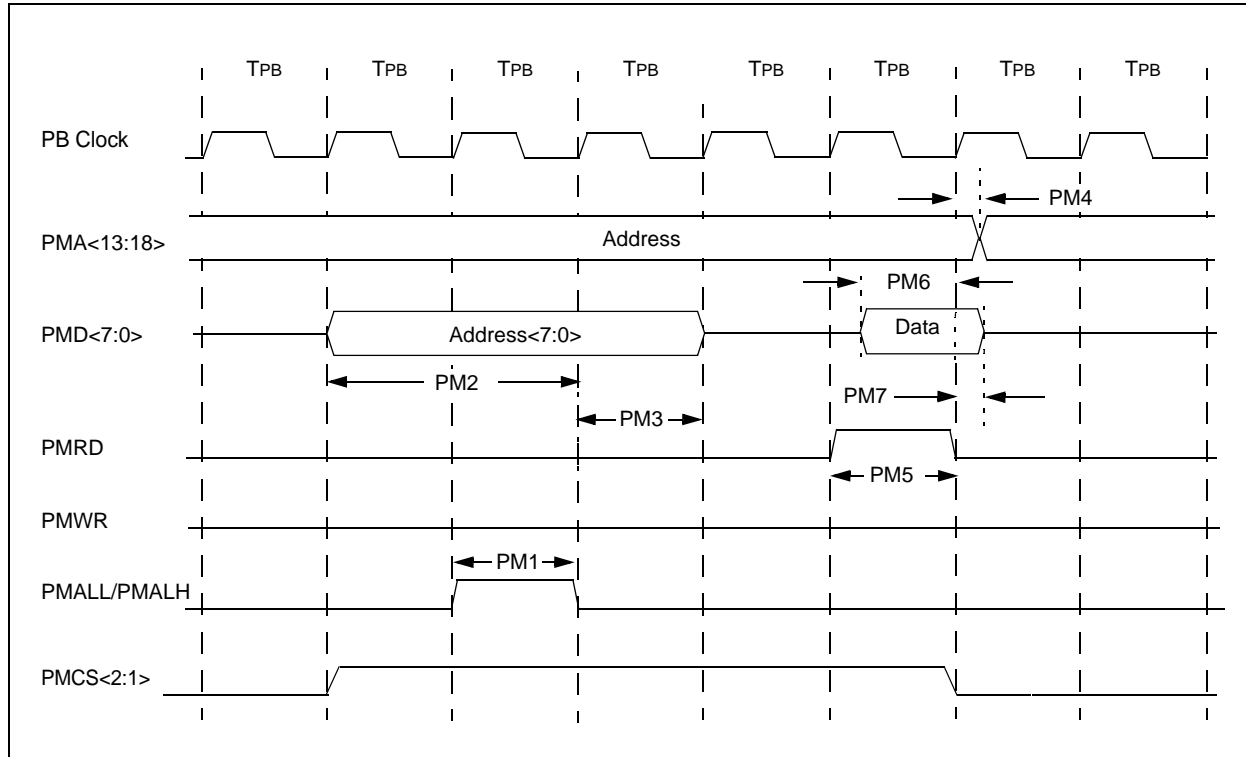
DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature    -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp					
Param. No.	Typical <sup>(3)</sup>	Max.	Units	Conditions				
Operating Current (IDD) <sup>(1,2)</sup>								
DC20	8.5	13	mA	Code executing from Flash	-40°C, +25°C, +85°C	—	4 MHz	
	9	15			+105°C			
DC20c	4.0	—	mA	Code executing from SRAM	—			
DC21	23.5	32	mA	Code executing from Flash	—	—	20 MHz (Note 4)	
DC21c	16.4	—	mA	Code executing from SRAM				
DC22	48	61	mA	Code executing from Flash	—	—	60 MHz (Note 4)	
DC22c	45	—	mA	Code executing from SRAM				
DC23	55	75	mA	Code executing from Flash	-40°C, +25°C, +85°C	2.3V	80 MHz	
	60	100			+105°C			
DC23c	55	—	mA	Code executing from SRAM	—	—		
DC24	—	100	μA	—	-40°C	2.3V	LPRC (31 kHz) (Note 4)	
DC24a	—	130	μA	—	+25°C			
DC24b	—	670	μA	—	+85°C			
DC24c	—	850	μA	—	+105°C			
DC25	94	—	μA	—	-40°C	3.3V		
DC25a	125	—	μA	—	+25°C			
DC25b	302	—	μA	—	+85°C			
DC25d	400	—	μA	—	+105°C			
DC25c	71	—	μA	Code executing from SRAM	—	—		
DC26	—	110	μA	—	-40°C	3.6V		
DC26a	—	180	μA	—	+25°C			
DC26b	—	700	μA	—	+85°C			
DC26c	—	900	μA	—	+105°C			

- Note 1:** A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type as well as temperature can have an impact on the current consumption.
- 2:** The test conditions for IDD measurements are as follows: Oscillator mode = EC+PLL with OSC1 driven by external square wave from rail to rail and PBCLK divisor = 1:8. CPU, Program Flash and SRAM data memory are operational, Program Flash memory Wait states = 7, program cache and prefetch are disabled and SRAM data memory Wait states = 1. All peripheral modules are disabled (ON bit = 0). WDT and FSCM are disabled. All I/O pins are configured as inputs and pulled to VSS. MCLR = VDD.
- 3:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.
- 4:** This parameter is characterized, but not tested in manufacturing.



# PIC32MX3XX/4XX

**FIGURE 29-21: PARALLEL MASTER PORT READ TIMING DIAGRAM**

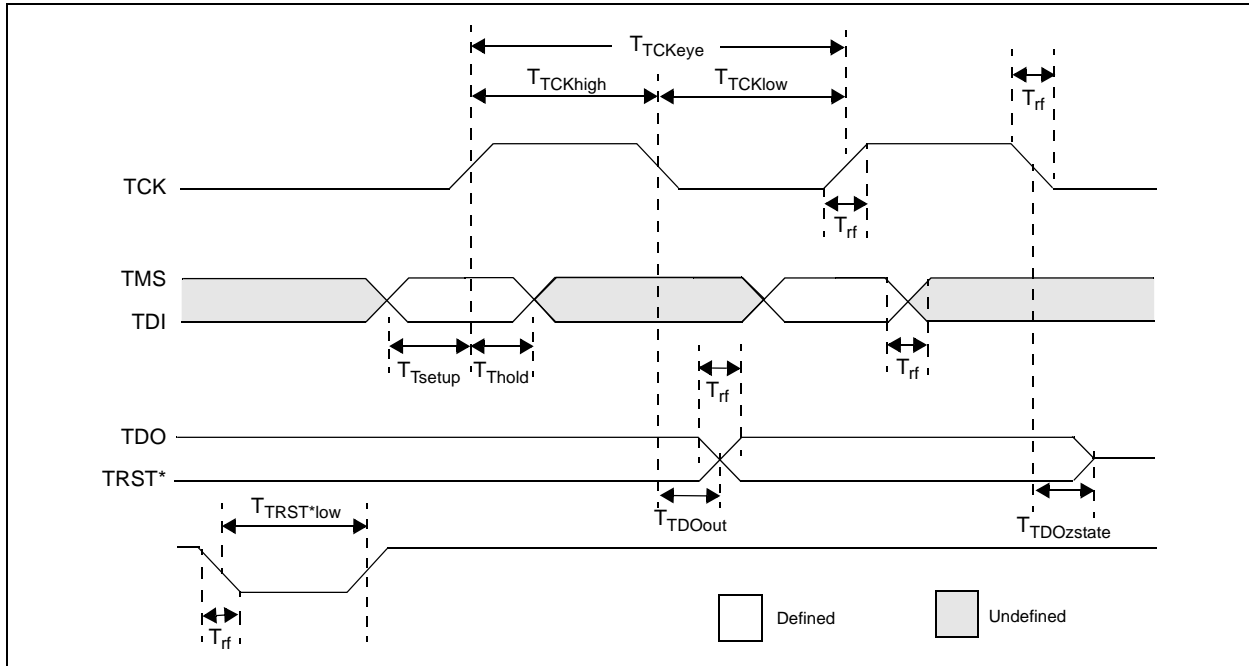


**TABLE 29-38: PARALLEL MASTER PORT READ TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	Symbol	Characteristics <sup>(1)</sup>	Min.	Typical	Max.	Units	Conditions
PM1	TLAT	PMALL/PMALH Pulse Width	—	1 TPB	—	—	—
PM2	TADSU	Address Out Valid to PMALL/PMALH Invalid (address setup time)	—	2 TPB	—	—	—
PM3	TADHOLD	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	1 TPB	—	—	—
PM4	TAHOLD	PMRD Inactive to Address Out Invalid (address hold time)	5	—	—	ns	—
PM5	TRD	PMRD Pulse Width	—	1 TPB	—	—	—
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	15	—	—	ns	—
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)	—	80	—	ns	—

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**FIGURE 29-23: EJTAG TIMING CHARACTERISTICS**



**TABLE 29-41: EJTAG TIMING REQUIREMENTS**

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp		
Param. No.	Symbol	Description <sup>(1)</sup>	Min.	Max.	Units	Conditions
EJ1	TTCKCYC	TCK Cycle Time	25	—	ns	—
EJ2	TTCKHIGH	TCK High Time	10	—	ns	—
EJ3	TTCKLOW	TCK Low Time	10	—	ns	—
EJ4	TTSETUP	TAP Signals Setup Time Before Rising TCK	5	—	ns	—
EJ5	TTHOLD	TAP Signals Hold Time After Rising TCK	3	—	ns	—
EJ6	TTDOOUT	TDO Output Delay Time from Falling TCK	—	5	ns	—
EJ7	TTDOZSTATE	TDO 3-State Delay Time from Falling TCK	—	5	ns	—
EJ8	TTRSTLOW	TRST Low Time	25	—	ns	—
EJ9	TRF	TAP Signals Rise/Fall Time, All Input and Output	—	—	ns	—

**Note 1:** These parameters are characterized, but not tested in manufacturing.

\_\_\_\_\_

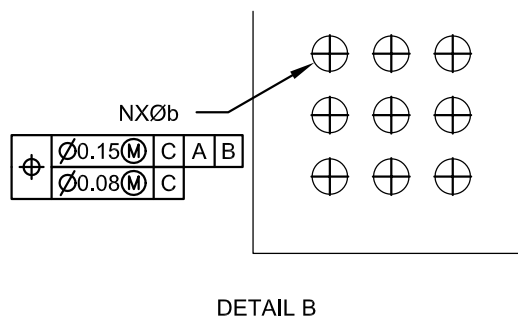
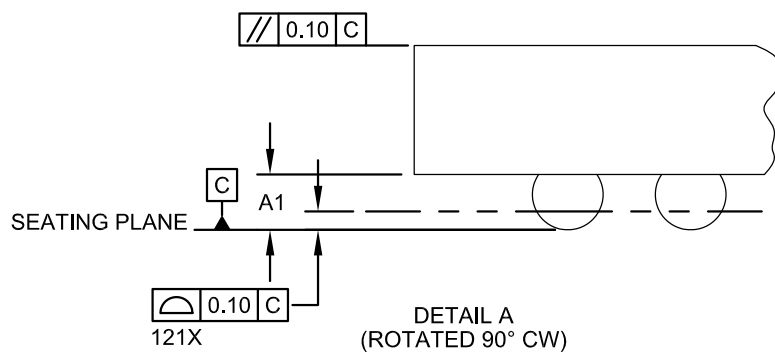
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



# PIC32MX3XX/4XX

### 121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [XBGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Contacts	N	121		
Contact Pitch	e	0.80 BSC		
Overall Height	A	1.00	1.10	1.20
Standoff	A1	0.25	0.30	0.35
Molded Package Thickness	A2	0.55	0.60	0.65
Overall Width	E	10.00 BSC		
Array Width	E1	8.00 BSC		
Overall Length	D	10.00 BSC		
Array Length	D1	8.00 BSC		
Contact Diameter	b	0.40 TYP		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M.  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.
3. The outer rows and columns of balls are located with respect to datums A and B.

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## W

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