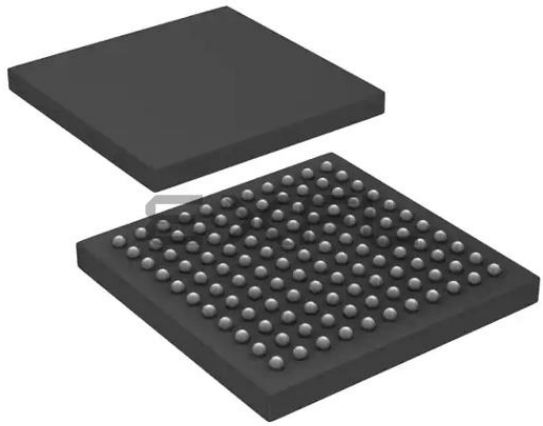
Microchip Technology - PIC32MX360F512L-80V/BG Datasheet



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Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx360f512l-80v-bg

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TABLE 4-25: PORTD REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L, PIC32MX360F512L, PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
60C0	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FFFF
60D0	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
60E0	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
60F0	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-26: PORTD REGISTERS MAP FOR PIC32MX320F032H, PIC32MX320F064H, PIC32MX320F128H, PIC32MX340F128H, PIC32MX340F256H, PIC32MX340F512H, PIC32MX420F032H, PIC32MX440F128H, PIC32MX440F256H AND PIC32MX440F512H DEVICES ONLY(1)

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
60C0	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	0FFF
60D0	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
60E0	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
60F0	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-37: PARALLEL MASTER PORT REGISTERS MAP(1)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7000	PMCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN	CSF<1:0>		ALP	CS2P	CS1P	—	WRSP	RDSP	0000
7010	PMMODE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>		WAITB<1:0>		WAITM<3:0>				WAITE<1:0>		0000
7020	PMADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CS2EN/A15	CS1EN/A14	ADDR<13:0>														0000
7030	PMDOUT	31:16	DATAOUT<31:0>																0000
		15:0																	0000
7040	PMDIN	31:16	DATAIN<31:0>																0000
		15:0																	0000
7050	PMAEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PTEN<15:0>																0000
7060	PMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

TABLE 4-38: PROGRAMMING AND DIAGNOSTICS REGISTERS MAP

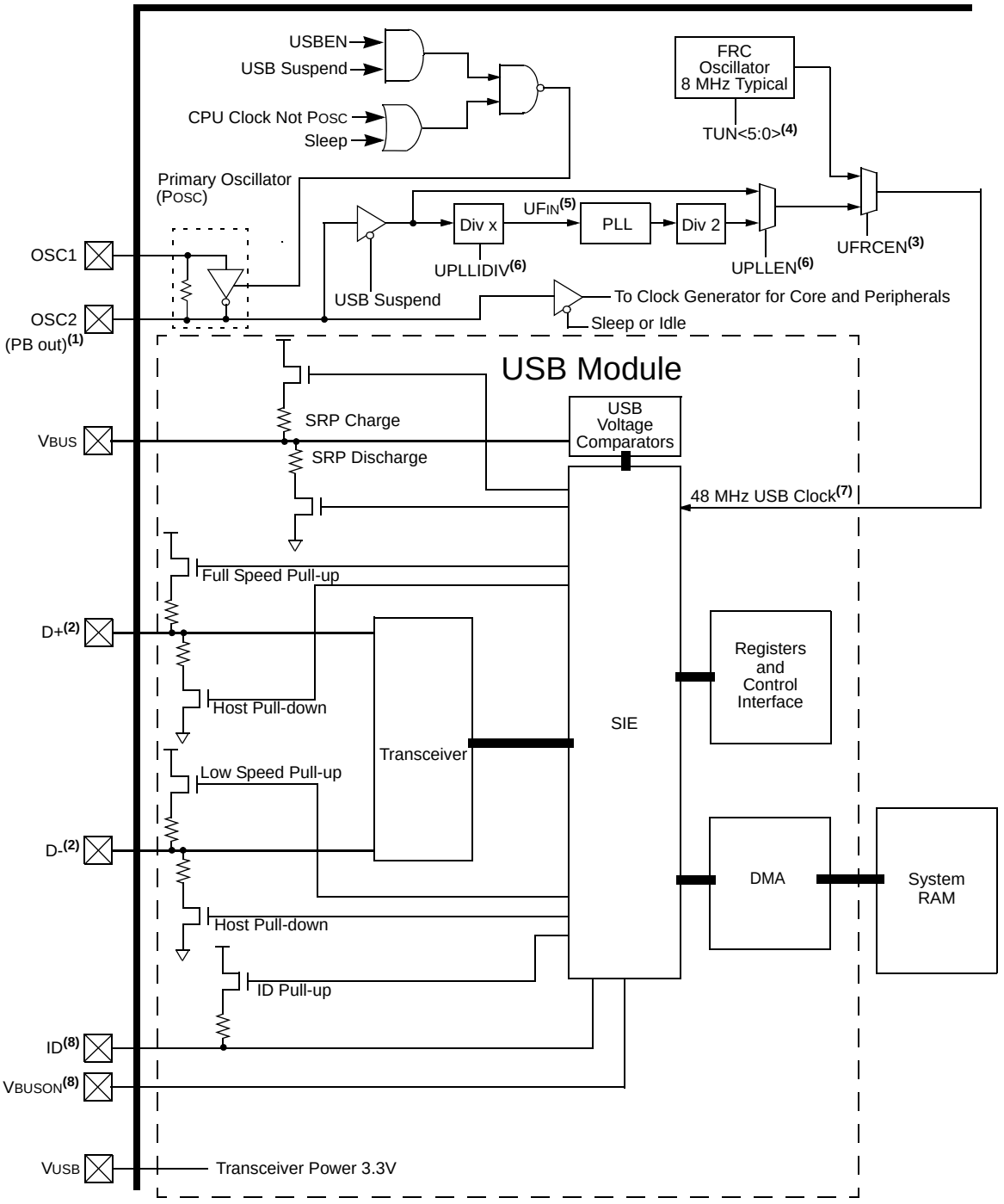
Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F200	DDPCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	JTAGEN	TROEN	—	—	0008

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

NOTES:

NOTES:

FIGURE 11-1: PIC32MX3XX/4XX FAMILY USB INTERFACE DIAGRAM



Note 1: PB clock is only available on this pin for select EC modes.
2: Pins can be used as digital inputs when USB is not enabled.
3: This bit field is contained in the OSCCON register.
4: This bit field is contained in the OSCTRM register.
5: USB PLL UFIN requirements: 4 MHz.
6: This bit field is contained in the DEVCFG2 register.
7: A 48 MHz clock is required for proper USB operation.
8: Pins can be used as GPIO when the USB module is disabled.

18.0 INTER-INTEGRATED CIRCUIT™ (I^2C™)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. "Inter-Integrated Circuit (I^2C™)"** (DS61116) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The I^2C module provides complete hardware support for both Slave and Multi-Master modes of the I^2C serial communication standard. Figure 18-1 illustrates the I^2C module block diagram.

The PIC32MX3XX/4XX devices have up to two I^2C interface modules, denoted as I2C1 and I2C2. Each I^2C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I^2C module, 'I2Cx' (x = 1 or 2), offers the following key features:

- I^2C Interface Supporting both Master and Slave Operation.
- I^2C Slave Mode Supports 7 and 10-bit Address.
- I^2C Master Mode Supports 7 and 10-bit Address.
- I^2C Port allows Bidirectional Transfers between Master and Slaves.
- Serial Clock Synchronization for I^2C Port can be used as a Handshake Mechanism to Suspend and Resume Serial Transfer (SCLREL control).
- I^2C Supports Multi-master Operation; Detects Bus Collision and Arbitrates Accordingly.
- Provides Support for Address Bit Masking.

26.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the PIC32MX3XX/4XX family family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog Timer and Power-up Timer"** (DS61114), **Section 32. "Configuration"** (DS61124) and **Section 33. "Programming and Diagnostics"** (DS61129) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX3XX/4XX devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. These are:

- Flexible Device Configuration
- Watchdog Timer
- JTAG Interface
- In-Circuit Serial Programming™ (ICSP™)

26.1 Configuration Bits

The Configuration bits can be programmed to select various device configurations.

REGISTER 26-1: DEVCFG0: DEVICE CONFIGURATION WORD 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-0	r-1	r-1	R/P	r-1	r-1	r-1	R/P
	—	—	—	CP	—	—	—	BWP
23:16	r-1	r-1	r-1	r-1	R/P	R/P	R/P	R/P
	—	—	—	—	PWP<7:4>			
15:8	R/P	R/P	R/P	R/P	r-1	r-1	r-1	r-1
	PWP<3:0>				—	—	—	—
7:0	r-1	r-1	r-1	r-1	R/P	r-1	R/P	R/P
	—	—	—	—	ICESEL	—	DEBUG<1:0>	

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: ('0', '1', x = Unknown)		

bit 31 **Reserved:** Write '0'

bit 30-29 **Reserved:** Write '1'

bit 28 **CP:** Code-Protect bit

Prevents boot and program Flash memory from being read or modified by an external programming device.
1 = Protection disabled
0 = Protection enabled

bit 27-25 **Reserved:** Write '1'

bit 24 **BWP:** Boot Flash Write-Protect bit

Prevents boot Flash memory from being modified during code execution.
1 = Boot Flash is writable
0 = Boot Flash is not writable

bit 23-20 **Reserved:** Write '1'

26.3 On-Chip Voltage Regulator

All PIC32MX3XX/4XX device's core and digital logic are designed to operate at a nominal 1.8V. To simplify system designs, most devices in the PIC32MX3XX/4XX incorporate an on-chip regulator providing the required core logic voltage from VDD.

The internal 1.8V regulator is controlled by the ENVREG pin. Tying this pin to VDD enables the regulator, which in turn provides power to the core. A low ESR capacitor (such as tantalum) must be connected to the VCORE/VCAP pin (Figure 26-2). This helps to maintain the stability of the regulator. The recommended value for the filer capacitor is provided in **Section 29.1 "DC Characteristics"**.

Note:	It is important that the low ESR capacitor is placed as close as possible to the VCORE/VCAP pin.

Tying the ENVREG pin to VSS disables the regulator. In this case, separate power for the core logic at a nominal 1.8V must be supplied to the device on the VCORE/VCAP pin.

Alternatively, the VCORE/VCAP and VDD pins can be tied together to operate at a lower nominal voltage. Refer to Figure 26-2 for possible configurations.

26.3.1 ON-CHIP REGULATOR AND POR

When the voltage regulator is enabled, it takes fixed delay for it to generate output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

If the regulator is disabled, a separate Power-up Timer (PWRT) is automatically enabled. The PWRT adds a fixed delay of TPWRT at device start-up. See **Section 29.0 "Electrical Characteristics"** for more information on TPU AND TPWRT.

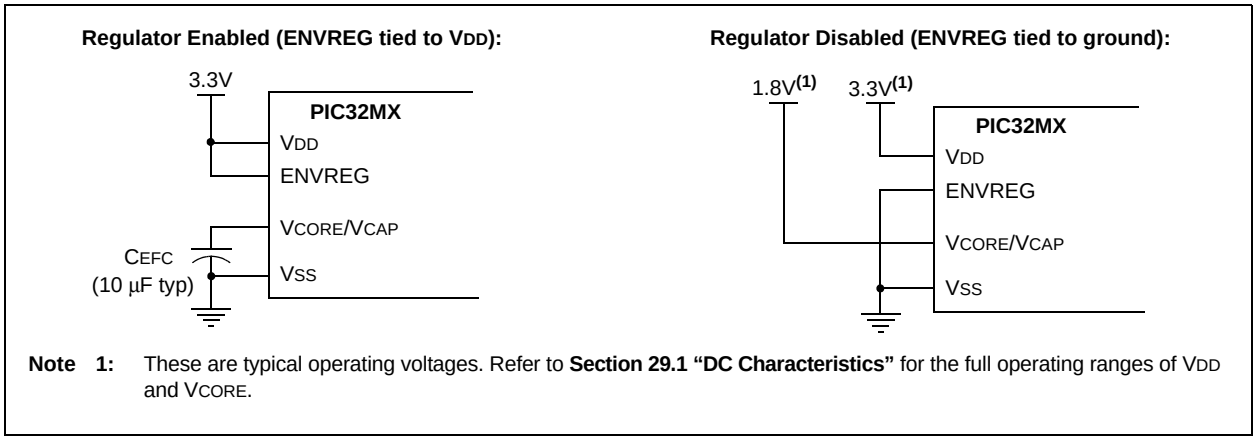
26.3.2 ON-CHIP REGULATOR AND BOR

When the on-chip regulator is enabled, PIC32MX3XX/4XX devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **Section 29.1 "DC Characteristics"**.

26.3.3 POWER-UP REQUIREMENTS

The on-chip regulator is designed to meet the power-up requirements for the device. If the application does not use the regulator, then strict power-up conditions must be adhered to. While powering up, VCORE must never exceed VDD by 0.3 volts.

FIGURE 26-2: CONNECTIONS FOR THE ON-CHIP REGULATOR



Note 1: These are typical operating voltages. Refer to **Section 29.1 "DC Characteristics"** for the full operating ranges of VDD and VCORE.

29.1 DC Characteristics

TABLE 29-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)	Temp. Range (in °C)	Max. Frequency
			PIC32MX3XX/4XX
DC5	2.3V-3.6V	-40°C to +85°C	80 MHz **(Note 1)**
DC5b	2.3V-3.6V	-40°C to +105°C	80 MHz **(Note 1)**

Note 1: 40 MHz maximum for PIC32MX320F032H and PIC32MX420F032H devices.

TABLE 29-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typical	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
V-Temp Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+105	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – S IOH) I/O Pin Power Dissipation: I/O = S ({VDD – VOH} x IOH) + S (VOL x IOL))	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 29-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typical	Max.	Unit	Notes
Package Thermal Resistance, 121-Pin XBGA (10x10x1.1 mm)	θJA	40	—	°C/W	**1**
Package Thermal Resistance, 100-Pin TQFP (12x12x1 mm)	θJA	43	—	°C/W	**1**
Package Thermal Resistance, 64-Pin TQFP (10x10x1 mm)	θJA	47	—	°C/W	**1**
Package Thermal Resistance, 64-Pin QFN (9x9x0.9 mm)	θJA	28	—	°C/W	**1**

Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

TABLE 29-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Operating Voltage							
DC10	VDD	**Supply Voltage**	2.3	—	3.6	V	—
DC12	VDR	**RAM Data Retention Voltage (Note 1)**	1.75	—	—	V	—
DC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	1.75	—	1.95	V	—
DC17	SVDD	**VDD Rise Rate** to Ensure Internal Power-on Reset Signal	0.05	—	—	V/ms	—

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

TABLE 29-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	**Typical(3)**	**Max.**	**Units**	**Conditions**			
Operating Current (IDD)(1,2)							
DC20	8.5	13	mA	Code executing from Flash	-40ºC, +25ºC, +85ºC	—	4 MHz
	9	15			+105ºC		
DC20c	4.0	—	mA	Code executing from SRAM	—		
DC21	23.5	32	mA	Code executing from Flash	—	—	20 MHz **(Note 4)**
DC21c	16.4	—	mA	Code executing from SRAM			
DC22	48	61	mA	Code executing from Flash	—	—	60 MHz **(Note 4)**
DC22c	45	—	mA	Code executing from SRAM			
DC23	55	75	mA	Code executing from Flash	-40ºC, +25ºC, +85ºC	2.3V	80 MHz
	60	100			+105ºC		
DC23c	55	—	mA	Code executing from SRAM	—	—	
DC24	—	100	µA	—	-40°C	2.3V	LPRC (31 kHz) **(Note 4)**
DC24a	—	130	µA	—	+25°C		
DC24b	—	670	µA	—	+85°C		
DC24c	—	850	µA	—	+105ºC		
DC25	94	—	µA	—	-40°C	3.3V	
DC25a	125	—	µA	—	+25°C		
DC25b	302	—	µA	—	+85°C		
DC25d	400	—	µA	—	+105ºC		
DC25c	71	—	µA	Code executing from SRAM	—	—	
DC26	—	110	µA	—	-40°C	3.6V	
DC26a	—	180	µA	—	+25°C		
DC26b	—	700	µA	—	+85°C		
DC26c	—	900	µA	—	+105ºC		

Note 1: A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type as well as temperature can have an impact on the current consumption.

2: The test conditions for IDD measurements are as follows: Oscillator mode = EC+PLL with OSC1 driven by external square wave from rail to rail and PBCLK divisor = 1:8. CPU, Program Flash and SRAM data memory are operational, Program Flash memory Wait states = 7, program cache and prefetch are disabled and SRAM data memory Wait states = 1. All peripheral modules are disabled (ON bit = 0). WDT and FSCM are disabled. All I/O pins are configured as inputs and pulled to VSS. MCLR = VDD.

3: Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

4: This parameter is characterized, but not tested in manufacturing.

TABLE 29-11: DC CHARACTERISTICS: PROGRAM MEMORY(3)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	1000	—	—	E/W	—
D131	VPR	VDD for Read	VMIN	—	3.6	V	—
D132	VPEW	VDD for Erase or Write	3.0	—	3.6	V	—
D134	TRETD	Characteristic Retention	20	—	—	Year	—
D135	IDDP	Supply Current during Programming	—	10	—	mA	—
	TWW	Word Write Cycle Time	20	—	40	µs	—
D136	TRW	Row Write Cycle Time(2) (128 words per row)	3	4.5	—	ms	—
D137	TPE	Page Erase Cycle Time	20	—	—	ms	—
	TCE	Chip Erase Cycle Time	80	—	—	ms	—
D138	LVDstartup	Flash LVD Delay	—	—	6	µs	—

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

2: The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

3: Refer to the "*PIC32MX Flash Programming Specification*" (DS61145) for operating conditions during programming and erase cycles.

TABLE 29-12: PROGRAM FLASH MEMORY WAIT STATE CHARACTERISTICS

DC CHARACTERISTICS	Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp		
Required Flash wait states	**SYSCLK**	**Units**	**Comments**
0 Wait State	0 to 30	MHz	—
1 Wait State	31 to 60		
2 Wait States	61 to 80		

Note 1: 40 MHz maximum for PIC32MX320F032H and PIC32MX420F032H devices.

29.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX3XX/4XX AC characteristics and timing parameters.

FIGURE 29-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

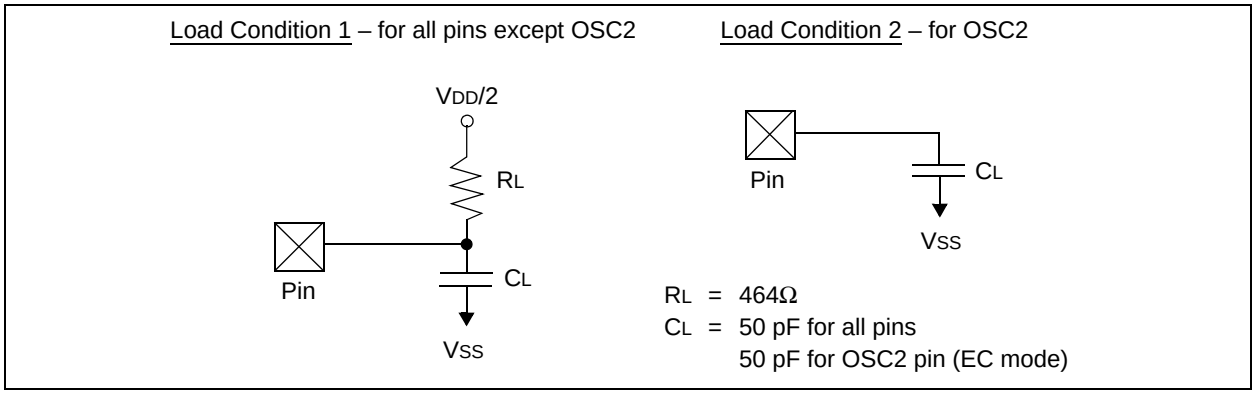


TABLE 29-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
DO56	CIO	All I/O pins and OSC2	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I^2C™ mode

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 29-2: EXTERNAL CLOCK TIMING

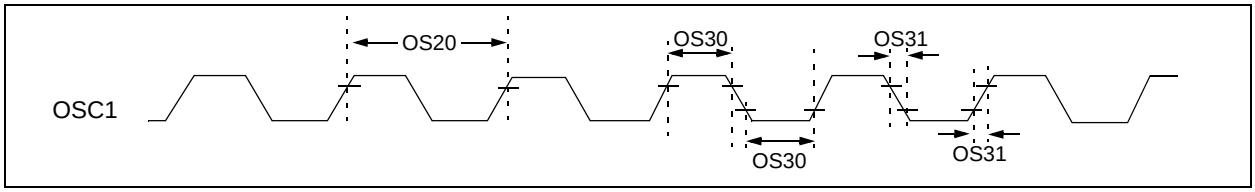


TABLE 29-17: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
OS10	FOSC	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4	— —	50(3) 50(5)	MHz MHz	EC **(Note 5)** ECPLL **(Note 4)**
OS11		Oscillator Crystal Frequency	3	—	10	MHz	XT **(Note 5)**
OS12			4	—	10	MHz	XTPLL **(Notes 4, 5)**
OS13			10	—	25	MHz	HS **(Note 5)**
OS14			10	—	25	MHz	HSPLL **(Notes 4, 5)**
OS15			32	32.768	100	kHz	SOSC **(Note 5)**
OS20	TOSC	TOSC = 1/FOSC = TCY(2)	—	—	—	—	See parameter OS10 for FOSC value
OS30	TOSL, TOSH	External Clock In (OSC1) High or Low Time	0.45 x TOSC	—	—	ns	EC **(Note 5)**
OS31	TOSR, TOSF	External Clock In (OSC1) Rise or Fall Time	—	—	0.05 x TOSC	ns	EC **(Note 5)**
OS40	TOST	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, XT, XTPLL and SOSC Clock Oscillator modes)	—	1024	—	TOSC	**(Note 5)**
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	**(Note 5)**
OS42	GM	External Oscillator Transconductance	—	12	—	mA/V	VDD = 3.3V TA = +25°C **(Note 5)**

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are characterized but are not tested.

2: Instruction cycle period (TCY) equals the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin.

3: 40 MHz maximum for PIC32MX320F032H and PIC32MX420F032H devices.

4: PLL input requirements: 4 MHz ≤FPLLIN ≤5 MHz (use PLL prescaler to reduce FOSC). This parameter is characterized, but tested at 10 MHz only at manufacturing.

5: This parameter is characterized, but not tested in manufacturing.

TABLE 29-18: PLL CLOCK TIMING SPECIFICATIONS (V_{DD} = 2.3V TO 3.6V)

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
OS50	FPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	4	—	5	MHz	ECPLL, HSPLL, XTPLL, FRCPLL modes
OS51	FSYS	On-Chip VCO System Frequency	60	—	120	MHz	—
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	2	ms	—
OS53	DCLK	CLKO Stability(2) (Period Jitter or Cumulative)	-0.25	—	+0.25	%	Measured over 100 ms period

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{SYSCLK}{CommunicationClock}}}$$

For example, if SYSCLK = 80 MHz and SPI bit rate = 20 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{80}{20}}} = \frac{D_{CLK}}{2}$$

TABLE 29-19: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Internal FRC Accuracy @ 8.00 MHz(1)						
F20	FRC	-2	—	+2	%	—

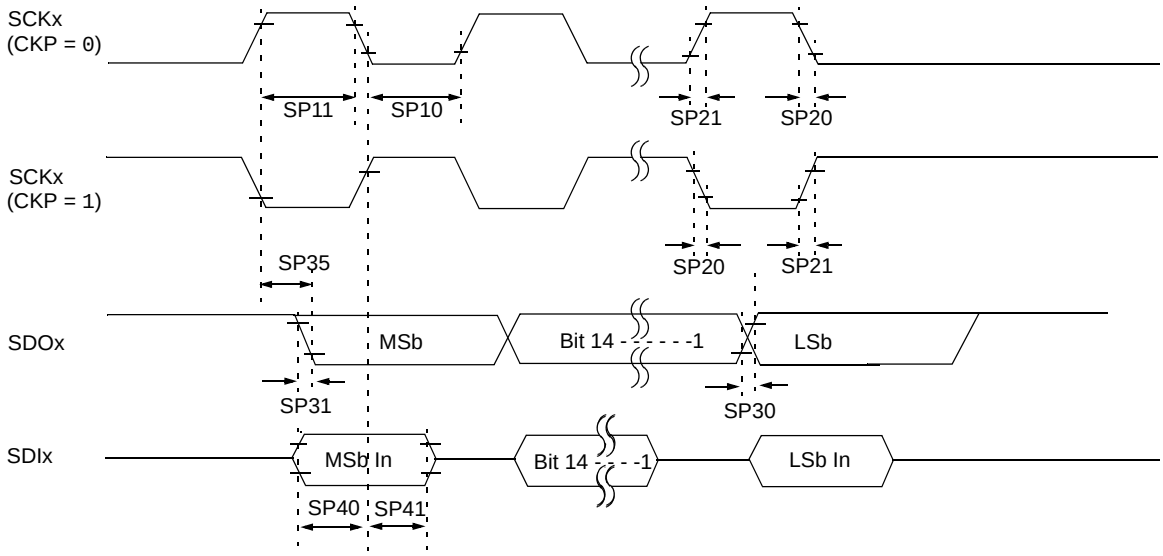
Note 1: Frequency calibrated at 25°C and 3.3V. TUN bits can be used to compensate for temperature drift.

TABLE 29-20: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
LPRC @ 31.25 kHz(1)						
F21	LPRC	-15	—	+15	%	—

Note 1: Change of LPRC frequency as V_{DD} changes.

FIGURE 29-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 29-1 for load conditions.

TABLE 29-28: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
SP10	TscL	SCKx Output Low Time(3)	Tsck/2	—	—	ns	—
SP11	TscH	SCKx Output High Time(3)	Tsck/2	—	—	ns	—
SP20	TscF	SCKx Output Fall Time(4)	—	—	—	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time(4)	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx Data Output Fall Time(4)	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time(4)	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	15	ns	VDD > 2.7V
			—	—	20	ns	VDD < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—

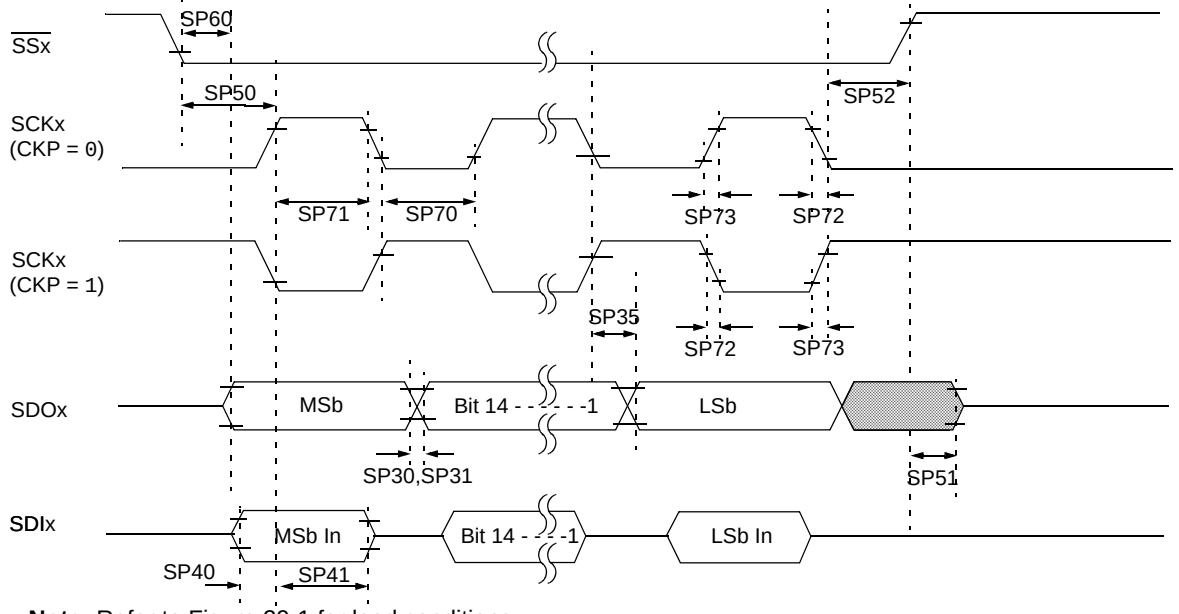
Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

FIGURE 29-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 29-1 for load conditions.

TABLE 29-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 2.3V to 3.6V** (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time(3)	Tsck/2	—	—	ns	—
SP71	TscH	SCKx Input High Time(3)	Tsck/2	—	—	ns	—
SP72	TscF	SCKx Input Fall Time	—	5	10	ns	—
SP73	TscR	SCKx Input Rise Time	—	5	10	ns	—
SP30	TdoF	SDOx Data Output Fall Time(4)	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time(4)	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	20	ns	VDD > 2.7V
			—	—	30	ns	VDD < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓to SCKx ↓or SCKx ↑ Input	175	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance(4)	5	—	25	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	Tsck + 20	—	—	ns	—
SP60	TssL2doV	$\overline{SDOx}$ Data Output Valid after $\overline{SSx}$ Edge	—	—	25	ns	—

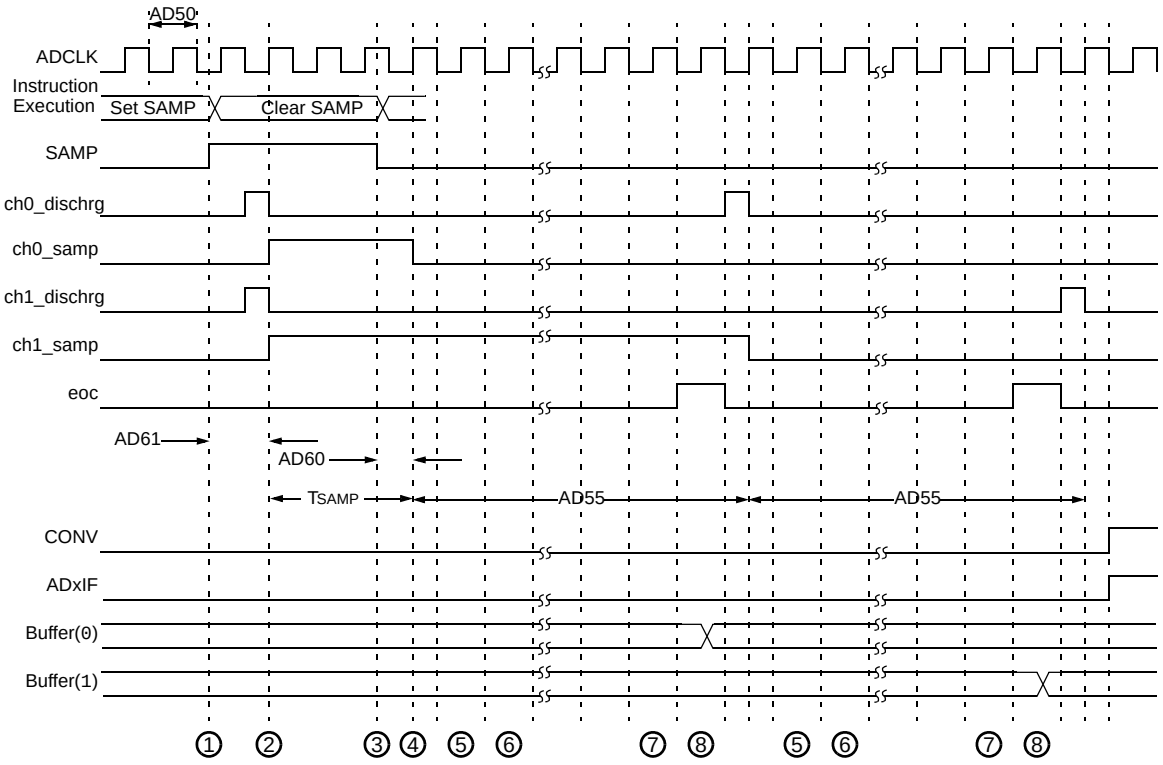
Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns.

4: Assumes 50 pF load on all SPIx pins.

FIGURE 29-18: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 0, SSRC<2:0> = 000)



(1) – Software sets ADxCON. SAMP to start sampling.

(2) – Sampling starts after discharge period. TSAMP is described in **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS61104) of the *"PIC32 Family Reference Manual"*.

(3) – Software clears ADxCON. SAMP to start conversion.

(4) – Sampling ends, conversion sequence starts.

(5) – Convert bit 9.

(6) – Convert bit 8.

(7) – Convert bit 0.

(8) – One TAD for end of conversion.

FIGURE 29-23: EJTAG TIMING CHARACTERISTICS

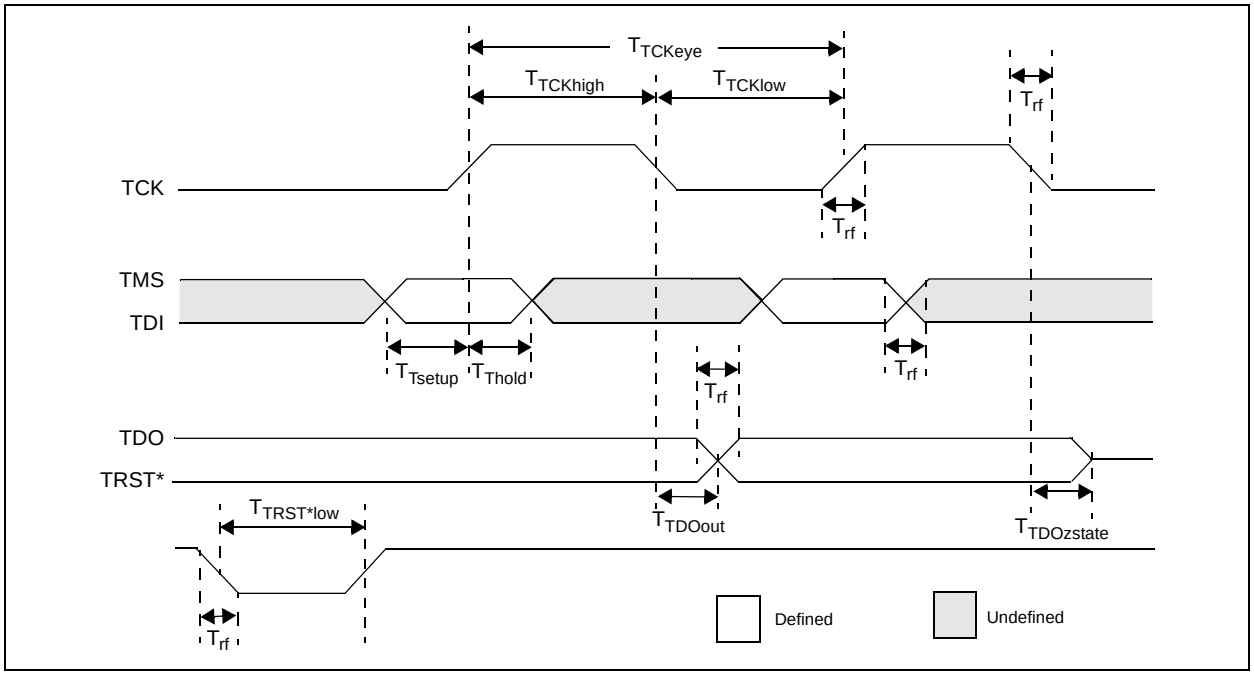


TABLE 29-41: EJTAG TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp			
Param. No.	**Symbol**	**Description(1)**	**Min.**	**Max.**	**Units**	**Conditions**
EJ1	TTCKCYC	TCK Cycle Time	25	—	ns	—
EJ2	TTCKHIGH	TCK High Time	10	—	ns	—
EJ3	TTCKLOW	TCK Low Time	10	—	ns	—
EJ4	TTSETUP	TAP Signals Setup Time Before Rising TCK	5	—	ns	—
EJ5	TTHOLD	TAP Signals Hold Time After Rising TCK	3	—	ns	—
EJ6	TTDOOUT	TDO Output Delay Time from Falling TCK	—	5	ns	—
EJ7	TTDOZSTATE	TDO 3-State Delay Time from Falling TCK	—	5	ns	—
EJ8	TTRSTLOW	TRST Low Time	25	—	ns	—
EJ9	TRF	TAP Signals Rise/Fall Time, All Input and Output	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE A-3: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 29.0 "Electrical Characteristics"	Added the new V-Temp temperature range (-40ºC to +105ºC) to the heading of all specification tables. Updated the Ambient temperature under bias, updated the Voltage on any 5V tolerant pin with respect to VSS when VDD < 2.3V, and added Voltage on VBUS with respect to Vss in Absolute Maximum Ratings. Added the characteristic, DC5a to Operating MIPS vs. Voltage (see Table 29-1). Updated or added the following parameters to the Operating Current (IDD) DC Characteristics: DC20, DC23, DC24c, DC25d, DC26c (see Table 29-5). Added the following parameters to the Idle Current (IIDLE) DC Characteristics: DC30c, DC31c, DC32c, DS33c, DC34c, DC35c, and DC36c (see Table 29-6). Added the following parameters to the Power-down Current (IPD) DC Characteristics: DC40g, DC40h, DC40i, DC41g, DC41h, DC42g, DC42h, DC42i, DC43h, and DC43i (see Table 29-7). Added the Brown-out Reset (BOR) Electrical Characteristics (see Table 29-10). Removed all Conditions from the Program Memory DC Characteristics (see Table 29-11). Removed the AC Characteristics voltage reference table (Table 29-15). Added Note 2 to the PLL Clock Timing Specifications (see Table 29-18). Updated the OC/PWM Module Timing Characteristics (see Figure 29-9). Added parameter IM51 and Note 3 to the I2Cx Bus Data Timing Requirements (Master Mode) (see Table 29-32). Added parameter numbers (AD13, AD14, and AD15) to the ADC Module Specifications (see Table 29-34). Updated the 10-bit ADC Conversion Rate Parameters (see Table 29-35). Updated parameter AD57 (TSAMP) in the Analog-to-Digital Conversion Timing Requirements (see Table 29-36). Updated the Conditions for parameters USB313, USB318, and USB319 in the OTG Electrical Specifications (see Table 29-40).
Section 30.0 "Packaging Information"	Updated the 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] packing diagram.
Product Identification System	Added the new V-Temp (V) temperature information.