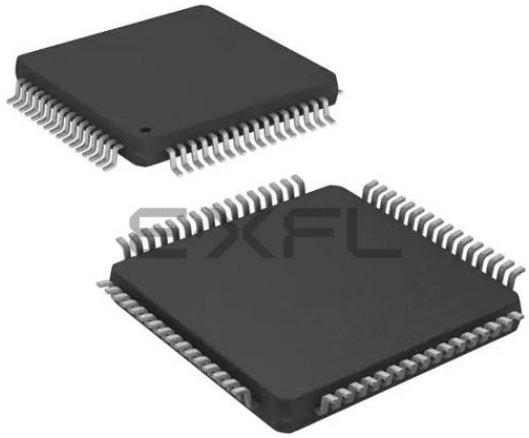
# Microchip Technology - PIC32MX420F032H-40V/PT Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 40MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 53 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TQFP |
| Supplier Device Package | 64-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx420f032h-40v-pt |

**TABLE 3: PIN NAMES: PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F128L, AND PIC32MX360F512L DEVICES (CONTINUED)**

| Pin Number | Full Pin Name |
|---|---|
| K4 | AN8/C1OUT/RB8 |
| K5 | No Connect (NC) |
| K6 | U2CTS/RF12 |
| K7 | AN14/PMALH/PMA1/RB14 |
| K8 | VDD |
| K9 | U1RTS/CN21/RD15 |
| K10 | U1TX/RF3 |
| K11 | U1RX/RF2 |
| L1 | PGEC2/AN6/OCFA/RB6 |
| L2 | VREF-/CVREF-/PMA7/RA9 |

| Pin Number | Full Pin Name |
|---|---|
| L3 | AVSS |
| L4 | AN9/C2OUT/RB9 |
| L5 | AN10/CVREFOUT/PMA13/RB10 |
| L6 | U2RTS/RF13 |
| L7 | AN13/PMA10/RB13 |
| L8 | AN15/OCFB/PMALL/PMA0/CN12/RB15 |
| L9 | CN20/U1CTS/RD14 |
| L10 | U2RX/PMA9/CN17/RF4 |
| L11 | U2TX/PMA8/CN18/RF5 |

## Pin Diagrams (Continued)

**100-Pin TQFP (USB)**

= Pins are up to 5V tolerant

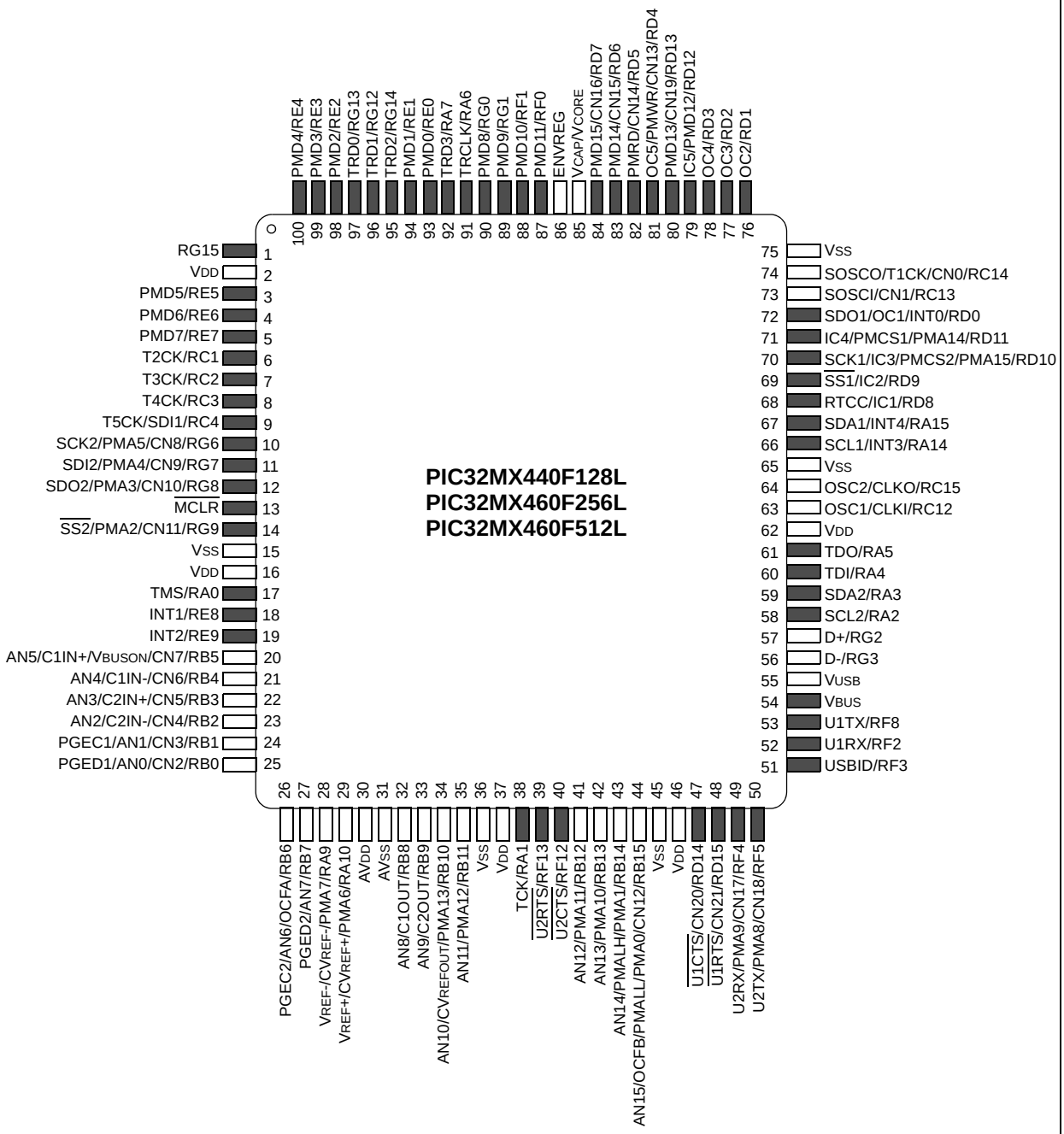

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**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number(1) | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | 64-pin QFN/TQFP | 100-pin TQFP | 121-pin XBGA | | | |
| INT3 | 44 | 66 | E11 | I | ST | External interrupt 3. |
| INT4 | 45 | 67 | E8 | I | ST | External interrupt 4. |
| RA0 | — | 17 | G3 | I/O | ST | PORTA is a bidirectional I/O port. |
| RA1 | — | 38 | J6 | I/O | ST | |
| RA2 | — | 58 | H11 | I/O | ST | |
| RA3 | — | 59 | G10 | I/O | ST | |
| RA4 | — | 60 | G11 | I/O | ST | |
| RA5 | — | 61 | G9 | I/O | ST | |
| RA6 | — | 91 | C5 | I/O | ST | |
| RA7 | — | 92 | B5 | I/O | ST | |
| RA9 | — | 28 | L2 | I/O | ST | |
| RA10 | — | 29 | K3 | I/O | ST | |
| RA14 | — | 66 | E11 | I/O | ST | |
| RA15 | — | 67 | E8 | I/O | ST | |
| RB0 | 16 | 25 | K2 | I/O | ST | PORTB is a bidirectional I/O port. |
| RB1 | 15 | 24 | K1 | I/O | ST | |
| RB2 | 14 | 23 | J2 | I/O | ST | |
| RB3 | 13 | 22 | J1 | I/O | ST | |
| RB4 | 12 | 21 | H2 | I/O | ST | |
| RB5 | 11 | 20 | H1 | I/O | ST | |
| RB6 | 17 | 26 | L1 | I/O | ST | |
| RB7 | 18 | 27 | J3 | I/O | ST | |
| RB8 | 21 | 32 | K4 | I/O | ST | |
| RB9 | 22 | 33 | L4 | I/O | ST | |
| RB10 | 23 | 34 | L5 | I/O | ST | |
| RB11 | 24 | 35 | J5 | I/O | ST | |
| RB12 | 27 | 41 | J7 | I/O | ST | |
| RB13 | 28 | 42 | L7 | I/O | ST | |
| RB14 | 29 | 43 | K7 | I/O | ST | |
| RB15 | 30 | 44 | L8 | I/O | ST | |
| RC1 | — | 6 | D1 | I/O | ST | PORTC is a bidirectional I/O port. |
| RC2 | — | 7 | E4 | I/O | ST | |
| RC3 | — | 8 | E2 | I/O | ST | |
| RC4 | — | 9 | E1 | I/O | ST | |
| RC12 | 39 | 63 | F9 | I/O | ST | |
| RC13 | 47 | 73 | C10 | I/O | ST | |
| RC14 | 48 | 74 | B11 | I/O | ST | |
| RC15 | 40 | 64 | F11 | I/O | ST | |

**Legend:** CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer
Analog = Analog input
O = Output
P = Power
I = Input

**Note 1:** Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

# 2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MICROCONTROLLERS

**Note 1:** This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

## 2.1 Basic Connection Requirements

Getting started with the PIC32MX3XX/4XX family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins (regardless if ADC module is not used)
  (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP/VCORE
  (see **Section 2.3 "Capacitor on Internal Voltage Regulator (VCAP/VCORE)"**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used
  (see **Section 2.8 "External Oscillator Pins"**)

Additionally, the following pins may be required:

- VREF+/VREF- pins used when external voltage reference for ADC module is implemented

**Note:** The AVDD and AVSS pins must be connected independent of ADC use and ADC voltage reference source.

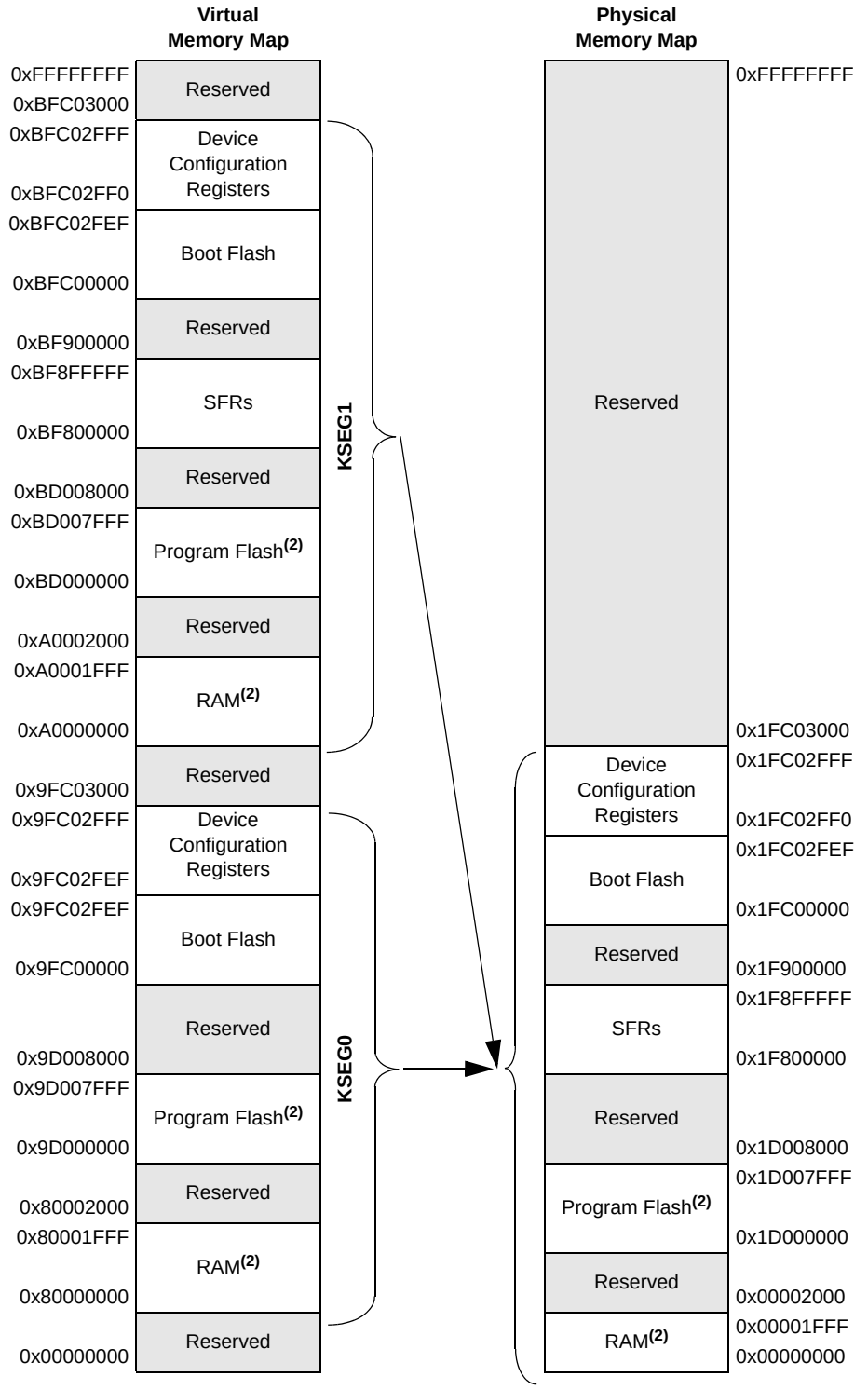
## 2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

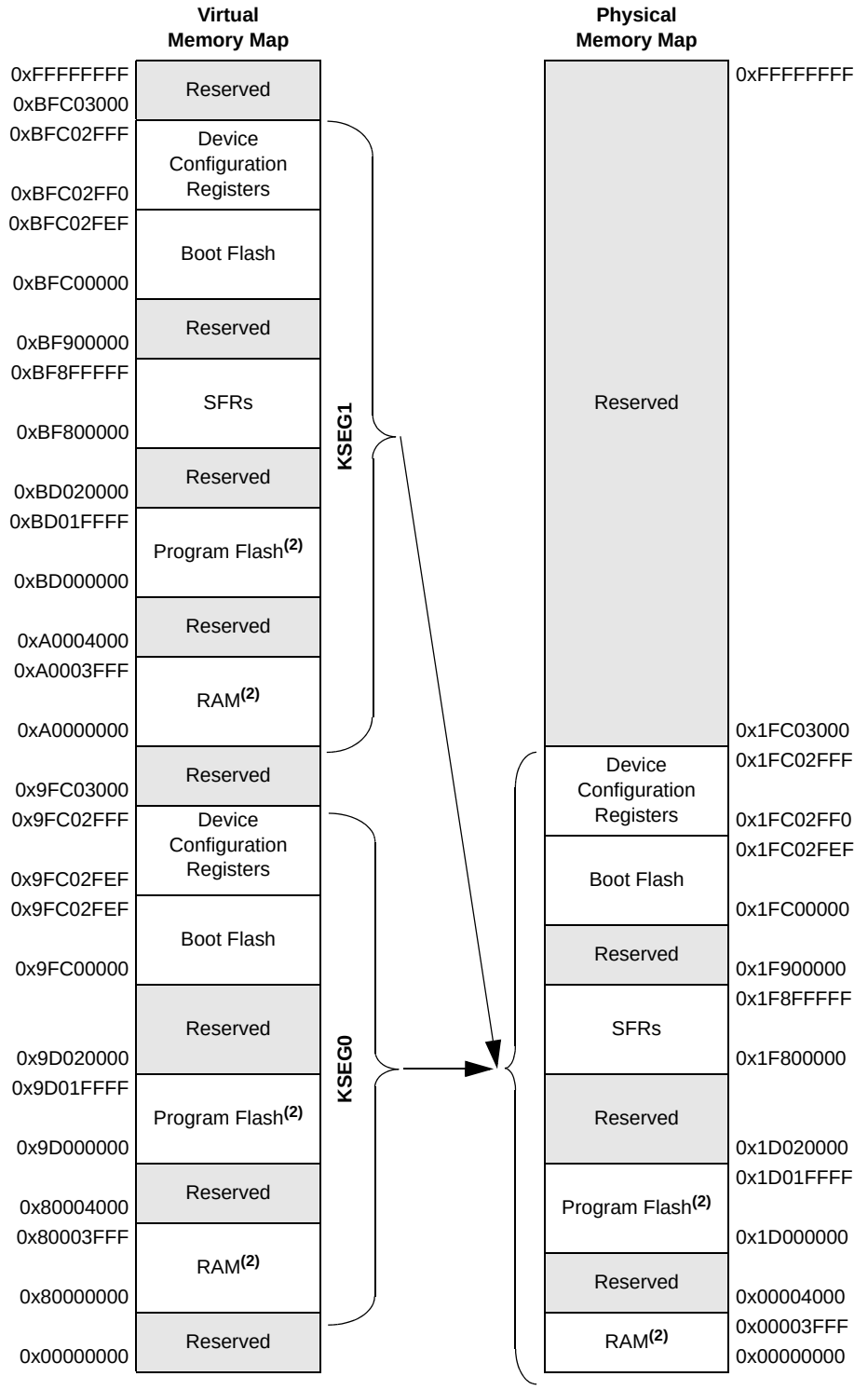
**FIGURE 4-1: MEMORY MAP ON RESET FOR PIC32MX320F032H AND PIC32MX420F032H DEVICES(1)**




**Note 1:** Memory areas are not shown to scale.

**2:** The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS61115)) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

**FIGURE 4-3: MEMORY MAP ON RESET FOR PIC32MX320F128H AND PIC32MX320F128L DEVICES(1)**




**Note 1:** Memory areas are not shown to scale.

**2:** The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS61115)) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

**TABLE 4-1: BUS MATRIX REGISTERS MAP**

| Virtual Address (BF88_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 2000 | BMX CON(1) | 31:16 | — | — | — | — | — | BMXCHEDMA | — | — | — | — | — | BMXERRIXI | BMXERRICD | BMXERRDMA | BMXERRDS | BMXERRIS | 001F |
| | | 15:0 | — | — | — | — | — | — | — | — | — | BMXWSDRM | — | — | — | BMXARB<2:0> | | | 0042 |
| 2010 | BMX DKPBA(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BMXDKPBA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 2020 | BMX DUDBA(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BMXDUDBA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 2030 | BMX DUPBA(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BMXDUPBA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 2040 | BMX DRMSZ | 31:16 | BMXDRMSZ<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 2050 | BMX PUPBA(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | BMXPUPBA<19:16> | | | | 0000 |
| | | 15:0 | BMXPUPBA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 2060 | BMX PFMSZ | 31:16 | BMXPFMSZ<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 2070 | BMX BOOTSZ | 31:16 | BMXBOOTSZ<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 3000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**TABLE 4-5: INTERRUPT REGISTERS MAP FOR PIC32MX440F128H, PIC32MX440F256H AND PIC32MX440F512H DEVICES ONLY(1)**

| Virtual Address (BF88_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 1000 | INTCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SS0 | 0000 |
| | | 15:0 | — | — | — | MVEC | — | TPC<2:0> | | | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 0000 |
| 1010 | INTSTAT(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | SRIPL<2:0> | | | — | — | VEC<5:0> | | | | | | 0000 |
| 1020 | IPTMR | 31:16 | IPTMR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 1030 | IFS0 | 31:16 | I2C1MIF | I2C1SIF | I2C1BIF | U1TXIF | U1RXIF | U1EIF | — | — | — | OC5IF | IC5IF | T5IF | INT4IF | OC4IF | IC4IF | T4IF | 0000 |
| | | 15:0 | INT3IF | OC3IF | IC3IF | T3IF | INT2IF | OC2IF | IC2IF | T2IF | INT1IF | OC1IF | IC1IF | T1IF | INT0IF | CS1IF | CS0IF | CTIF | 0000 |
| 1040 | IFS1 | 31:16 | — | — | — | — | — | — | USBIF | FCEIF | — | — | — | — | DMA3IF | DMA2IF | DMA1IF | DMA0IF | 0000 |
| | | 15:0 | RTCCIF | FSCMIF | I2C2MIF | I2C2SIF | I2C2BIF | U2TXIF | U2RXIF | U2EIF | SPI2RXIF | SPI2TXIF | SPI2EIF | CMP2IF | CMP1IF | PMPIF | AD1IF | CNIF | 0000 |
| 1060 | IEC0 | 31:16 | I2C1MIE | I2C1SIE | I2C1BIE | U1TXIE | U1RXIE | U1EIE | — | — | — | OC5IE | IC5IE | T5IE | INT4IE | OC4IE | IC4IE | T4IE | 0000 |
| | | 15:0 | INT3IE | OC3IE | IC3IE | T3IE | INT2IE | OC2IE | IC2IE | T2IE | INT1IE | OC1IE | IC1IE | T1IE | INT0IE | CS1IE | CS0IE | CTIE | 0000 |
| 1070 | IEC1 | 31:16 | — | — | — | — | — | — | USBIE | FCEIE | — | — | — | — | DMA3IE | DMA2IE | DMA1IE | DMA0IE | 0000 |
| | | 15:0 | RTCCIE | FSCMIE | I2C2MIE | I2C2SIE | I2C2BIE | U2TXIE | U2RXIE | U2EIE | SPI2RXIE | SPI2TXIE | SPI2EIE | CMP2IE | CMP1IE | PMPIE | AD1IE | CNIE | 0000 |
| 1090 | IPC0 | 31:16 | — | — | — | INT0IP<2:0> | | | INT0IS<1:0> | | — | — | — | CS1IP<2:0> | | | CS1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CS0IP<2:0> | | | CS0IS<1:0> | | — | — | — | CTIP<2:0> | | | CTIS<1:0> | | 0000 |
| 10A0 | IPC1 | 31:16 | — | — | — | INT1IP<2:0> | | | INT1IS<1:0> | | — | — | — | OC1IP<2:0> | | | OC1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC1IP<2:0> | | | IC1IS<1:0> | | — | — | — | T1IP<2:0> | | | T1IS<1:0> | | 0000 |
| 10B0 | IPC2 | 31:16 | — | — | — | INT2IP<2:0> | | | INT2IS<1:0> | | — | — | — | OC2IP<2:0> | | | OC2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC2IP<2:0> | | | IC2IS<1:0> | | — | — | — | T2IP<2:0> | | | T2IS<1:0> | | 0000 |
| 10C0 | IPC3 | 31:16 | — | — | — | INT3IP<2:0> | | | INT3IS<1:0> | | — | — | — | OC3IP<2:0> | | | OC3IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC3IP<2:0> | | | IC3IS<1:0> | | — | — | — | T3IP<2:0> | | | T3IS<1:0> | | 0000 |
| 10D0 | IPC4 | 31:16 | — | — | — | INT4IP<2:0> | | | INT4IS<1:0> | | — | — | — | OC4IP<2:0> | | | OC4IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC4IP<2:0> | | | IC4IS<1:0> | | — | — | — | T4IP<2:0> | | | T4IS<1:0> | | 0000 |
| 10E0 | IPC5 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | OC5IP<2:0> | | | OC5IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC5IP<2:0> | | | IC5IS<1:0> | | — | — | — | T5IP<2:0> | | | T5IS<1:0> | | 0000 |
| 10F0 | IPC6 | 31:16 | — | — | — | AD1IP<2:0> | | | AD1IS<1:0> | | — | — | — | CNIP<2:0> | | | CNIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | I2C1IP<2:0> | | | I2C1IS<1:0> | | — | — | — | U1IP<2:0> | | | U1IS<1:0> | | 0000 |
| 1100 | IPC7 | 31:16 | — | — | — | SPI2IP<2:0> | | | SPI2IS<1:0> | | — | — | — | CMP2IP<2:0> | | | CMP2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CMP1IP<2:0> | | | CMP1IS<1:0> | | — | — | — | PMPIP<2:0> | | | PMPIS<1:0> | | 0000 |
| 1110 | IPC8 | 31:16 | — | — | — | RTCCIP<2:0> | | | RTCCIS<1:0> | | — | — | — | FSCMIP<2:0> | | | FSCMIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | I2C2IP<2:0> | | | I2C2IS<1:0> | | — | — | — | U2IP<2:0> | | | U2IS<1:0> | | 0000 |
| 1120 | IPC9 | 31:16 | — | — | — | DMA3IP<2:0> | | | DMA3IS<1:0> | | — | — | — | DMA2IP<2:0> | | | DMA2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | DMA1IP<2:0> | | | DMA1IS<1:0> | | — | — | — | DMA0IP<2:0> | | | DMA0IS<1:0> | | 0000 |
| 1140 | IPC11 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | USBIP<2:0> | | | USBIS<1:0> | | — | — | — | FCEIP<2:0> | | | FCEIS<1:0> | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** This register does not have associated CLR, SET, and INV registers.

**TABLE 4-10: I2C1-2 REGISTERS MAP(1)**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 5000 | I2C1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | SCLREL | STRICT | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 1000 |
| 5010 | I2C1STAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D/A | P | S | R/W | RBF | TBF | 0000 |
| 5020 | I2C1ADD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| | | | — | — | — | — | — | — | ADD<9:0> | | | | | | | | | | 0000 |
| 5030 | I2C1MSK | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | MSK<9:0> | | | | | | | | | | 0000 |
| 5040 | I2C1BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | I2C1BRG<11:0> | | | | | | | | | | | | 0000 |
| 5050 | I2C1TRN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | I2CT1DATA<7:0> | | | | | | | | 0000 |
| 5260 | I2C1RCV | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | I2CR1DATA<7:0> | | | | | | | | 0000 |
| 5200 | I2C2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | SCLREL | STRICT | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 1000 |
| 5210 | I2C2STAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D/A | P | S | R/W | RBF | TBF | 0000 |
| 5220 | I2C2ADD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | ADD<9:0> | | | | | | | | | | 0000 |
| 5230 | I2C2MSK | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | MSK<9:0> | | | | | | | | | | 0000 |
| 5240 | I2C2BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | I2C2BRG<11:0> | | | | | | | | | | | | 0000 |
| 5250 | I2C2TRN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | I2CT2DATA<7:0> | | | | | | | | 0000 |
| 5260 | I2C2RCV | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | I2CR2DATA<7:0> | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table except I2CxRCV have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**TABLE 4-31: PORTF REGISTERS MAP FOR PIC32MX320F032H, PIC32MX320F064H, PIC32MX320F128H, PIC32MX340F128H, PIC32MX340F256H AND PIC32MX340F512H DEVICES ONLY(1)**

| Virtual Address (BF88_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6140 | TRISF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | TRISF6 | TRISF5 | TRISF4 | TRISF3 | TRISF2 | TRISF1 | TRISF0 | 07FF |
| 6150 | PORTF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | RF6 | RF5 | RF4 | RF3 | RF2 | RF1 | RF0 | xxxx |
| 6160 | LATF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | LATF6 | LATF5 | LATF4 | LATF3 | LATF2 | LATF1 | LATF0 | xxxx |
| 6170 | ODCF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | ODCF6 | ODCF5 | ODCF4 | ODCF3 | ODCF2 | ODCF1 | ODCF0 | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**TABLE 4-32: PORTF REGISTERS MAP FOR PIC32MX420F032H, PIC32MX440F128H AND PIC2MX440F256H DEVICES ONLY(1)**

| Virtual Address (BF88_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6140 | TRISF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | TRISF5 | TRISF4 | TRISF3 | TRISF2 | TRISF1 | TRISF0 | 03FF |
| 6150 | PORTF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | RF5 | RF4 | RF3 | RF2 | RF1 | RF0 | xxxx |
| 6160 | LATF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | LATF5 | LATF4 | LATF3 | LATF2 | LATF1 | LATF0 | xxxx |
| 6170 | ODCF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | ODCF5 | ODCF4 | ODCF3 | ODCF2 | ODCF1 | ODCF0 | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**NOTES:**

## 9.0 PREFETCH CACHE

**Note 1:** This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 4. "Prefetch Cache"** (DS61119) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

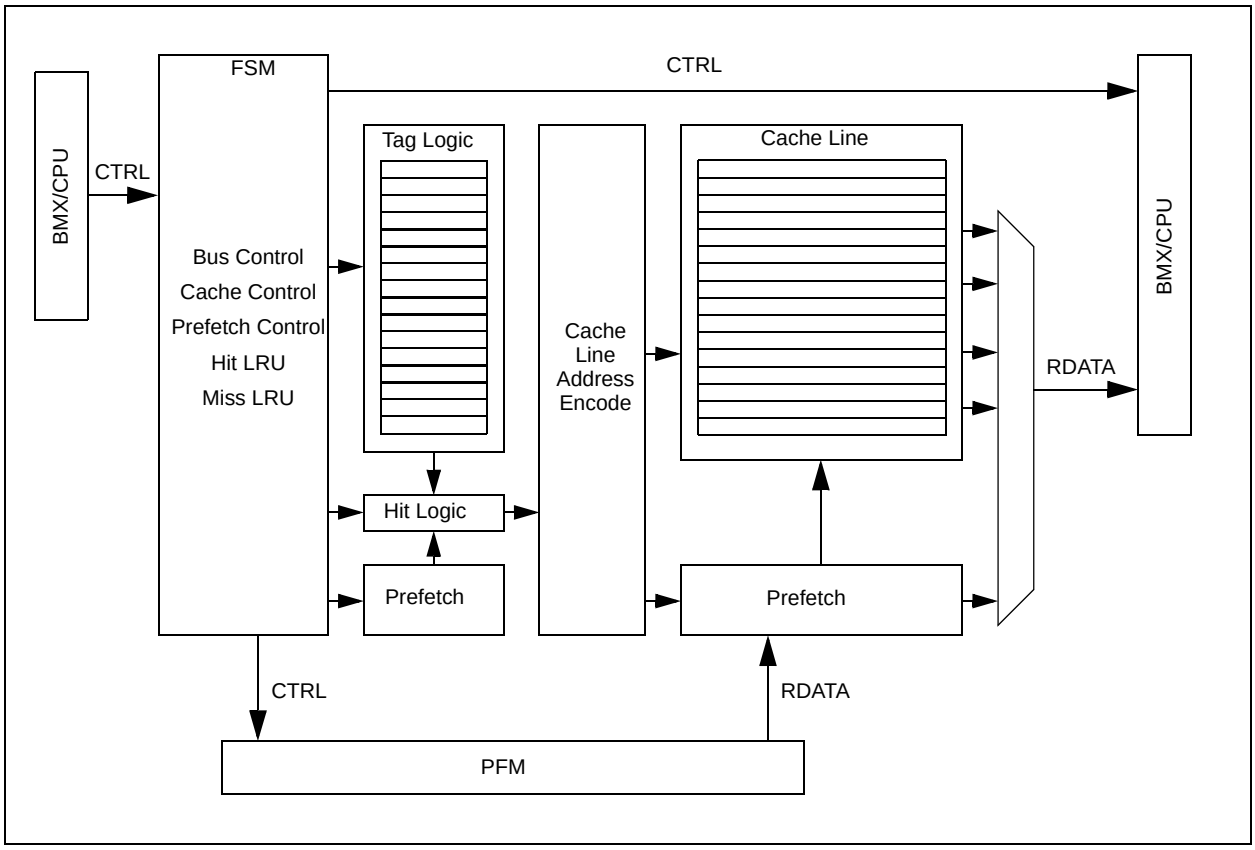
**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

Prefetch cache increases performance for applications executing out of the cacheable program Flash memory regions by implementing instruction caching, constant data caching and instruction prefetching.

### 9.1 Features

- 16 Fully Associative Lockable Cache Lines
- 16-byte Cache Lines
- Up to four Cache Lines Allocated to Data
- Two Cache Lines with Address Mask to hold repeated instructions
- Pseudo LRU replacement policy
- All Cache Lines are software writable
- 16-byte parallel memory fetch
- Predictive Instruction Prefetch

**FIGURE 9-1: PREFETCH MODULE BLOCK DIAGRAM**



## 26.0 SPECIAL FEATURES

**Note:** This data sheet summarizes the features of the PIC32MX3XX/4XX family family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog Timer and Power-up Timer"** (DS61114), **Section 32. "Configuration"** (DS61124) and **Section 33. "Programming and Diagnostics"** (DS61129) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX3XX/4XX devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. These are:

- Flexible Device Configuration
- Watchdog Timer
- JTAG Interface
- In-Circuit Serial Programming™ (ICSP™)

### 26.1 Configuration Bits

The Configuration bits can be programmed to select various device configurations.

**REGISTER 26-1: DEVCFG0: DEVICE CONFIGURATION WORD 0**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | r-0 | r-1 | r-1 | R/P | r-1 | r-1 | r-1 | R/P |
| | — | — | — | CP | — | — | — | BWP |
| 23:16 | r-1 | r-1 | r-1 | r-1 | R/P | R/P | R/P | R/P |
| | — | — | — | — | PWP<7:4> | | | |
| 15:8 | R/P | R/P | R/P | R/P | r-1 | r-1 | r-1 | r-1 |
| | PWP<3:0> | | | | — | — | — | — |
| 7:0 | r-1 | r-1 | r-1 | r-1 | R/P | r-1 | R/P | R/P |
| | — | — | — | — | ICESEL | — | DEBUG<1:0> | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | P = Programmable bit | r = Reserved bit |
| U = Unimplemented bit | -n = Bit Value at POR: ('0', '1', x = Unknown) | | |

bit 31 **Reserved:** Write '0'

bit 30-29 **Reserved:** Write '1'

bit 28 **CP:** Code-Protect bit

Prevents boot and program Flash memory from being read or modified by an external programming device.
1 = Protection disabled
0 = Protection enabled

bit 27-25 **Reserved:** Write '1'

bit 24 **BWP:** Boot Flash Write-Protect bit

Prevents boot Flash memory from being modified during code execution.
1 = Boot Flash is writable
0 = Boot Flash is not writable

bit 23-20 **Reserved:** Write '1'

**TABLE 29-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Typical(3)** | **Max.** | **Units** | **Conditions** | | | |
| **Operating Current (IDD)(1,2)** | | | | | | | |
| DC20 | 8.5 | 13 | mA | Code executing from Flash | -40ºC, +25ºC, +85ºC | — | 4 MHz |
| | 9 | 15 | | | +105ºC | | |
| DC20c | 4.0 | — | mA | Code executing from SRAM | — | | |
| DC21 | 23.5 | 32 | mA | Code executing from Flash | — | — | 20 MHz **(Note 4)** |
| DC21c | 16.4 | — | mA | Code executing from SRAM | | | |
| DC22 | 48 | 61 | mA | Code executing from Flash | — | — | 60 MHz **(Note 4)** |
| DC22c | 45 | — | mA | Code executing from SRAM | | | |
| DC23 | 55 | 75 | mA | Code executing from Flash | -40ºC, +25ºC, +85ºC | 2.3V | 80 MHz |
| | 60 | 100 | | | +105ºC | | |
| DC23c | 55 | — | mA | Code executing from SRAM | — | — | |
| DC24 | — | 100 | µA | — | -40°C | 2.3V | LPRC (31 kHz) **(Note 4)** |
| DC24a | — | 130 | µA | — | +25°C | | |
| DC24b | — | 670 | µA | — | +85°C | | |
| DC24c | — | 850 | µA | — | +105ºC | | |
| DC25 | 94 | — | µA | — | -40°C | 3.3V | |
| DC25a | 125 | — | µA | — | +25°C | | |
| DC25b | 302 | — | µA | — | +85°C | | |
| DC25d | 400 | — | µA | — | +105ºC | | |
| DC25c | 71 | — | µA | Code executing from SRAM | — | — | |
| DC26 | — | 110 | µA | — | -40°C | 3.6V | |
| DC26a | — | 180 | µA | — | +25°C | | |
| DC26b | — | 700 | µA | — | +85°C | | |
| DC26c | — | 900 | µA | — | +105ºC | | |

**Note 1:** A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type as well as temperature can have an impact on the current consumption.

**2:** The test conditions for IDD measurements are as follows: Oscillator mode = EC+PLL with OSC1 driven by external square wave from rail to rail and PBCLK divisor = 1:8. CPU, Program Flash and SRAM data memory are operational, Program Flash memory Wait states = 7, program cache and prefetch are disabled and SRAM data memory Wait states = 1. All peripheral modules are disabled (ON bit = 0). WDT and FSCM are disabled. All I/O pins are configured as inputs and pulled to VSS. MCLR = VDD.

**3:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

**4:** This parameter is characterized, but not tested in manufacturing.

**TABLE 29-11: DC CHARACTERISTICS: PROGRAM MEMORY(3)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| | | **Program Flash Memory** | | | | | |
| D130 | EP | Cell Endurance | 1000 | — | — | E/W | — |
| D131 | VPR | VDD for Read | VMIN | — | 3.6 | V | — |
| D132 | VPEW | VDD for Erase or Write | 3.0 | — | 3.6 | V | — |
| D134 | TRETD | Characteristic Retention | 20 | — | — | Year | — |
| D135 | IDDP | Supply Current during Programming | — | 10 | — | mA | — |
| | TWW | Word Write Cycle Time | 20 | — | 40 | µs | — |
| D136 | TRW | Row Write Cycle Time(2) (128 words per row) | 3 | 4.5 | — | ms | — |
| D137 | TPE | Page Erase Cycle Time | 20 | — | — | ms | — |
| | TCE | Chip Erase Cycle Time | 80 | — | — | ms | — |
| D138 | LVDstartup | Flash LVD Delay | — | — | 6 | µs | — |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

**2:** The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

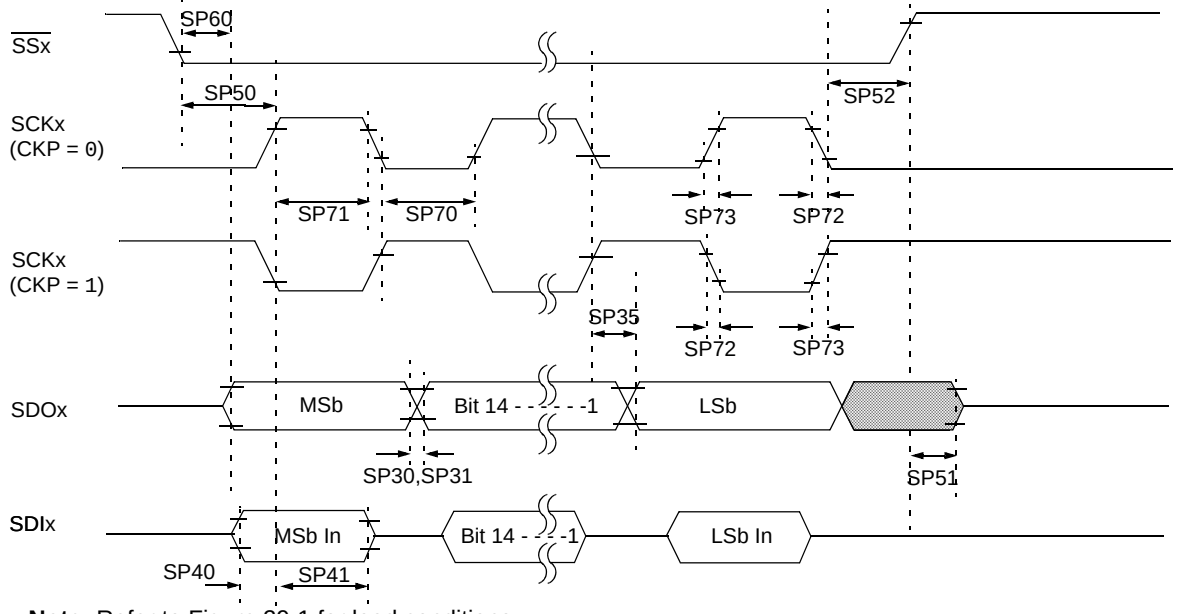
**3:** Refer to the "*PIC32MX Flash Programming Specification*" (DS61145) for operating conditions during programming and erase cycles.

**TABLE 29-12: PROGRAM FLASH MEMORY WAIT STATE CHARACTERISTICS**

| DC CHARACTERISTICS | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+105°C for V-Temp | | |
|---|---|---|---|
| **Required Flash wait states** | **SYSCLK** | **Units** | **Comments** |
| 0 Wait State | 0 to 30 | MHz | — |
| 1 Wait State | 31 to 60 | | |
| 2 Wait States | 61 to 80 | | |

**Note 1:** 40 MHz maximum for PIC32MX320F032H and PIC32MX420F032H devices.

**FIGURE 29-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 29-1 for load conditions.

**TABLE 29-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | **Standard Operating Conditions: 2.3V to 3.6V** (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | TscL | SCKx Input Low Time(3) | Tsck/2 | — | — | ns | — |
| SP71 | TscH | SCKx Input High Time(3) | Tsck/2 | — | — | ns | — |
| SP72 | TscF | SCKx Input Fall Time | — | 5 | 10 | ns | — |
| SP73 | TscR | SCKx Input Rise Time | — | 5 | 10 | ns | — |
| SP30 | TdoF | SDOx Data Output Fall Time(4) | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time(4) | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 20 | ns | VDD > 2.7V |
| | | | — | — | 30 | ns | VDD < 2.7V |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓to SCKx ↓or SCKx ↑ Input | 175 | — | — | ns | — |
| SP51 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output High-Impedance(4) | 5 | — | 25 | ns | — |
| SP52 | TscH2ssH TscL2ssH | $\overline{SSx}$ ↑ after SCKx Edge | Tsck + 20 | — | — | ns | — |
| SP60 | TssL2doV | $\overline{SDOx}$ Data Output Valid after $\overline{SSx}$ Edge | — | — | 25 | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 40 ns.

**4:** Assumes 50 pF load on all SPIx pins.

**NOTES:**

## Revision H (May 2011)

The revision includes the following global update:

- All references to VDDCORE/VCAP have been changed to: VCORE/VCAP
- Added references to the new V-Temp temperature range: -40ºC to +105ºC

This revision also includes minor typographical and formatting changes throughout the data sheet text. Major updates are referenced by their respective section in the following table.

**TABLE A-3: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **Section 1.0 “Device Overview”** | Updated the VBUS description in **Table 1-1: “Pinout I/O Descriptions”**. |
| **Section 4.0 “Memory Organization”** | Added Note 2 and changed the RIPL<2:0> bits to SRIPL<2:0> in the Interrupt Register Map tables (see Table 4-2 through Table 4-6.<br>Added Note 2 to the Timer1-5 Register Map (see Table 4-7).<br>Updated the All Resets value for I2C1CON<15:0> and I2C2CON<15:0> in the I2C1 and I2C2 Register Map (see Table 4-10).<br>Updated the All Resets value for SPI1STAT<15:0> and SPI2STAT<15:0> in the SPI1 and SPI2 Register Map (see Table 4-12).<br>Updated the All Resets value for CM1CON<15:0> and CM2CON<15:0> in the Comparator Register Map (see Table 4-17).<br>Renamed the RCDIV<2:0> bits to FRCDIV<2:0> and the LOCK bit to SLOCK in the OSCCON register, and added Note 3 and the SYSKEYregister to the System Control Registers Map (see Table 4-20).<br>Updated the All Resets value for the PMSTAT register in the Parallel Master Port Register Map (see Table 4-37).<br>Updated the All Resets value for CHECON<15:0> and CHETAG<15:0> in the Prefetch Register Map (see Table 4-39).<br>Renamed FUPLLEN, FUPLLIDIV, and FPLLMULT in the DEVCFG2 register to: UPLLEN, UPLLIDIV, and FPLLMUL, respectively in the Device Configuration Word Summary (see Table 4-41).<br>Added Notes 1 through 4 to the USB Register Map (see Table 4-43). |
| **Section 5.0 “Flash Program Memory”** | Added a note on Flash LVD Delay and Example 5-1. |
| **Section 8.0 “Oscillator Configuration”** | Updated the PIC32MX3XX/4XX Family Clock Diagram (see Figure 8-1). |
| **Section 11.0 “USB On-The-Go (OTG)”** | Updated the PIC32MX3XX/4XX Family USB Interface Diagram (see Figure 11-1). |
| **Section 16.0 “Output Compare”** | Updated the Output Compare Module Block Diagram (see Figure 16-1). |
| **Section 22.0 “10-bit Analog-to-Digital Converter (ADC)”** | Updated the ADC Conversion Clock Period Block Diagram (see Figure 22-2). |
| **Section 26.0 “Special Features”** | Renamed FUPLLEN, FUPLLIDIV, and FPLLMULT in the DEVCFG2 register to: UPLLEN, UPLLIDIV, and FPLLMUL, respectively (see Register 26-3). |

**TABLE A-3: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **Section 29.0 "Electrical Characteristics"** | Added the new V-Temp temperature range (-40ºC to +105ºC) to the heading of all specification tables.<br><br>Updated the Ambient temperature under bias, updated the Voltage on any 5V tolerant pin with respect to VSS when VDD < 2.3V, and added Voltage on VBUS with respect to Vss in Absolute Maximum Ratings.<br><br>Added the characteristic, DC5a to Operating MIPS vs. Voltage (see Table 29-1).<br><br>Updated or added the following parameters to the Operating Current (IDD) DC Characteristics: DC20, DC23, DC24c, DC25d, DC26c (see Table 29-5).<br><br>Added the following parameters to the Idle Current (IIDLE) DC Characteristics: DC30c, DC31c, DC32c, DS33c, DC34c, DC35c, and DC36c (see Table 29-6).<br><br>Added the following parameters to the Power-down Current (IPD) DC Characteristics: DC40g, DC40h, DC40i, DC41g, DC41h, DC42g, DC42h, DC42i, DC43h, and DC43i (see Table 29-7).<br><br>Added the Brown-out Reset (BOR) Electrical Characteristics (see Table 29-10).<br><br>Removed all Conditions from the Program Memory DC Characteristics (see Table 29-11).<br><br>Removed the AC Characteristics voltage reference table (Table 29-15).<br><br>Added Note 2 to the PLL Clock Timing Specifications (see Table 29-18).<br><br>Updated the OC/PWM Module Timing Characteristics (see Figure 29-9).<br><br>Added parameter IM51 and Note 3 to the I2Cx Bus Data Timing Requirements (Master Mode) (see Table 29-32).<br><br>Added parameter numbers (AD13, AD14, and AD15) to the ADC Module Specifications (see Table 29-34).<br><br>Updated the 10-bit ADC Conversion Rate Parameters (see Table 29-35).<br><br>Updated parameter AD57 (TSAMP) in the Analog-to-Digital Conversion Timing Requirements (see Table 29-36).<br><br>Updated the Conditions for parameters USB313, USB318, and USB319 in the OTG Electrical Specifications (see Table 29-40). |
| **Section 30.0 "Packaging Information"** | Updated the 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] packing diagram. |
| **Product Identification System** | Added the new V-Temp (V) temperature information. |