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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx440f128h-80i-mr

Pin Diagrams (Continued)

121-Pin XBGA⁽¹⁾

● = Pins are up to 5V tolerant

PIC32MX440F128L
PIC32MX460F256L
PIC32MX460F512L

	1	2	3	4	5	6	7	8	9	10	11
A	● RE4	● RE3	● RG13	● RE0	● RG0	● RF1	○ ENVREG	○ Vss	● RD12	● RD2	● RD1
B	● NC	● RG15	● RE2	● RE1	● RA7	● RF0	○ Vcore/ VCAP	● RD5	● RD3	○ Vss	○ RC14
C	● RE6	○ VDD	● RG12	● RG14	● RA6	● NC	● RD7	● RD4	○ VDD	○ RC13	● RD11
D	● RC1	● RE7	● RE5	○ Vss	○ Vss	● NC	● RD6	● RD13	● RD0	● NC	● RD10
E	● RC4	● RC3	● RG6	● RC2	○ VDD	● RG1	○ Vss	● RA15	● RD8	● RD9	● RA14
F	● MCLR	● RG8	● RG9	● RG7	○ Vss	● NC	● NC	○ VDD	○ RC12	○ Vss	○ RC15
G	● RE8	● RE9	● RA0	● NC	○ VDD	○ Vss	○ Vss	● NC	● RA5	● RA3	● RA4
H	○ RB5	○ RB4	○ Vss	○ VDD	● NC	○ VDD	● NC	● VBUS	○ VUSB	● RG2	● RA2
J	○ RB3	○ RB2	○ RB7	○ AVDD	○ RB11	○ RA1	○ RB12	● NC	● NC	● RF8	○ RG3
K	○ RB1	○ RB0	○ RA10	○ RB8	● NC	● RF12	○ RB14	○ VDD	● RD15	● RF3	● RF2
L	○ RB6	○ RA9	○ AVss	○ RB9	○ RB10	● RF13	○ RB13	○ RB15	● RD14	● RF4	● RF5

Note 1: Refer to Table 4 for full pin names.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number ⁽¹⁾			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
TMS	23	17	G3	I	ST	JTAG Test mode select pin.
TCK	27	38	J6	I	ST	JTAG test clock input pin.
TDI	28	60	G11	I	ST	JTAG test data input pin.
TDO	24	61	G9	O	—	JTAG test data output pin.
RTCC	42	68	E9	O	—	Real-Time Clock Alarm Output.
CVREF-	15	28	L2	I	Analog	Comparator Voltage Reference (low).
CVREF+	16	29	K3	I	Analog	Comparator Voltage Reference (high).
CVREFOUT	23	34	L5	O	Analog	Comparator Voltage Reference Output.
C1IN-	12	21	H2	I	Analog	Comparator 1 Negative Input.
C1IN+	11	20	H1	I	Analog	Comparator 1 Positive Input.
C1OUT	21	32	K4	O	—	Comparator 1 Output.
C2IN-	14	23	J2	I	Analog	Comparator 2 Negative Input.
C2IN+	13	22	J1	I	Analog	Comparator 2 Positive Input.
C2OUT	22	33	L4	O	—	Comparator 2 Output.
PMA0	30	44	L8	I/O	TTL/ST	Parallel Master Port Address Bit 0 Input (Buffered Slave modes) and Output (Master modes).
PMA1	29	43	K7	I/O	TTL/ST	Parallel Master Port Address Bit 1 Input (Buffered Slave modes) and Output (Master modes).
PMA2	8	14	F3	O	—	Parallel Master Port Address (De-multiplexed Master Modes).
PMA3	6	12	F2	O	—	
PMA4	5	11	F4	O	—	
PMA5	4	10	E3	O	—	
PMA6	16	29	K3	O	—	
PMA7	22	28	L2	O	—	
PMA8	32	50	L11	O	—	
PMA9	31	49	L10	O	—	
PMA10	28	42	L7	O	—	
PMA11	27	41	J7	O	—	
PMA12	24	35	J5	O	—	
PMA13	23	34	L5	O	—	
PMA14	45	71	C11	O	—	
PMA15	44	70	D11	O	—	
PMCS1	45	71	C11	O	—	Parallel Master Port Chip Select 1 Strobe.
PMCS2	44	70	D11	O	—	Parallel Master Port Chip Select 2 Strobe.

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer

Analog = Analog input P = Power
O = Output I = Input

Note 1: Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

2.11 Referenced Sources

This device data sheet is based on the following individual chapters of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the PIC32MX460F512L product page on the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features, and other documentation, the resulting page provides links to the related family reference manual sections.

- **Section 1. "Introduction"** (DS61127)
- **Section 2. "CPU"** (DS61113)
- **Section 3. "Memory Organization"** (DS61115)
- **Section 4. "Prefetch Cache"** (DS61119)
- **Section 5. "Flash Program Memory"** (DS61121)
- **Section 6. "Oscillator Configuration"** (DS61112)
- **Section 7. "Resets"** (DS61118)
- **Section 8. "Interrupt Controller"** (DS61108)
- **Section 9. "Watchdog Timer and Power-up Timer"** (DS61114)
- **Section 10. "Power-Saving Features"** (DS61130)
- **Section 12. "I/O Ports"** (DS61120)
- **Section 13. "Parallel Master Port (PMP)"** (DS61128)
- **Section 14. "Timers"** (DS61105)
- **Section 15. "Input Capture"** (DS61122)
- **Section 16. "Output Compare"** (DS61111)
- **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS61104)
- **Section 19. "Comparator"** (DS61110)
- **Section 20. "Comparator Voltage Reference (CVREF)"** (DS61109)
- **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS61107)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS61106)
- **Section 24. "Inter-Integrated Circuit™ (I²C™)"** (DS61116)
- **Section 27. "USB On-The-Go (OTG)"** (DS61126)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS61125)
- **Section 31. "Direct Memory Access (DMA) Controller"** (DS61117)
- **Section 32. "Configuration"** (DS61124)
- **Section 33. "Programming and Diagnostics"** (DS61129)

3.3 Power Management

The MIPS32® M4K® Processor Core offers a number of power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or halting the clocks, which reduces system power consumption during idle periods.

3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking power-down mode is through execution of the WAIT instruction. For more information on power management, see **Section 25.0 “Power-Saving Features”**.

3.3.2 LOCAL CLOCK GATING

The majority of the power consumed by the PIC32MX3XX/4XX family core is in the clock tree and clocking registers. The PIC32MX family uses extensive use of local gated-clocks to reduce this dynamic power consumption.

3.4 EJTAG Debug Support

The MIPS32® M4K® Processor Core provides for an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard user mode and kernel modes of operation, the core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a debug exception return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define what registers are selected and how they are used.

FIGURE 4-4: MEMORY MAP ON RESET FOR PIC32MX340F128H, PIC32MX340F128L, PIC32MX440F128H AND PIC32MX440F128L DEVICES⁽¹⁾

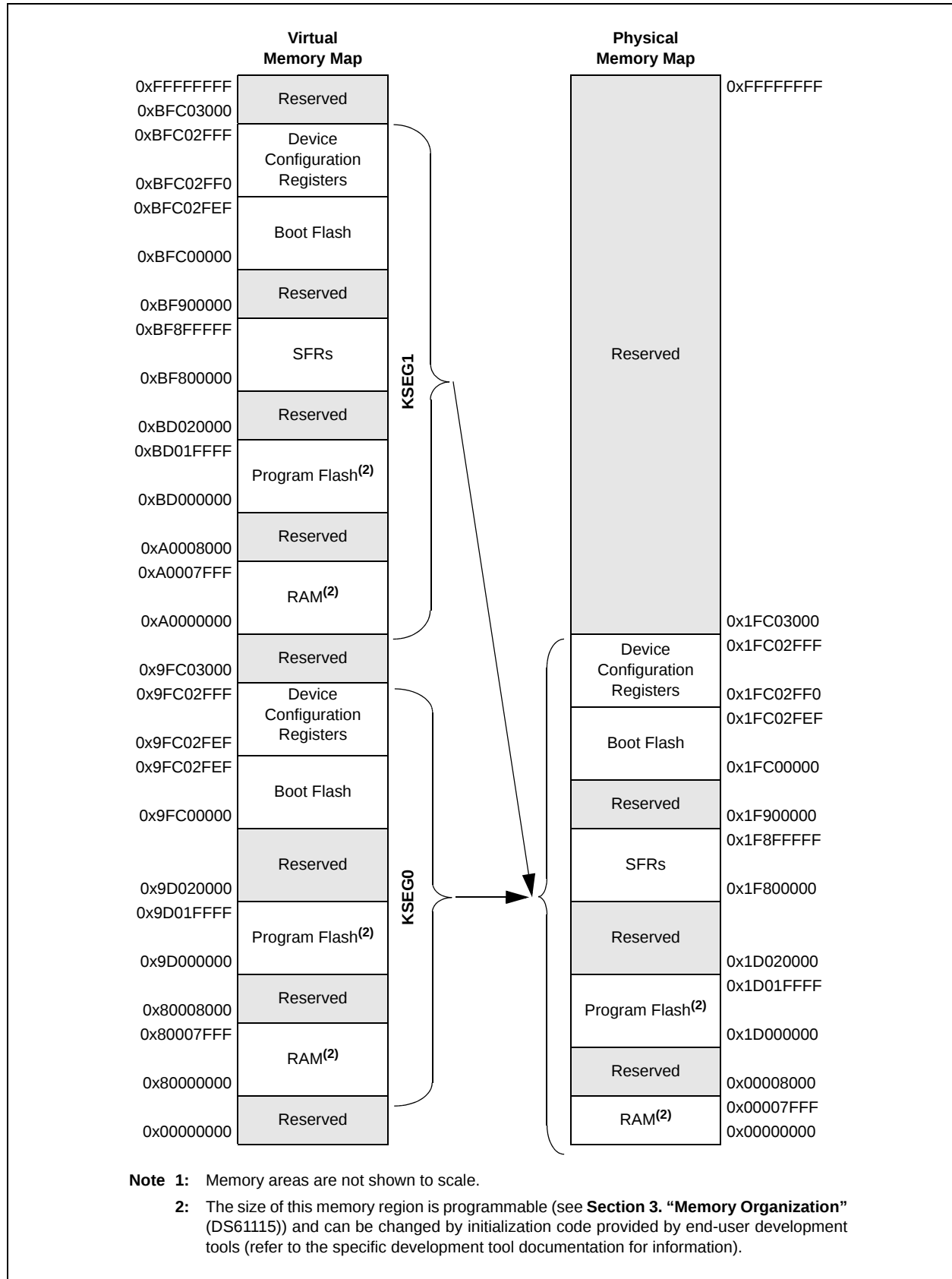


TABLE 4-6: INTERRUPT REGISTERS MAP FOR THE PIC32MX420F032H DEVICE ONLY⁽¹⁾

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			—	—	VEC<5:0>						0000
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	—	—	—	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	0000
		15:0	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	—	—	—	—	—	—	USBIF	FCEIF	—	—	—	—	—	—	—	—	0000
		15:0	RTCCIF	FSCMIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF	SPI2RXIF	SPI2TXIF	SPI2EIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF	0000
1060	IEC0	31:16	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	—	—	—	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE	0000
		15:0	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	—	—	—	—	—	—	USBIE	FCEIE	—	—	—	—	—	—	—	—	0000
		15:0	RTCCIE	FSCMIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE	U2RXIE	U2EIE	SPI2RXIE	SPI2TXIE	SPI2EIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE	0000
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>			—	—	—	CS1IP<2:0>		CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>			—	—	—	CTIP<2:0>		CTIS<1:0>		0000
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>			—	—	—	OC1IP<2:0>		OC1IS<1:0>		0000
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>			—	—	—	T1IP<2:0>		T1IS<1:0>		0000
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>			—	—	—	OC2IP<2:0>		OC2IS<1:0>		0000
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>			—	—	—	T2IP<2:0>		T2IS<1:0>		0000
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>			—	—	—	OC3IP<2:0>		OC3IS<1:0>		0000
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>			—	—	—	T3IP<2:0>		T3IS<1:0>		0000
10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>			—	—	—	OC4IP<2:0>		OC4IS<1:0>		0000
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>			—	—	—	T4IP<2:0>		T4IS<1:0>		0000
10E0	IPC5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	OC5IP<2:0>		OC5IS<1:0>		0000
		15:0	—	—	—	IC5IP<2:0>			IC5IS<1:0>			—	—	—	T5IP<2:0>		T5IS<1:0>		0000
10F0	IPC6	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>			—	—	—	CNIP<2:0>		CNIS<1:0>		0000
		15:0	—	—	—	I2C1IP<2:0>			I2C1IS<1:0>			—	—	—	U1IP<2:0>		U1IS<1:0>		0000
1100	IPC7	31:16	—	—	—	SPI2IP<2:0>			SPI2IS<1:0>			—	—	—	CMP2IP<2:0>		CMP2IS<1:0>		0000
		15:0	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>			—	—	—	PMPIP<2:0>		PMPIS<1:0>		0000
1110	IPC8	31:16	—	—	—	RTCCIP<2:0>			RTCCIS<1:0>			—	—	—	FSCMIP<2:0>		FSCMIS<1:0>		0000
		15:0	—	—	—	I2C2IP<2:0>			I2C2IS<1:0>			—	—	—	U2IP<2:0>		U2IS<1:0>		0000
1140	IPC11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	USBIP<2:0>			USBIS<1:0>			—	—	—	FCEIP<2:0>		FCEIS<1:0>		0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

2: This register does not have associated CLR, SET, and INV registers.

TABLE 4-43: USB REGISTERS MAP⁽¹⁾

Virtual Address (BF88-#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5040	U1OTG IR ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15:0	—	—	—	—	—	—	—	—	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF	0000
5050	U1OTG IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE	0000
5060	U1OTG STAT ⁽³⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD	0000
5070	U1OTG CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
5080	U1PWRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UACTPND ⁽⁴⁾	—	—	USLPGRD	—	—	USUSPEND	USBPWR	0000
5200	U1IR ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF DETACHIF	0000 0000
5210	U1IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE DETACHIE	0000 0000
5220	U1EIR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF EOFEF	PIDEF	0000 0000
5230	U1EIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE EOFEE	PIDEE	0000 0000
5240	U1STAT ⁽³⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ENDPT<3:0> ⁽⁴⁾				DIR	PPBI	—	—	0000
5250	U1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	JSTATE ⁽⁴⁾	SE0 ⁽⁴⁾	PKTDIS TOKBUSY	USBRST	HOSTEN	RESUME	PPBRST	USBEN SOFEN	0000 0000
5260	U1ADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPDEN	DEVADDR<6:0>							0000
5270	U1BDTP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRL<7:1>							—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
- 2:** This register does not have associated CLR, SET, and INV registers.
- 3:** All bits in this register are read-only; therefore, CLR, SET, and INV registers are not supported.
- 4:** The reset value for this bit is undefined.

PIC32MX3XX/4XX

NOTES:

18.0 INTER-INTEGRATED CIRCUIT™ (I²C™)

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. “Inter-Integrated Circuit (I²C™)”** (DS61116) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The I²C module provides complete hardware support for both Slave and Multi-Master modes of the I²C serial communication standard. Figure 18-1 illustrates the I²C module block diagram.

The PIC32MX3XX/4XX devices have up to two I²C interface modules, denoted as I2C1 and I2C2. Each I²C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I²C module, ‘I2Cx’ (x = 1 or 2), offers the following key features:

- I²C Interface Supporting both Master and Slave Operation.
- I²C Slave Mode Supports 7 and 10-bit Address.
- I²C Master Mode Supports 7 and 10-bit Address.
- I²C Port allows Bidirectional Transfers between Master and Slaves.
- Serial Clock Synchronization for I²C Port can be used as a Handshake Mechanism to Suspend and Resume Serial Transfer (SCLREL control).
- I²C Supports Multi-master Operation; Detects Bus Collision and Arbitrates Accordingly.
- Provides Support for Address Bit Masking.

23.0 COMPARATOR

Note 1: This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to **Section 19. “Comparator”** (DS61110) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

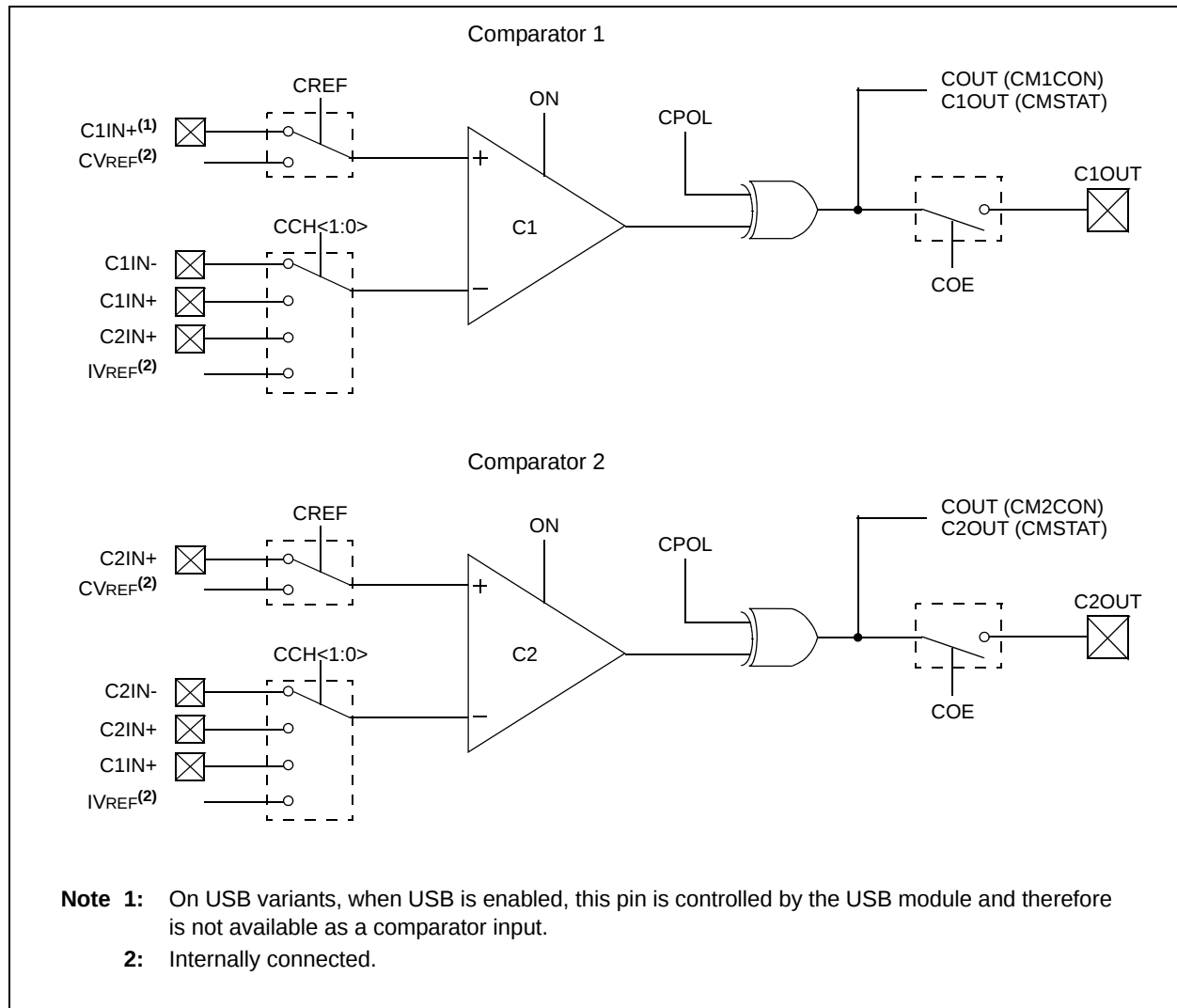
The PIC32MX3XX/4XX Analog Comparator module contains one or more comparator(s) that can be configured in a variety of ways.

Following are some of the key features of this module:

- Selectable inputs available include:
 - Analog inputs multiplexed with I/O pins
 - On-chip internal absolute voltage reference (IVREF)
 - Comparator voltage reference (CVREF)
- Outputs can be inverted
- Selectable interrupt generation

A block diagram of the comparator module is illustrated in Figure 23-1.

FIGURE 23-1: COMPARATOR BLOCK DIAGRAM



PIC32MX3XX/4XX

REGISTER 26-6: DDPCON: DEBUG DATA PORT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-X	r-X	r-X	r-X	r-X	r-X	r-X	r-X
	—	—	—	—	—	—	—	—
23:16	r-X	r-X	r-X	r-X	r-X	r-X	r-X	r-X
	—	—	—	—	—	—	—	—
15:8	r-X	r-X	r-X	r-X	r-X	r-X	r-X	r-X
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	r-X	r-X
	DDPUSB	DDPU1	DDPU2	DDPSPI1	JTAGEN	TROEN	—	—

Legend:

R = Readable bit W = Writable bit P = Programmable bit r = Reserved bit
U = Unimplemented bit -n = Bit Value at POR: ('0', '1', x = Unknown)

bit 31-8 **Reserved:** Write '0'; ignore read

bit 7 **DDPUSB:** Debug Data Port Enable for USB bit
1 = USB peripheral ignores USBFRZ (U1CNFG1<5>) setting
0 = USB peripheral follows USBFRZ setting

bit 6 **DDPU1:** Debug Data Port Enable for UART1 bit
1 = UART1 peripheral ignores FRZ (U1MODE<14>) setting
0 = UART1 peripheral follows FRZ setting

bit 5 **DDPU2:** Debug Data Port Enable for UART2 bit
1 = UART2 peripheral ignores FRZ (U2MODE<14>) setting
0 = UART2 peripheral follows FRZ setting

bit 4 **DDPSPI1:** Debug Data Port Enable for SPI1 bit
1 = SPI1 peripheral ignores FRZ (SPI1CON<14>) setting
0 = SPI1 peripheral follows FRZ setting

bit 3 **JTAGEN:** JTAG Port Enable bit
1 = Enable JTAG Port
0 = Disable JTAG Port

bit 2 **TROEN:** Trace Output Enable bit
1 = Enable Trace Port
0 = Disable Trace Port

bit 1-0 **Reserved:** Write '1'; ignore read

27.0 INSTRUCTION SET

The PIC32MX3XX/4XX family instruction set complies with the MIPS32 Release 2 instruction set architecture. PIC32MX does not support the following features:

- CoreExtend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Table 27-1 provides a summary of the instructions that are implemented by the PIC32MX3XX/4XX family core.

Note: Refer to “MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set” at www.mips.com for more information.

TABLE 27-1: MIPS32® INSTRUCTION SET

Instruction	Description	Function
ADD	Integer Add	$Rd = Rs + Rt$
ADDI	Integer Add Immediate	$Rt = Rs + \text{Immed}$
ADDIU	Unsigned Integer Add Immediate	$Rt = Rs +_U \text{Immed}$
ADDU	Unsigned Integer Add	$Rd = Rs +_U Rt$
AND	Logical AND	$Rd = Rs \& Rt$
ANDI	Logical AND Immediate	$Rt = Rs \& (0_{16} \parallel \text{Immed})$
B	Unconditional Branch (Assembler idiom for: BEQ r0, r0, offset)	$PC += (\text{int})\text{offset}$
BAL	Branch and Link (Assembler idiom for: BGEZAL r0, offset)	$GPR[31] = PC + 8$ $PC += (\text{int})\text{offset}$
BEQ	Branch on Equal	if $Rs == Rt$ $PC += (\text{int})\text{offset}$
BEQL	Branch on Equal Likely ⁽¹⁾	if $Rs == Rt$ $PC += (\text{int})\text{offset}$ else Ignore Next Instruction
BGEZ	Branch on Greater Than or Equal to Zero	if $!Rs[31]$ $PC += (\text{int})\text{offset}$
BGEZAL	Branch on Greater Than or Equal to Zero and Link	$GPR[31] = PC + 8$ if $!Rs[31]$ $PC += (\text{int})\text{offset}$
BGEZALL	Branch on Greater Than or Equal to Zero and Link Likely ⁽¹⁾	$GPR[31] = PC + 8$ if $!Rs[31]$ $PC += (\text{int})\text{offset}$ else Ignore Next Instruction
BGEZL	Branch on Greater Than or Equal to Zero Likely ⁽¹⁾	if $!Rs[31]$ $PC += (\text{int})\text{offset}$ else Ignore Next Instruction
BGTZ	Branch on Greater Than Zero	if $!Rs[31] \&\& Rs != 0$ $PC += (\text{int})\text{offset}$
BGTZL	Branch on Greater Than Zero Likely ⁽¹⁾	if $!Rs[31] \&\& Rs != 0$ $PC += (\text{int})\text{offset}$ else Ignore Next Instruction
BLEZ	Branch on Less Than or Equal to Zero	if $Rs[31] \parallel Rs == 0$ $PC += (\text{int})\text{offset}$

Note 1: This instruction is deprecated and should not be used.

TABLE 27-1: MIPS32® INSTRUCTION SET (CONTINUED)

Instruction	Description	Function
TGE	Trap if Greater Than or Equal	if (int)Rs >= (int)Rt TrapException
TGEI	Trap if Greater Than or Equal Immediate	if (int)Rs >= (int)Immed TrapException
TGEIU	Trap if Greater Than or Equal Immediate Unsigned	if (uns)Rs >= (uns)Immed TrapException
TGEU	Trap if Greater Than or Equal Unsigned	if (uns)Rs >= (uns)Rt TrapException
TLT	Trap if Less Than	if (int)Rs < (int)Rt TrapException
TLTI	Trap if Less Than Immediate	if (int)Rs < (int)Immed TrapException
TLTIU	Trap if Less Than Immediate Unsigned	if (uns)Rs < (uns)Immed TrapException
TLTU	Trap if Less Than Unsigned	if (uns)Rs < (uns)Rt TrapException
TNE	Trap if Not Equal	if Rs != Rt TrapException
TNEI	Trap if Not Equal Immediate	if Rs != (int)Immed TrapException
WAIT	Wait for Interrupt	Go to a low power mode and stall until interrupt occurs
WRPGPR	Write to GPR in Previous Shadow Set	SGPR[SRSCtl _{PSS} , Rd] = Rt
WSBH	Word Swap Bytes Within Halfwords	Rd = Rt _{23..16} Rt _{31..24} Rt _{7..0} Rt _{15..8}
XOR	Exclusive OR	Rd = Rs ^ Rt
XORI	Exclusive OR Immediate	Rt = Rs ^ (uns)Immed

Note 1: This instruction is deprecated and should not be used.

28.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

28.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

28.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

28.10 PICkit 3 In-Circuit Debugger/Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC® and dsPIC® Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming™.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

TABLE 29-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)		
			Operating temperature -40°C ≤TA ≤+85°C for Industrial 		

- Note 1:** Base IPD is measured with all digital peripheral modules disabled. All I/Os are configured as inputs and pulled low. WDT and FSCM are disabled.
- 2:** Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.
- 4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.
- 5:** Data is characterized at +70°C and not tested. Parameter is for design guidance only.
- 6:** This parameter is characterized, but not tested in manufacturing.

PIC32MX3XX/4XX

TABLE 29-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Param. No.	Symbol	Characteristics		Min. ⁽¹⁾	Max.	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	T _{PB} * (BRG + 2)	—	μs	—
			400 kHz mode	T _{PB} * (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	T _{PB} * (BRG + 2)	—	μs	
IM11	THI:SCL	Clock High Time	100 kHz mode	T _{PB} * (BRG + 2)	—	μs	—
			400 kHz mode	T _{PB} * (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	T _{PB} * (BRG + 2)	—	μs	
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF.
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode ⁽²⁾	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF.
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode ⁽²⁾	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode ⁽²⁾	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	—
			400 kHz mode	0	0.9	μs	
			1 MHz mode ⁽²⁾	0	0.3	μs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	T _{PB} * (BRG + 2)	—	μs	Only relevant for Repeated Start condition.
			400 kHz mode	T _{PB} * (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	T _{PB} * (BRG + 2)	—	μs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	T _{PB} * (BRG + 2)	—	μs	After this period, the first clock pulse is generated.
			400 kHz mode	T _{PB} * (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	T _{PB} * (BRG + 2)	—	μs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	T _{PB} * (BRG + 2)	—	μs	—
			400 kHz mode	T _{PB} * (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	T _{PB} * (BRG + 2)	—	μs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	T _{PB} * (BRG + 2)	—	ns	—
			400 kHz mode	T _{PB} * (BRG + 2)	—	ns	
			1 MHz mode ⁽²⁾	T _{PB} * (BRG + 2)	—	ns	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	—
			400 kHz mode	—	1000	ns	
			1 MHz mode ⁽²⁾	—	350	ns	
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus must be free before a new transmission can start.
			400 kHz mode	1.3	—	μs	
			1 MHz mode ⁽²⁾	0.5	—	μs	
IM50	Cb	Bus Capacitive Loading		—	400	pF	—
IM51	TPGD	Pulse Gobbler Delay ⁽³⁾		52	312	ns	—

Note 1: BRG is the value of the I²C™ Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

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TABLE 29-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	μs	PBCLK must operate at a minimum of 800 KHz.
			400 kHz mode	1.3	—	μs	PBCLK must operate at a minimum of 3.2 MHz.
			1 MHz mode ⁽¹⁾	0.5	—	μs	—
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μs	PBCLK must operate at a minimum of 800 KHz.
			400 kHz mode	0.6	—	μs	PBCLK must operate at a minimum of 3.2 MHz.
			1 MHz mode ⁽¹⁾	0.5	—	μs	—
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF.
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode ⁽¹⁾	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF.
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode ⁽¹⁾	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode ⁽¹⁾	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	—
			400 kHz mode	0	0.9	μs	
			1 MHz mode ⁽¹⁾	0	0.3	μs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4700	—	ns	Only relevant for Repeated Start condition.
			400 kHz mode	600	—	ns	
			1 MHz mode ⁽¹⁾	250	—	ns	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated.
			400 kHz mode	600	—	ns	
			1 MHz mode ⁽¹⁾	250	—	ns	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
			1 MHz mode ⁽¹⁾	600	—	ns	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
			1 MHz mode ⁽¹⁾	250	—	ns	
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	ns	—
			400 kHz mode	0	1000	ns	
			1 MHz mode ⁽¹⁾	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus must be free before a new transmission can start.
			400 kHz mode	1.3	—	μs	
			1 MHz mode ⁽¹⁾	0.5	—	μs	
IS50	Cb	Bus Capacitive Loading		—	400	pF	—

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

TABLE 29-34: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.5	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module VSS Supply	VSS	—	VSS + 0.3	V	—
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 2.0	—	AVDD	V	(Note 1)
AD05a			2.5	—	3.6	V	VREFH = AVDD (Note 3)
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 2.0	V	(Note 1)
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	2.0	—	AVDD	V	(Note 3)
AD08	IREF	Current Drain	—	250 —	400 3	μA μA	ADC operating ADC off
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	—
AD13	VINL	Absolute VINL Input Voltage	AVSS – 0.3	—	AVDD/2	V	—
AD14	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	—
AD15	—	Leakage Current	—	±0.001	±0.610	μA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V Source Impedance = 10KΩ
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	5K	Ω	(Note 1)
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	10 data bits			bits	—
AD21c	INL	Integral Nonlinearity	—	—	<±1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD22c	DNL	Differential Nonlinearity	—	—	<±1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V (Note 2)
AD23c	GERR	Gain Error	—	—	<±1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD24n	EOFF	Offset Error	—	—	<±1	LSb	VINL = AVSS = 0V, AVDD = 3.3V
AD25c	—	Monotonicity	—	—	—	—	Guaranteed

Note 1: These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

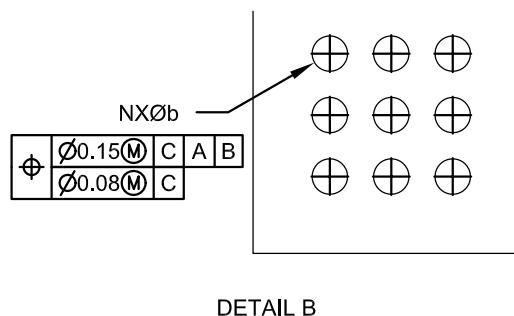
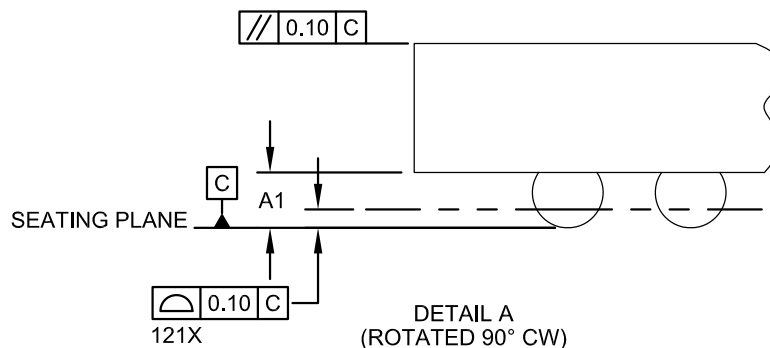
3: These parameters are characterized, but not tested in manufacturing.

4: Characterized with 1 kHz sinewave.

PIC32MX3XX/4XX

121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [XBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Contacts	N	121		
Contact Pitch	e	0.80 BSC		
Overall Height	A	1.00	1.10	1.20
Standoff	A1	0.25	0.30	0.35
Molded Package Thickness	A2	0.55	0.60	0.65
Overall Width	E	10.00 BSC		
Array Width	E1	8.00 BSC		
Overall Length	D	10.00 BSC		
Array Length	D1	8.00 BSC		
Contact Diameter	b	0.40 TYP		

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
- The outer rows and columns of balls are located with respect to datums A and B.

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APPENDIX A: REVISION HISTORY

Revision E (July 2008)

- Updated the PIC32MX340F128H features in Table 1 to include 4 programmable DMA channels.

Revision F (June 2009)

This revision includes minor typographical and formatting changes throughout the data sheet text.

Global changes include:

- Changed all instances of OSCI to OSC1 and OSC0 to OSC2
- Changed all instances of VDDCORE and VDDCORE/VCAP to VCAP/VDDCORE
- Deleted registers in most sections, refer to the related section of the “PIC32 Family Reference Manual” (DS61132).

The other changes are referenced by their respective section in the following table.

TABLE A-1: MAJOR SECTION UPDATES

Section Name	Update Description
“High-Performance, General Purpose and USB 32-bit Flash Microcontrollers”	Added a “Packages” column to Table 1 and Table 2. Corrected all pin diagrams to update the following pin names. - Changed PGC1/EMUC1 to PGEC1 - Changed PGD1/EMUD1 to PGED1 - Changed PGC2/EMUC2 to PGEC2 - Changed PGD2/EMUD2 to PGED2 Shaded appropriate pins in each diagram to indicate which pins are 5V tolerant. Added 64-Lead QFN package pin diagrams, one for General Purpose and one for USB.
Section 1.0 “Device Overview”	Reconstructed Figure 1-1 to include Timers, ADC and RTCC in the block diagram.
Section 2.0 “Guidelines for Getting Started with 32-bit Microcontrollers”	Added a new section to the data sheet that provides the following information: - Basic Connection Requirements - Capacitors - Master Clear Pin - ICSP™ Pins - External Oscillator Pins - Configuration of Analog and Digital Pins - Unused I/Os
Section 4.0 “Memory Organization”	Updated the memory maps, Figure 4-1 through Figure 4-6. All summary peripheral register maps were relocated to Section 4.0 “Memory Organization”.
Section 7.0 “Interrupt Controller”	Removed the “Address” column from Table 7-1.
Section 12.0 “I/O Ports”	Added a second paragraph in Section 12.1.3 “Analog Inputs” to clarify that all pins that share ANx functions are analog by default, because the AD1PCFG register has a default value of 0x0000.