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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

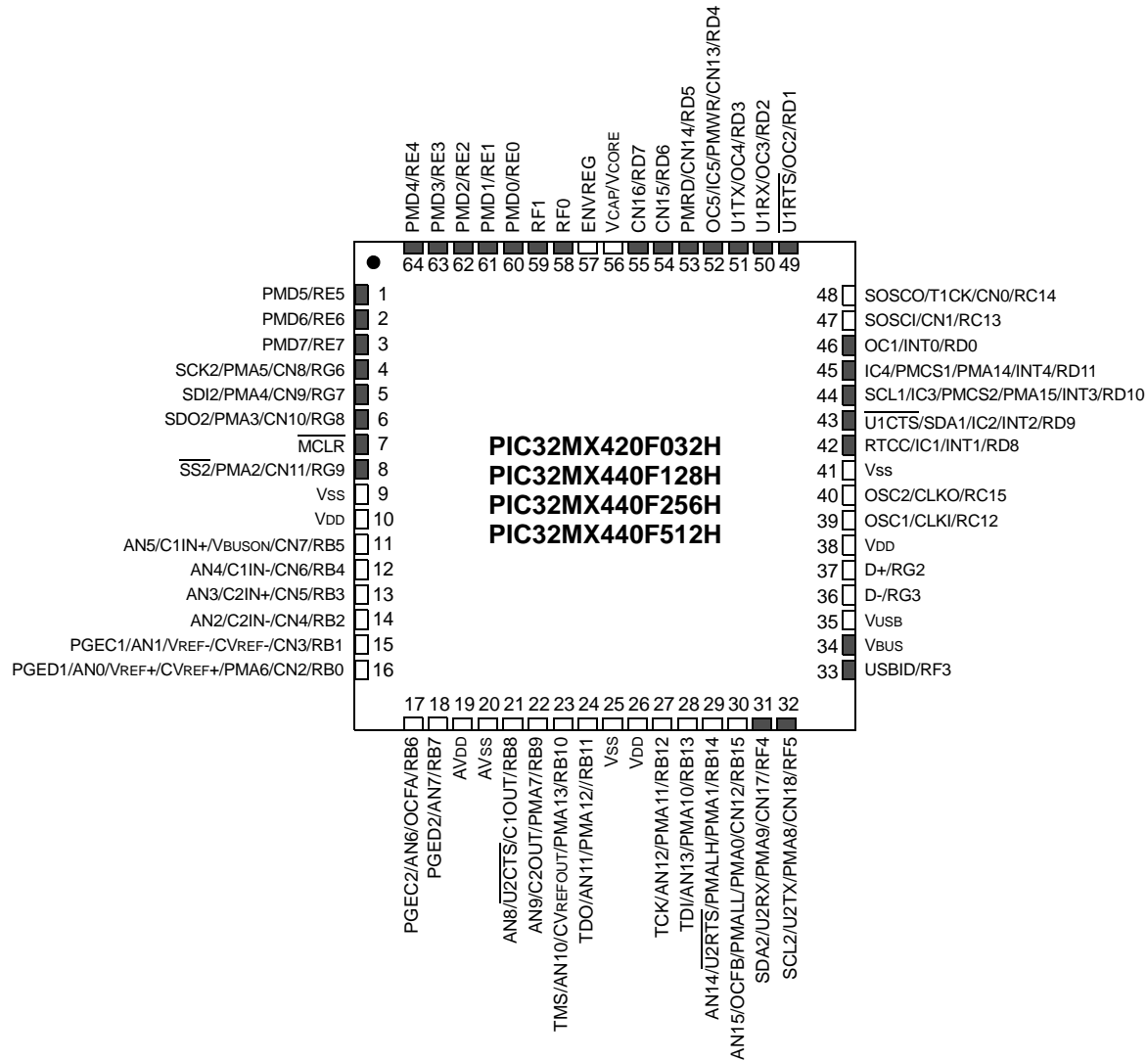
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx440f128lt-80i-bg">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx440f128lt-80i-bg</a>

# PIC32MX3XX/4XX

## Pin Diagrams (Continued)

### 64-Pin QFN (USB)

■ = Pins are up to 5V tolerant



**Note:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number <sup>(1)</sup>			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
RD0	46	72	D9	I/O	ST	PORTD is a bidirectional I/O port.
RD1	49	76	A11	I/O	ST	
RD2	50	77	A10	I/O	ST	
RD3	51	78	B9	I/O	ST	
RD4	52	81	C8	I/O	ST	
RD5	53	82	B8	I/O	ST	
RD6	54	83	D7	I/O	ST	
RD7	55	84	C7	I/O	ST	
RD8	42	68	E9	I/O	ST	
RD9	43	69	E10	I/O	ST	
RD10	44	70	D11	I/O	ST	
RD11	45	71	C11	I/O	ST	
RD12	—	79	A9	I/O	ST	
RD13	—	80	D8	I/O	ST	
RD14	—	47	L9	I/O	ST	
RD15	—	48	K9	I/O	ST	
RE0	60	93	A4	I/O	ST	PORTE is a bidirectional I/O port.
RE1	61	94	B4	I/O	ST	
RE2	62	98	B3	I/O	ST	
RE3	63	99	A2	I/O	ST	
RE4	64	100	A1	I/O	ST	
RE5	1	3	D3	I/O	ST	
RE6	2	4	C1	I/O	ST	
RE7	3	5	D2	I/O	ST	
RE8	—	18	G1	I/O	ST	
RE9	—	19	G2	I/O	ST	
RF0	58	87	B6	I/O	ST	PORTF is a bidirectional I/O port.
RF1	59	88	A6	I/O	ST	
RF2	34	52	K11	I/O	ST	
RF3	33	51	K10	I/O	ST	
RF4	31	49	L10	I/O	ST	
RF5	32	50	L11	I/O	ST	
RF6	35	55	H9	I/O	ST	
RF7	—	54	H8	I/O	ST	
RF8	—	53	J10	I/O	ST	
RF12	—	40	K6	I/O	ST	
RF13	—	39	L6	I/O	ST	

**Legend:** CMOS = CMOS compatible input or output      Analog = Analog input      P = Power  
ST = Schmitt Trigger input with CMOS levels      O = Output      I = Input  
TTL = TTL input buffer

**Note 1:** Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

# PIC32MX3XX/4XX

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number <sup>(1)</sup>			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
RG0	—	90	A5	I/O	ST	PORTG is a bidirectional I/O port.
RG1	—	89	E6	I/O	ST	
RG6	4	10	E3	I/O	ST	
RG7	5	11	F4	I/O	ST	
RG8	6	12	F2	I/O	ST	
RG9	8	14	F3	I/O	ST	
RG12	—	96	C3	I/O	ST	
RG13	—	97	A3	I/O	ST	
RG14	—	95	C4	I/O	ST	
RG15	—	1	B2	I/O	ST	
RG2	37	57	H10	I	ST	PORTG input pins.
RG3	36	56	J11	I	ST	
T1CK	48	74	B11	I	ST	Timer1 external clock input.
T2CK	—	6	D1	I	ST	Timer2 external clock input.
T3CK	—	7	E4	I	ST	Timer3 external clock input.
T4CK	—	8	E2	I	ST	Timer4 external clock input.
T5CK	—	9	E1	I	ST	Timer5 external clock input.
U1CTS	43	47	L9	I	ST	UART1 clear to send.
U1RTS	35, 49	48	K9	O	—	UART1 ready to send.
U1RX	34, 50	52	K11	I	ST	UART1 receive.
U1TX	33, 51	51, 53	J10, K10	O	—	UART1 transmit.
U2CTS	21	40	K6	I	ST	UART2 clear to send.
U2RTS	29	39	L6	O	—	UART2 ready to send.
U2RX	31	49	L10	I	ST	UART2 receive.
U2TX	32	50	L11	O	—	UART2 transmit.
SCK1	35	55, 70	D11, H9	I/O	ST	Synchronous serial clock input/output for SPI1.
SDI1	34	9, 54	E1, H8	I	ST	SPI1 data in.
SDO1	33	53, 72	D9, J10	O	—	SPI1 data out.
SS1	14	23, 69	E10, J2	I/O	ST	SPI1 slave synchronization or frame pulse I/O.
SCK2	4	10	E3	I/O	ST	Synchronous serial clock input/output for SPI2.
SDI2	5	11	F4	I	ST	SPI2 data in.
SDO2	6	12	F2	O	—	SPI2 data out.
SS2	8	14	F3	I/O	ST	SPI2 slave synchronization or frame pulse I/O.
SCL1	37, 44	57, 66	E11, H10	I/O	ST	Synchronous serial clock input/output for I2C1.
SDA1	36, 43	56, 67	E8, J11	I/O	ST	Synchronous serial data input/output for I2C1.
SCL2	32	58	H11	I/O	ST	Synchronous serial clock input/output for I2C2.
SDA2	31	59	G10	I/O	ST	Synchronous serial data input/output for I2C2.

**Legend:** CMOS = CMOS compatible input or output      Analog = Analog input      P = Power  
ST = Schmitt Trigger input with CMOS levels      O = Output      I = Input  
TTL = TTL input buffer

**Note 1:** Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

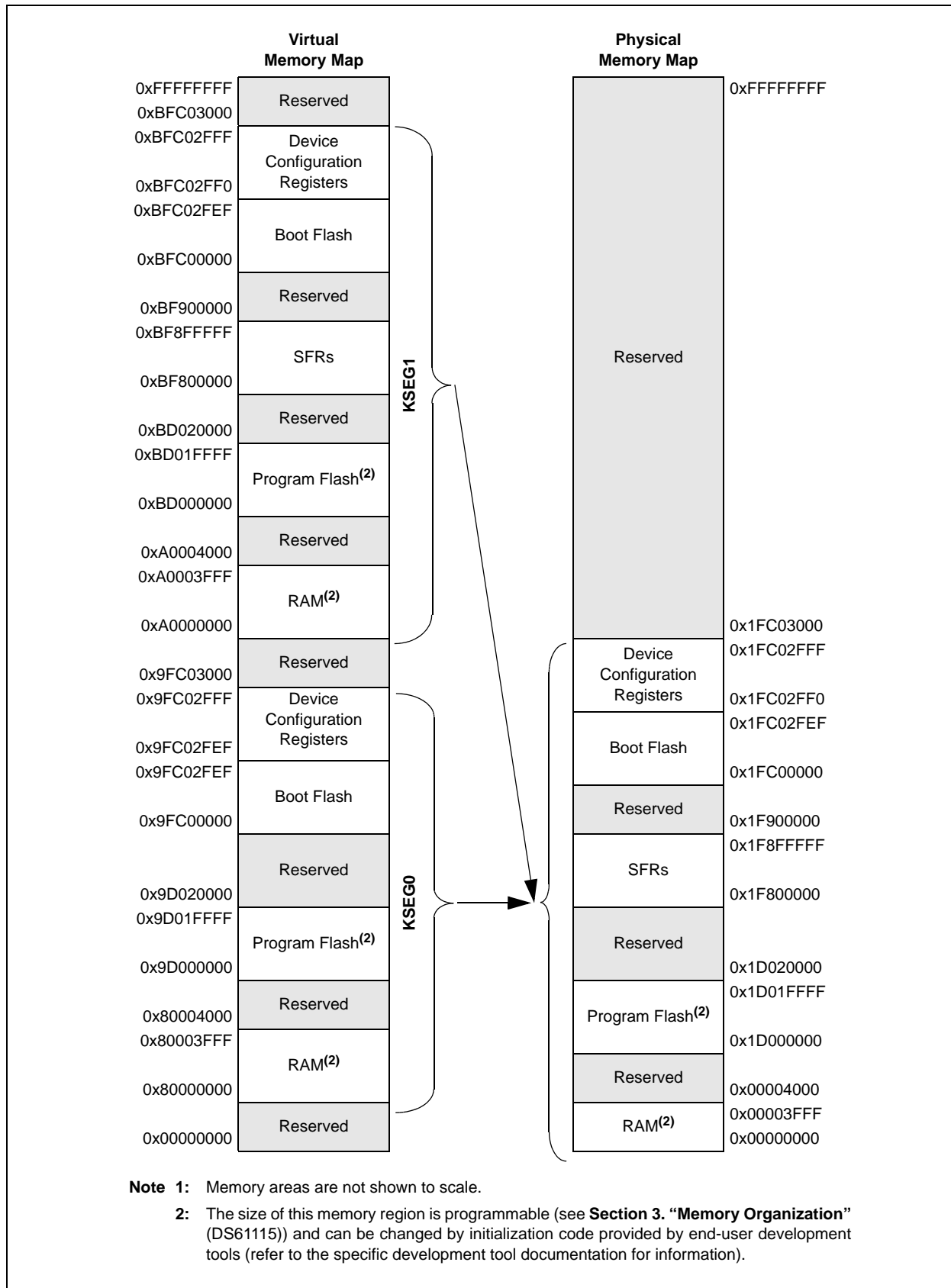
Pin Name	Pin Number <sup>(1)</sup>			Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	121-pin XBGA			
PGED2	18	27	J3	I/O	ST	Data I/O pin for programming/debugging communication channel 2.
PGEC2	17	26	L1	I	ST	Clock input pin for programming/debugging communication channel 2.
MCLR	7	13	F1	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	19	30	J4	P	P	Positive supply for analog modules. This pin must be connected at all times.
AVSS	20	31	L3	P	P	Ground reference for analog modules.
VDD	10, 26, 38	2, 16, 37, 46, 62	C2, C9, E5, F8, G5, H4, H6, K8	P	—	Positive supply for peripheral logic and I/O pins.
VCORE/VCAP	56	85	B7	P	—	Capacitor for Internal Voltage Regulator.
Vss	9, 25, 41	15, 36, 45, 65, 75	A8, B10, D4, D5, E7, F10, F5, G6, G7, H3	P	—	Ground reference for logic and I/O pins.
VREF+	16	29	K3	I	Analog	Analog voltage reference (high) input.
VREF-	15	28	L2	I	Analog	Analog voltage reference (low) input.

**Legend:** CMOS = CMOS compatible input or output      Analog = Analog input      P = Power  
ST = Schmitt Trigger input with CMOS levels      O = Output      I = Input  
TTL = TTL input buffer

**Note 1:** Pin numbers are provided for reference only. See the “Pin Diagrams” section for device pin availability.

# PIC32MX3XX/4XX

**FIGURE 4-3: MEMORY MAP ON RESET FOR PIC32MX320F128H AND PIC32MX320F128L DEVICES<sup>(1)</sup>**



**TABLE 4-7: TIMER1-5 REGISTERS MAP<sup>(1)</sup>**

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	T1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	TWDIS	TWIP	—	—	—	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—	0000
0610	TMR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR1<15:0>																0000
0620	PR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR1<15:0>																FFFF
0800	T2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>		—	T32	—	TCS <sup>(2)</sup>	—	0000
0810	TMR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR2<15:0>																0000
0820	PR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR2<15:0>																FFFF
0A00	T3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>		—	—	—	TCS <sup>(2)</sup>	—	0000
0A10	TMR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR3<15:0>																0000
0A20	PR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR3<15:0>																FFFF
0C00	T4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>		—	T32	—	TCS <sup>(2)</sup>	—	0000
0C10	TMR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR4<15:0>																0000
0C20	PR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR4<15:0>																FFFF
0E00	T5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>		—	—	—	TCS <sup>(2)</sup>	—	0000
0E10	TMR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR5<15:0>																0000
0E20	PR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR5<15:0>																FFFF

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.
- 2: This bit is not available on 64-pin devices.

TABLE 4-13: ADC REGISTERS MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9110	ADC1BUFA	31:16	ADC Result Word A (ADC1BUFA<31:0>)																0000
		15:0																	0000
9120	ADC1BUFB	31:16	ADC Result Word B (ADC1BUFB<31:0>)																0000
		15:0																	0000
9130	ADC1BUFC	31:16	ADC Result Word C (ADC1BUFC<31:0>)																0000
		15:0																	0000
9140	ADC1BUFD	31:16	ADC Result Word D (ADC1BUFD<31:0>)																0000
		15:0																	0000
9150	ADC1BUFE	31:16	ADC Result Word E (ADC1BUFE<31:0>)																0000
		15:0																	0000
9160	ADC1BUFF	31:16	ADC Result Word F (ADC1BUFF<31:0>)																0000
		15:0																	0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.  
**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.



**TABLE 4-43: USB REGISTERS MAP<sup>(1)</sup> (CONTINUED)**

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5280	U1FRML <sup>(3)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	FRML<7:0>								0000
5290	U1FRMH <sup>(3)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	FRMH<10:8>				0000
52A0	U1TOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	PID<3:0>				EP<3:0>				0000
52B0	U1SOF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNT<7:0>								0000
52C0	U1BDTP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRH<7:0>								0000
52D0	U1BDTP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRU<7:0>								0000
52E0	U1CNFG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UTEYE	UOEMON	USBFRZ	USBSIDL	—	—	—	—	0000
5300	U1EP0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPD	RETRYDIS	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5310	U1EP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5320	U1EP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5330	U1EP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5340	U1EP4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5350	U1EP5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5360	U1EP6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5370	U1EP7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

**2:** This register does not have associated CLR, SET, and INV registers.

**3:** All bits in this register are read-only; therefore, CLR, SET, and INV registers are not supported.

**4:** The reset value for this bit is undefined.

**TABLE 4-43: USB REGISTERS MAP<sup>(1)</sup> (CONTINUED)**

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5380	U1EP8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5390	U1EP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53A0	U1EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53B0	U1EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53C0	U1EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53D0	U1EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53E0	U1EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53F0	U1EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 “CLR, SET and INV Registers”** for more information.

**2:** This register does not have associated CLR, SET, and INV registers.

**3:** All bits in this register are read-only; therefore, CLR, SET, and INV registers are not supported.

**4:** The reset value for this bit is undefined.

# PIC32MX3XX/4XX

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NOTES:

## 19.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

**Note 1:** This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. “Universal Asynchronous Receiver Transmitter (UART)”** (DS61107) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com/PIC32](http://www.microchip.com/PIC32)).

**Note 2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

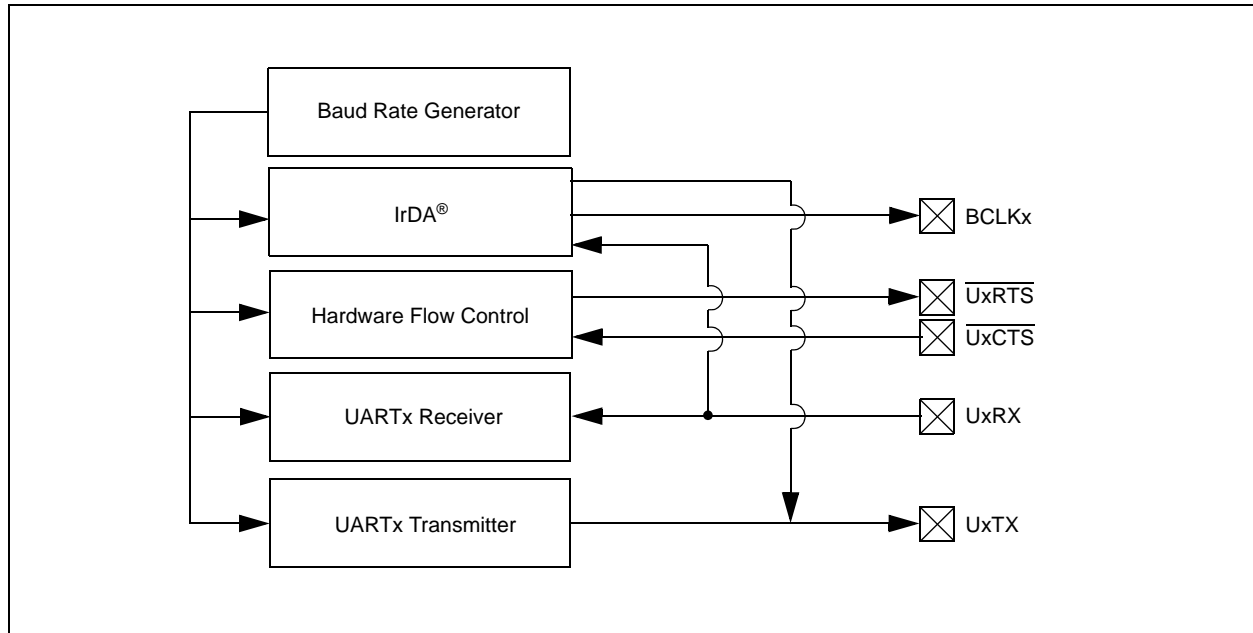
The UART module is one of the serial I/O modules available in PIC32MX3XX/4XX family devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols such as RS-232, RS-485, LIN 1.2 and IrDA®. The module also supports the hardware flow control option, with UxCTS and UxRTS pins, and also includes an IrDA encoder and decoder.

The primary features of the UART module are:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, odd or no parity options (for 8-bit data)
- One or two Stop bits
- Hardware auto-baud feature
- Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 76 bps to 20 Mbps at 80 MHz
- 4-level-deep First-In-First-Out (FIFO) Transmit Data Buffer
- 4-level-deep FIFO Receive Data Buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt only on address detect (9th bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support

Figure 19-1 illustrates a simplified block diagram of the UART.

**FIGURE 19-1: UART SIMPLIFIED BLOCK DIAGRAM**



## 24.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

**Note 1:** This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. Refer to **Section 20. “Comparator Voltage Reference (CVREF)”** (DS61109) of the “PIC32 Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com/PIC32](http://www.microchip.com/PIC32)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

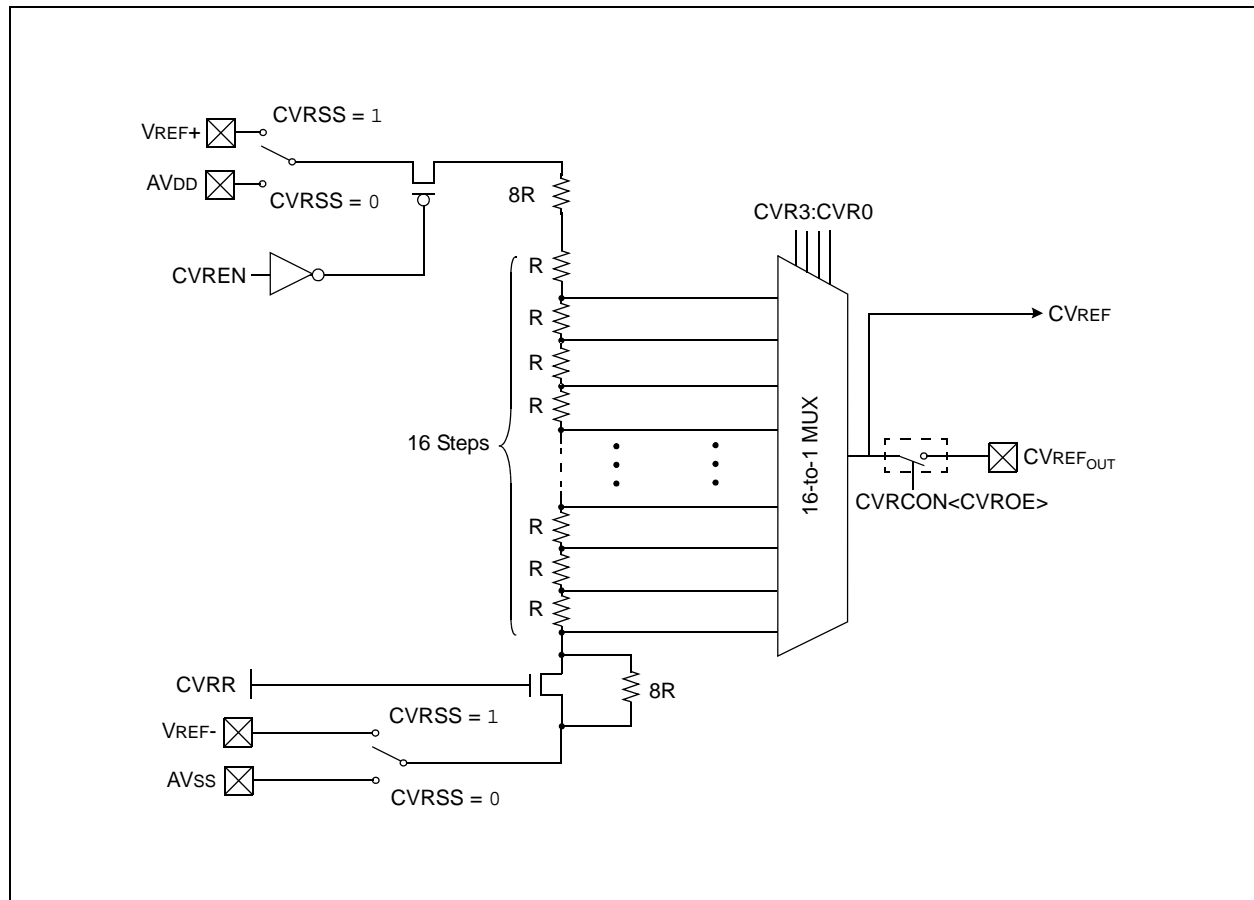
The CVREF is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them.

A block diagram of the module is illustrated in Figure 24-1. The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/VSS or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

The comparator voltage reference has the following features:

- High and low range selection
- Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- Output can be connected to a pin

**FIGURE 24-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM**



# PIC32MX3XX/4XX

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## REGISTER 26-1: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

bit 19-12 **PWP<7:0>**: Program Flash Write-Protect bits

Prevents selected program Flash memory pages from being modified during code execution. The PWP bits represent the one's complement of the number of write protected program Flash memory pages.

11111111 = Disabled  
11111110 = 0xBD00\_0FFF  
11111101 = 0xBD00\_1FFF  
11111100 = 0xBD00\_2FFF  
11111011 = 0xBD00\_3FFF  
11111010 = 0xBD00\_4FFF  
11111001 = 0xBD00\_5FFF  
11111000 = 0xBD00\_6FFF  
11110111 = 0xBD00\_7FFF  
11110110 = 0xBD00\_8FFF  
11110101 = 0xBD00\_9FFF  
11110100 = 0xBD00\_AFFF  
11110011 = 0xBD00\_BFFF  
11110010 = 0xBD00\_CFFF  
11110001 = 0xBD00\_DFFF  
11110000 = 0xBD00\_EFFF  
11101111 = 0xBD00\_FFFF  
.  
.  
.  
01111111 = 0xBD07\_FFFF

bit 11-4 **Reserved**: Write '1'

bit 3 **ICESEL**: In-Circuit Emulator/Debugger Communication Channel Select bit

1 = PGEC2/PGED2 pair is used  
0 = PGEC1/PGED1 pair is used

bit 2 **Reserved**: Write '1'

bit 1-0 **DEBUG<1:0>**: Background Debugger Enable bits (forced to '11' if code-protect is enabled)

11 = Debugger disabled  
10 = Debugger enabled  
01 = Reserved (same as '11' setting)  
00 = Reserved (same as '11' setting)

**REGISTER 26-2: DEVCFG1: DEVICE CONFIGURATION WORD 1**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	R/P	r-1	r-1	R/P	R/P	R/P	R/P	R/P
	FWDTEN	—	—	WDTPS<4:0>				
15:8	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P
	IESO	—	FSOSCEN	—	—	FNOSC<2:0>		

**Legend:**

R = Readable bit                      W = Writable bit                      P = Programmable bit                      r = Reserved bit  
U = Unimplemented bit                      -n = Bit Value at POR: ('0', '1', x = Unknown)

bit 31-24 **Reserved:** Write '1'

bit 23 **FWDTEN:** Watchdog Timer Enable bit

1 = The WDT is enabled and cannot be disabled by software  
0 = The WDT is not enabled; it can be enabled in software

bit 22-21 **Reserved:** Write '1'

bit 20-16 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits

10100 = 1:1048576  
10011 = 1:524288  
10010 = 1:262144  
10001 = 1:131072  
10000 = 1:65536  
01111 = 1:32768  
01110 = 1:16384  
01101 = 1:8192  
01100 = 1:4096  
01011 = 1:2048  
01010 = 1:1024  
01001 = 1:512  
01000 = 1:256  
00111 = 1:128  
00110 = 1:64  
00101 = 1:32  
00100 = 1:16  
00011 = 1:8  
00010 = 1:4  
00001 = 1:2  
00000 = 1:1

All other combinations not shown result in operation = '10100'

bit 15-14 **FCKSM<1:0>:** Clock Switching and Monitor Selection Configuration bits

1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled  
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled  
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

**Note 1:** Do not disable Posc (POSCMOD = 00) when using this oscillator source.

# PIC32MX3XX/4XX

**TABLE 27-1: MIPS32® INSTRUCTION SET (CONTINUED)**

Instruction	Description	Function
RDPGPR	Read GPR from Previous Shadow Set	$Rt = SGPR[SRSCtl_{PSS}, Rd]$
ROTR	Rotate Word Right	$Rd = Rt_{sa-1..0} \parallel Rt_{31..sa}$
ROTRV	Rotate Word Right Variable	$Rd = Rt_{Rs-1..0} \parallel Rt_{31..Rs}$
SB	Store Byte	$(byte)Mem[Rs+offset] = Rt$
SC	Store Conditional Word	if $LL_{bit} = 1$ $mem[Rs+offset] = Rt$ $Rt = LL_{bit}$
SDBBP	Software Debug Break Point	Trap to SW Debug Handler
SEB	Sign-Extend Byte	$Rd = SignExtend(Rs-7..0)$
SEH	Sign-Extend Half	$Rd = SignExtend(Rs-15..0)$
SH	Store Half	$(half)Mem[Rs+offset] = Rt$
SLL	Shift Left Logical	$Rd = Rt \ll sa$
SLLV	Shift Left Logical Variable	$Rd = Rt \ll Rs[4:0]$
SLT	Set on Less Than	if $(int)Rs < (int)Rt$ $Rd = 1$ else $Rd = 0$
SLTI	Set on Less Than Immediate	if $(int)Rs < (int)Immed$ $Rt = 1$ else $Rt = 0$
SLTIU	Set on Less Than Immediate Unsigned	if $(uns)Rs < (uns)Immed$ $Rt = 1$ else $Rt = 0$
SLTU	Set on Less Than Unsigned	if $(uns)Rs < (uns)Immed$ $Rd = 1$ else $Rd = 0$
SRA	Shift Right Arithmetic	$Rd = (int)Rt \gg sa$
SRAV	Shift Right Arithmetic Variable	$Rd = (int)Rt \gg Rs[4:0]$
SRL	Shift Right Logical	$Rd = (uns)Rt \gg sa$
SRLV	Shift Right Logical Variable	$Rd = (uns)Rt \gg Rs[4:0]$
SSNOP	Superscalar Inhibit No Operation	NOP
SUB	Integer Subtract	$Rt = (int)Rs - (int)Rd$
SUBU	Unsigned Subtract	$Rt = (uns)Rs - (uns)Rd$
SW	Store Word	$Mem[Rs+offset] = Rt$
SWL	Store Word Left	$Mem[Rs+offset] = Rt$
SWR	Store Word Right	$Mem[Rs+offset] = Rt$
SYNC	Synchronize	Orders the cached coherent and uncached loads and stores for access to the shared memory
SYSCALL	System Call	SystemCallException
TEQ	Trap if Equal	if $Rs == Rt$ TrapException
TEQI	Trap if Equal Immediate	if $Rs == (int)Immed$ TrapException

**Note 1:** This instruction is deprecated and should not be used.



## 28.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

## 28.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, pre-processor, and one-step driver, and can run on multiple platforms.

## 28.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

## 28.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/librarian features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

## 28.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

## 28.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

## 28.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

## 28.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

## 28.10 PICkit 3 In-Circuit Debugger/Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC® and dsPIC® Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming™.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

## 28.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

## 28.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

## 28.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page ([www.microchip.com](http://www.microchip.com)) for the complete list of demonstration, development and evaluation kits.

**TABLE 29-11: DC CHARACTERISTICS: PROGRAM MEMORY<sup>(3)</sup>**

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical <sup>(1)</sup>	Max.	Units	Conditions
<b>Program Flash Memory</b>							
D130	EP	Cell Endurance	1000	—	—	E/W	—
D131	VPR	VDD for Read	V <sub>MIN</sub>	—	3.6	V	—
D132	VPEW	VDD for Erase or Write	3.0	—	3.6	V	—
D134	TRETD	Characteristic Retention	20	—	—	Year	—
D135	IDDP	Supply Current during Programming	—	10	—	mA	—
D136	TWW	Word Write Cycle Time	20	—	40	μs	—
	TRW	Row Write Cycle Time <sup>(2)</sup> (128 words per row)	3	4.5	—	ms	—
D137	TPE	Page Erase Cycle Time	20	—	—	ms	—
D138	TCE	Chip Erase Cycle Time	80	—	—	ms	—
	LVDstartup	Flash LVD Delay	—	—	6	μs	—

**Note 1:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated.

**2:** The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

**3:** Refer to the “PIC32MX Flash Programming Specification” (DS61145) for operating conditions during programming and erase cycles.

**TABLE 29-12: PROGRAM FLASH MEMORY WAIT STATE CHARACTERISTICS**

DC CHARACTERISTICS	Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature    -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp		
	Required Flash wait states	SYSCLK	Units
0 Wait State	0 to 30	MHz	—
1 Wait State	31 to 60		
2 Wait States	61 to 80		

**Note 1:** 40 MHz maximum for PIC32MX320F032H and PIC32MX420F032H devices.

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