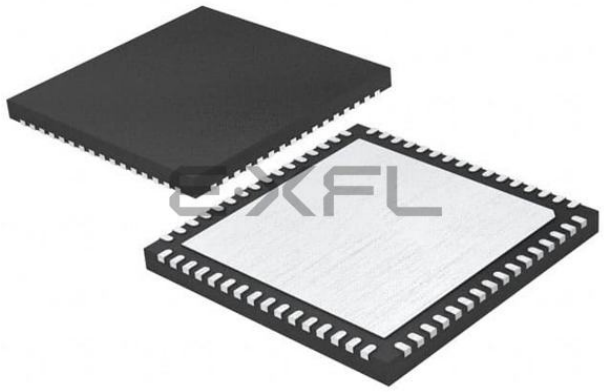
# Microchip Technology - PIC32MX440F512H-80I/MR Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 53 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-VQFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx440f512h-80i-mr |

## Pin Diagrams (Continued)

**121-Pin XBGA(1)**

● = Pins are up to 5V tolerant

**PIC32MX320F128L**
**PIC32MX340F128L**
**PIC32MX360F256L**
**PIC32MX360F512L**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | RE4 | RE3 | RG13 | RE0 | RG0 | RF1 | ENVREG | VSS | RD12 | RD2 | RD1 |
| B | NC | RG15 | RE2 | RE1 | RA7 | RF0 | VCORE/ VCAP | RD5 | RD3 | VSS | RC14 |
| C | RE6 | VDD | RG12 | RG14 | RA6 | NC | RD7 | RD4 | VDD | RC13 | RD11 |
| D | RC1 | RE7 | RE5 | VSS | VSS | NC | RD6 | RD13 | RD0 | NC | RD10 |
| E | RC4 | RC3 | RG6 | RC2 | VDD | RG1 | VSS | RA15 | RD8 | RD9 | RA14 |
| F | $\overline{\text{MCLR}}$ | RG8 | RG9 | RG7 | VSS | NC | NC | VDD | RC12 | VSS | RC15 |
| G | RE8 | RE9 | RA0 | NC | VDD | VSS | VSS | NC | RA5 | RA3 | RA4 |
| H | RB5 | RB4 | VSS | VDD | NC | VDD | NC | RF7 | RF6 | RG2 | RA2 |
| J | RB3 | RB2 | RB7 | AVDD | RB11 | RA1 | RB12 | NC | NC | RF8 | RG3 |
| K | RB1 | RB0 | RA10 | RB8 | NC | RF12 | RB14 | VDD | RD15 | RF3 | RF2 |
| L | RB6 | RA9 | AVSS | RB9 | RB10 | RF13 | RB13 | RB15 | RD14 | RF4 | RF5 |

**Note 1:** Refer to Table 3 for full pin names.

**TABLE 4: PIN NAMES: PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES (CONTINUED)**

| Pin Number | Full Pin Name |
|---|---|
| K4 | AN8/C1OUT/RB8 |
| K5 | No Connect (NC) |
| K6 | U2CTS/RF12 |
| K7 | AN14/PMALH/PMA1/RB14 |
| K8 | VDD |
| K9 | U1RTS/CN21/RD15 |
| K10 | USBID/RF3 |
| K11 | U1RX/RF2 |
| L1 | PGEC2/AN6/OCFA/RB6 |
| L2 | VREF-/CVREF-/PMA7/RA9 |

| Pin Number | Full Pin Name |
|---|---|
| L3 | AVSS |
| L4 | AN9/C2OUT/RB9 |
| L5 | AN10/CVREFOUT/PMA13/RB10 |
| L6 | U2RTS/RF13 |
| L7 | AN13/PMA10/RB13 |
| L8 | AN15/OCFB/PMALL/PMA0/CN12/RB15 |
| L9 | U1CTS/CN20/RD14 |
| L10 | U2RX/PMA9/CN17/RF4 |
| L11 | U2TX/PMA8/CN18/RF5 |

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An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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## 1.0 DEVICE OVERVIEW

**Note 1:** This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

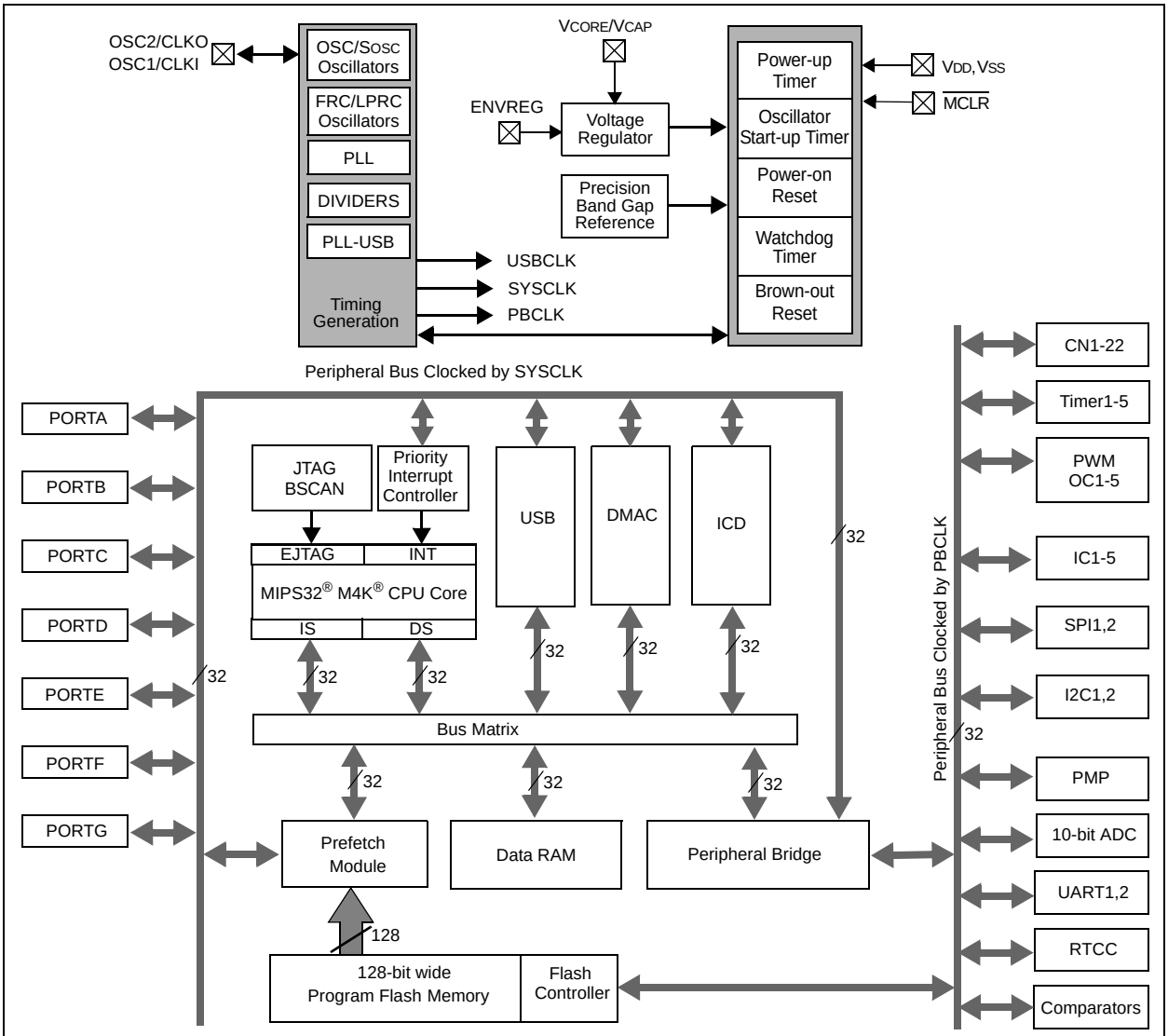
**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the PIC32MX3XX/4XX devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX3XX/4XX family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

**FIGURE 1-1: BLOCK DIAGRAM(1,2)**




**Note 1:** Some features are not available on all device variants.
**2:** BOR functionality is provided when the on-board voltage regulator is enabled.

# 2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MICROCONTROLLERS

**Note 1:** This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

## 2.1 Basic Connection Requirements

Getting started with the PIC32MX3XX/4XX family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins (regardless if ADC module is not used)
  (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP/VCORE
  (see **Section 2.3 "Capacitor on Internal Voltage Regulator (VCAP/VCORE)"**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used
  (see **Section 2.8 "External Oscillator Pins"**)

Additionally, the following pins may be required:

- VREF+/VREF- pins used when external voltage reference for ADC module is implemented

**Note:** The AVDD and AVSS pins must be connected independent of ADC use and ADC voltage reference source.

## 2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

## 2.11 Referenced Sources

This device data sheet is based on the following individual chapters of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

**Note 1:** To access the documents listed below, browse to the documentation section of the PIC32MX460F512L product page on the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features, and other documentation, the resulting page provides links to the related family reference manual sections.

- **Section 1. "Introduction"** (DS61127)
- **Section 2. "CPU"** (DS61113)
- **Section 3. "Memory Organization"** (DS61115)
- **Section 4. "Prefetch Cache"** (DS61119)
- **Section 5. "Flash Program Memory"** (DS61121)
- **Section 6. "Oscillator Configuration"** (DS61112)
- **Section 7. "Resets"** (DS61118)
- **Section 8. "Interrupt Controller"** (DS61108)
- **Section 9. "Watchdog Timer and Power-up Timer"** (DS61114)
- **Section 10. "Power-Saving Features"** (DS61130)
- **Section 12. "I/O Ports"** (DS61120)
- **Section 13. "Parallel Master Port (PMP)"** (DS61128)
- **Section 14. "Timers"** (DS61105)
- **Section 15. "Input Capture"** (DS61122)
- **Section 16. "Output Compare"** (DS61111)
- **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS61104)
- **Section 19. "Comparator"** (DS61110)
- **Section 20. "Comparator Voltage Reference (CV$_{REF}$)"** (DS61109)
- **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS61107)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS61106)
- **Section 24. "Inter-Integrated Circuit™ (I$^2$C™)"** (DS61116)
- **Section 27. "USB On-The-Go (OTG)"** (DS61126)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS61125)
- **Section 31. "Direct Memory Access (DMA) Controller"** (DS61117)
- **Section 32. "Configuration"** (DS61124)
- **Section 33. "Programming and Diagnostics"** (DS61129)

**NOTES:**

**TABLE 4-27: PORTE REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L, PIC32MX360F512L, PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY(1)**

| Virtual Address (BF88_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6100 | TRISE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | TRISE9 | TRISE8 | TRISE7 | TRISE6 | TRISE5 | TRISE4 | TRISE3 | TRISE2 | TRISE1 | TRISE0 | 03FF |
| 6110 | PORTE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | RE9 | RE8 | RE7 | RE6 | RE5 | RE4 | RE3 | RE2 | RE1 | RE0 | xxxx |
| 6120 | LATE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | LATE9 | LATE8 | LATE7 | LATE6 | LATE5 | LATE4 | LATE3 | LATE2 | LATE1 | LATE0 | xxxx |
| 6130 | ODCE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | ODCE9 | ODCE8 | ODCE7 | ODCE6 | ODCE5 | ODCE4 | ODCE3 | ODCE2 | ODCE1 | ODCE0 | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**TABLE 4-28: PORTE REGISTERS MAP FOR PIC32MX320F032H, PIC32MX320F064H, PIC32MX320F128H, PIC32MX340F128H, PIC32MX340F256H, PIC32MX340F512H, PIC32MX420F032H, PIC32MX440F128H, PIC32MX440F256H AND PIC32MX440F512H DEVICES ONLY(1)**

| Virtual Address (BF88_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6100 | TRISE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | TRISE7 | TRISE6 | TRISE5 | TRISE4 | TRISE3 | TRISE2 | TRISE1 | TRISE0 | 00FF |
| 6110 | PORTE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | RE7 | RE6 | RE5 | RE4 | RE3 | RE2 | RE1 | RE0 | xxxx |
| 6120 | LATE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | LATE7 | LATE6 | LATE5 | LATE4 | LATE3 | LATE2 | LATE1 | LATE0 | xxxx |
| 6130 | ODCE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | ODCE7 | ODCE6 | ODCE5 | ODCE4 | ODCE3 | ODCE2 | ODCE1 | ODCE0 | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**TABLE 4-29: PORTF REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L AND PIC32MX360F512L DEVICES ONLY(1)**

| Virtual Address (BF88_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6140 | TRISF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | TRISF13 | TRISF12 | — | — | — | TRISF8 | TRISF7 | TRISF6 | TRISF5 | TRISF4 | TRISF3 | TRISF2 | TRISF1 | TRISF0 | 31FF |
| 6150 | PORTF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | RF13 | RF12 | — | — | — | RF8 | RF7 | RF6 | RF5 | RF4 | RF3 | RF2 | RF1 | RF0 | xxxx |
| 6160 | LATF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | LATF13 | LATF12 | — | — | — | LATF8 | LATF7 | LATF6 | LATF5 | LATF4 | LATF3 | LATF2 | LATF1 | LATF0 | xxxx |
| 6170 | ODCF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | ODCF13 | ODCF12 | — | — | — | ODCF8 | ODCF7 | ODCF6 | ODCF5 | ODCF4 | ODCF3 | ODCF2 | ODCF1 | ODCF0 | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**TABLE 4-30: PORTF REGISTERS MAP FOR PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY(1)**

| Virtual Address (BF88_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6140 | TRISF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | TRISF13 | TRISF12 | — | — | — | TRISF8 | — | — | TRISF5 | TRISF4 | TRISF3 | TRISF2 | TRISF1 | TRISF0 | 313F |
| 6150 | PORTF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | RF13 | RF12 | — | — | — | RF8 | — | — | RF5 | RF4 | RF3 | RF2 | RF1 | RF0 | xxxx |
| 6160 | LATF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | LATF13 | LATF12 | — | — | — | LATF8 | — | — | LATF5 | LATF4 | LATF3 | LATF2 | LATF1 | LATF0 | xxxx |
| 6170 | ODCF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | ODCF13 | ODCF12 | — | — | — | ODCF8 | — | — | ODCF5 | ODCF4 | ODCF3 | ODCF2 | ODCF1 | ODCF0 | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

## 5.0 FLASH PROGRAM MEMORY

**Note 1:** This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. "Flash Program Memory"** (DS61121) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

PIC32MX3XX/4XX devices contain an internal program Flash memory for executing user code. There are three methods by which the user can program this memory:

- Run-Time Self Programming (RTSP)
- In-Circuit Serial Programming™ (ICSP™)
- EJTAG Programming

RTSP is performed by software executing from either Flash or RAM memory. EJTAG is performed using the EJTAG port of the device and a EJTAG capable programmer. ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP. RTSP techniques are described in this chapter. The ICSP and EJTAG methods are described in the "*PIC32MX Flash Programming Specification*" (DS61145), which can be downloaded from the Microchip web site.

**Note:** Flash LVD Delay (LVDstartup) must be taken into account between setting up and executing any Flash command operation. See Example 5-1 for a code example to set up and execute a Flash command operation.

**EXAMPLE 5-1:**

```
NVMCON = 0x4004;          // Enable and configure for erase operation
Wait(delay);              // Delay for 6 µs for LVDstartup

NVMKEY = 0xAA996655;
NVMKEY = 0x556699AA;
NVMCONSET = 0x8000;       // Initiate operation

while(NVMCONbits.WR==1);  // Wait for current operation to complete
```

**NOTES:**

## 10.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

**Note 1:** This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. "Direct Memory Access (DMA) Controller"** (DS61117) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

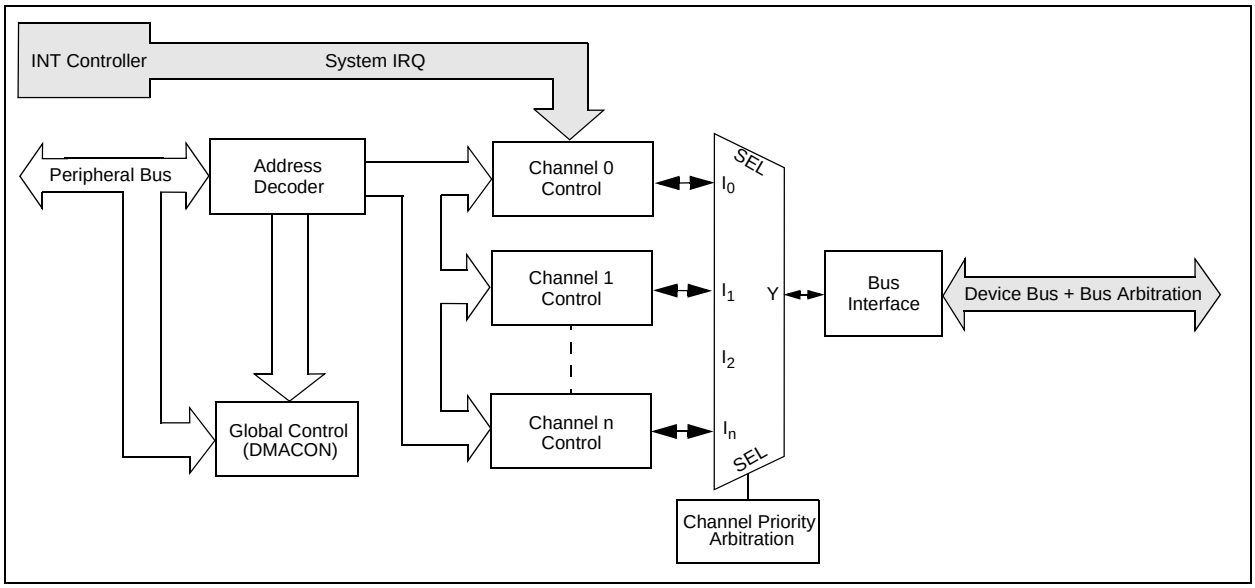
**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The PIC32MX Direct Memory Access (DMA) controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the PIC32MX (such as Peripheral Bus (PBUS) devices: SPI, UART, PMP, and so on) or memory itself.

Following are some of the key features of the DMA controller module:

- Four Identical Channels, each featuring:
  - Auto-Increment Source and Destination Address Registers
  - Source and Destination Pointers
  - Memory to Memory and Memory to Peripheral Transfers
- Automatic Word-Size Detection:
  - Transfer Granularity, down to byte level
  - Bytes need not be word-aligned at source and destination
- Fixed Priority Channel Arbitration
- Flexible DMA Channel Operating Modes:
  - Manual (software) or automatic (interrupt) DMA requests
  - One-Shot or Auto-Repeat Block Transfer modes
  - Channel-to-channel chaining
- Flexible DMA Requests:
  - A DMA request can be selected from any of the peripheral interrupt sources
  - Each channel can select any (appropriate) observable interrupt as its DMA request source
  - A DMA transfer abort can be selected from any of the peripheral interrupt sources
  - Pattern (data) match transfer termination
- Multiple DMA Channel Status Interrupts:
  - DMA channel block transfer complete
  - Source empty or half empty
  - Destination full or half-full
  - DMA transfer aborted due to an external event
  - Invalid DMA address generated
- DMA Debug Support Features:
  - Most recent address accessed by a DMA channel
  - Most recent DMA channel to transfer data
- CRC Generation Module:
  - CRC module can be assigned to any of the available channels
  - CRC module is highly configurable

**FIGURE 10-1: DMA BLOCK DIAGRAM**



## 16.0 OUTPUT COMPARE

**Note 1:** This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. "Output Compare"** (DS61111) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

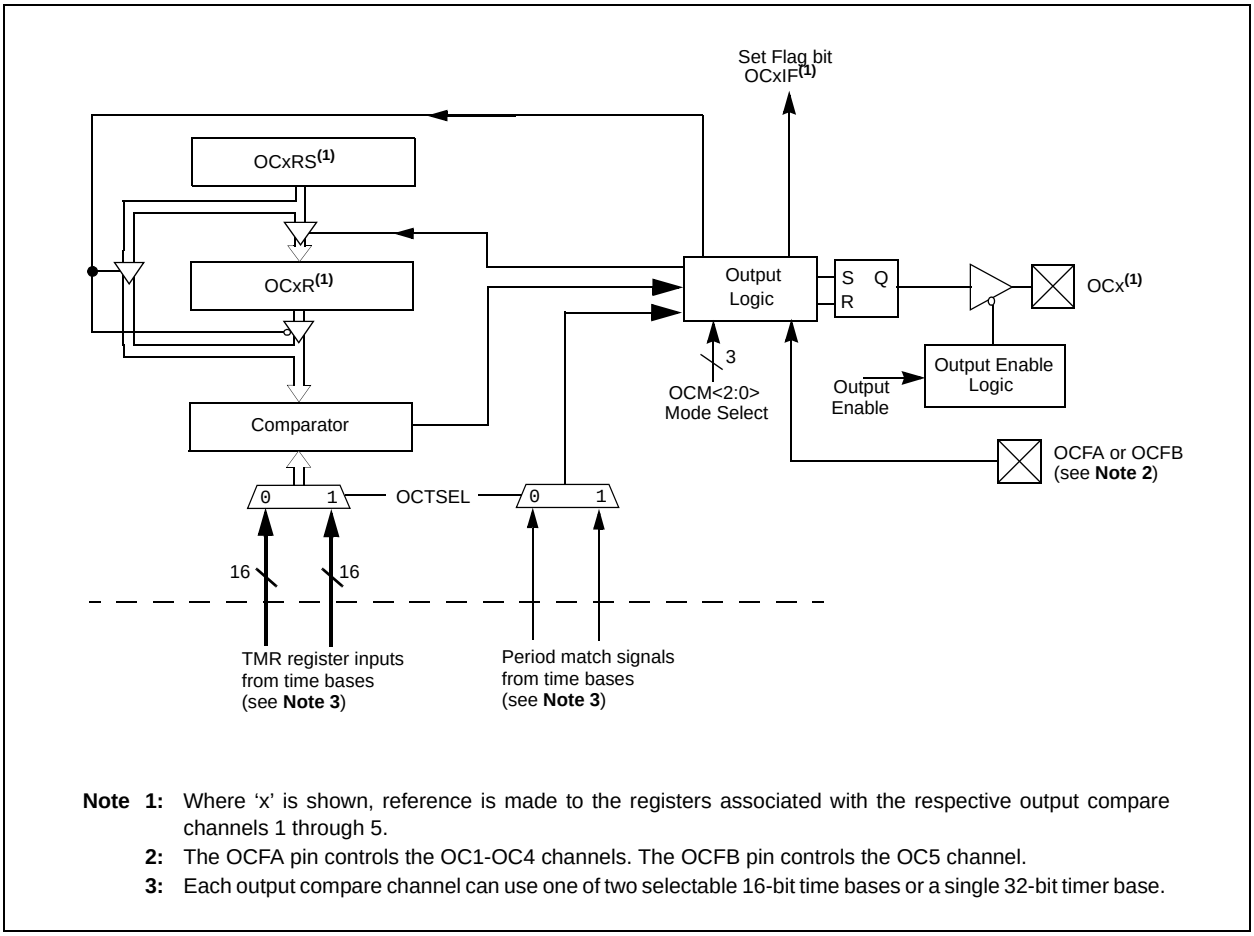
**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Output Compare module (OCMP) is used to generate a single pulse or a train of pulses in response to selected time base events. For all modes of operation, the OCMP module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the OCMP module generates an event based on the selected mode of operation.

The following are some of the key features:

- Multiple output compare modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Programmable selection of 16-bit or 32-bit time bases.
- Can operate from either of two available 16-bit time bases or a single 32-bit time base

**FIGURE 16-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM**

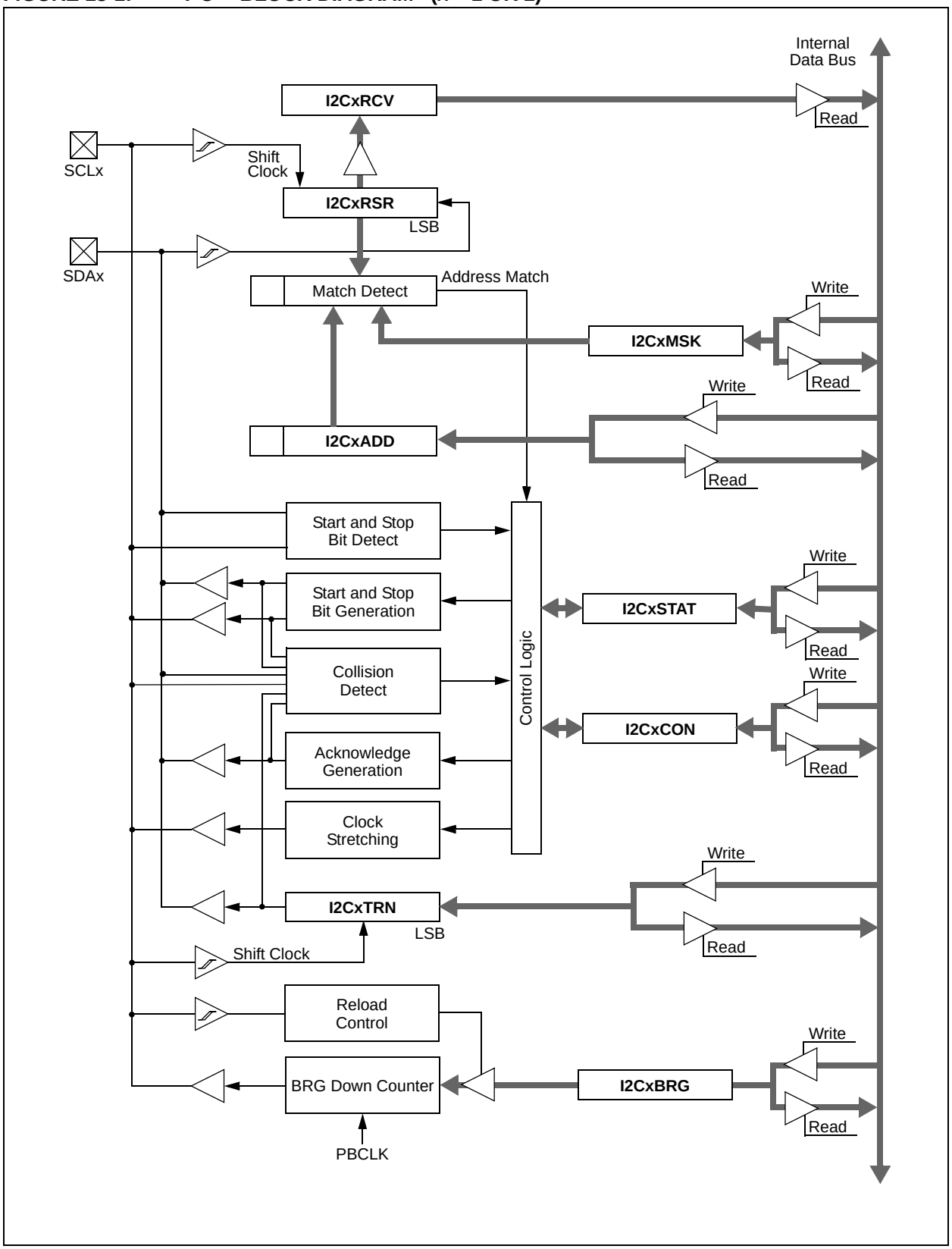



**Note 1:** Where 'x' is shown, reference is made to the registers associated with the respective output compare channels 1 through 5.

**2:** The OCFA pin controls the OC1-OC4 channels. The OCFB pin controls the OC5 channel.

**3:** Each output compare channel can use one of two selectable 16-bit time bases or a single 32-bit timer base.

**FIGURE 18-1: I²C™ BLOCK DIAGRAM (X = 1 OR 2)**



## 21.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

**Note 1:** This data sheet summarizes the features of the PIC32MX3XX/4XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS61125) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

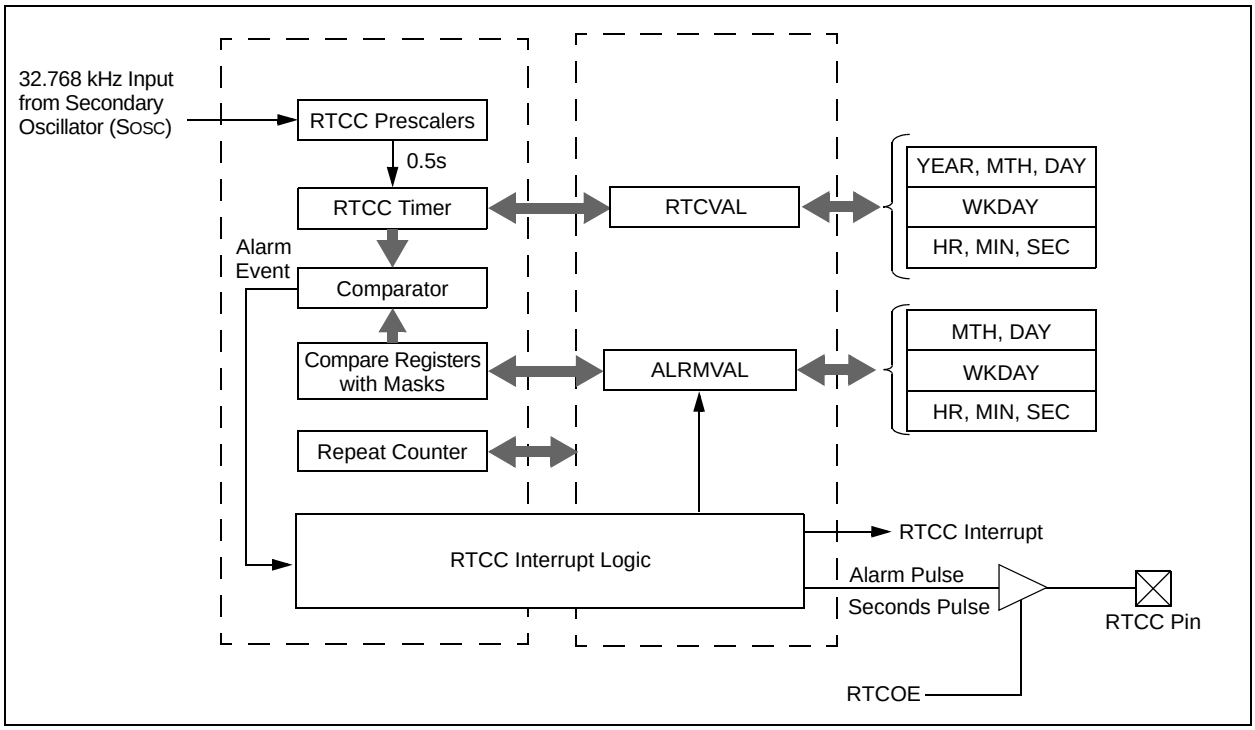
**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The PIC32MX RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

The following are some of the key features of this module:

- Time: Hours, Minutes and Seconds
- 24-Hour Format (Military Time)
- Visibility of One-Half-Second Period
- Provides Calendar: Weekday, Date, Month and Year
- Alarm Intervals are configurable for Half of a Second, One Second, 10 Seconds, One Minute, 10 Minutes, One Hour, One Day, One Week, One Month and One Year
- Alarm Repeat with Decrementing Counter
- Alarm with Indefinite Repeat: Chime
- Year Range: 2000 to 2099
- Leap Year Correction
- BCD Format for Smaller Firmware Overhead
- Optimized for Long-Term Battery Operation
- Fractional Second Synchronization
- User Calibration of the Clock Crystal Frequency with Auto-Adjust
- Calibration Range: ±0.66 Seconds Error per Month
- Calibrates up to 260 ppm of Crystal Error
- Requirements: External 32.768 kHz Clock Crystal
- Alarm Pulse or Seconds Clock Output on RTCC pin

**FIGURE 21-1: RTCC BLOCK DIAGRAM**



## 29.1 DC Characteristics

**TABLE 29-1: OPERATING MIPS VS. VOLTAGE**

| Characteristic | VDD Range (in Volts) | Temp. Range (in °C) | Max. Frequency |
|---|---|---|---|
| | | | PIC32MX3XX/4XX |
| DC5 | 2.3V-3.6V | -40°C to +85°C | 80 MHz **(Note 1)** |
| DC5b | 2.3V-3.6V | -40°C to +105°C | 80 MHz **(Note 1)** |

**Note 1:** 40 MHz maximum for PIC32MX320F032H and PIC32MX420F032H devices.

**TABLE 29-2: THERMAL OPERATING CONDITIONS**

| Rating | Symbol | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|
| **Industrial Temperature Devices** | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +125 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +85 | °C |
| **V-Temp Temperature Devices** | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +140 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +105 | °C |
| Power Dissipation:<br>Internal Chip Power Dissipation:<br>PINT = VDD x (IDD – S IOH)<br>I/O Pin Power Dissipation:<br>I/O = S ({VDD – VOH} x IOH) + S (VOL x IOL)) | PD | PINT + PI/O | | | W |
| Maximum Allowed Power Dissipation | PDMAX | (TJ – TA)/θJA | | | W |

**TABLE 29-3: THERMAL PACKAGING CHARACTERISTICS**

| Characteristics | Symbol | Typical | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Package Thermal Resistance, 121-Pin XBGA (10x10x1.1 mm) | θJA | 40 | — | °C/W | **1** |
| Package Thermal Resistance, 100-Pin TQFP (12x12x1 mm) | θJA | 43 | — | °C/W | **1** |
| Package Thermal Resistance, 64-Pin TQFP (10x10x1 mm) | θJA | 47 | — | °C/W | **1** |
| Package Thermal Resistance, 64-Pin QFN (9x9x0.9 mm) | θJA | 28 | — | °C/W | **1** |

**Note 1:** Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

**TABLE 29-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| **Operating Voltage** | | | | | | | |
| DC10 | VDD | **Supply Voltage** | 2.3 | — | 3.6 | V | — |
| DC12 | VDR | **RAM Data Retention Voltage (Note 1)** | 1.75 | — | — | V | — |
| DC16 | VPOR | **VDD Start Voltage** to Ensure Internal Power-on Reset Signal | 1.75 | — | 1.95 | V | — |
| DC17 | SVDD | **VDD Rise Rate** to Ensure Internal Power-on Reset Signal | 0.05 | — | — | V/ms | — |

**Note 1:** This is the limit to which VDD can be lowered without losing RAM data.

**TABLE 29-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| | VIL | **Input Low Voltage** | | | | | |
| DI10 | | I/O pins: | | | | | |
| | | with TTL Buffer | VSS | — | 0.15 VDD | V | **(Note 4)** |
| | | with Schmitt Trigger Buffer | VSS | — | 0.2 VDD | V | **(Note 4)** |
| DI15 | | $\overline{MCLR}$ | VSS | — | 0.2 VDD | V | **(Note 4)** |
| DI16 | | OSC1 (XT mode) | VSS | — | 0.2 VDD | V | **(Note 4)** |
| DI17 | | OSC1 (HS mode) | VSS | — | 0.2 VDD | V | **(Note 4)** |
| DI18 | | SDAx, SCLx | VSS | — | 0.3 VDD | V | SMBus disabled **(Note 4)** |
| DI19 | | SDAx, SCLx | VSS | — | 0.8 | V | SMBus enabled **(Note 4)** |
| | VIH | **Input High Voltage** | | | | | |
| DI20 | | I/O pins: | | | | | |
| | | with Analog Functions | 0.8 VDD | — | VDD | V | **(Note 4)** |
| | | Digital Only | 0.8 VDD | — | | V | **(Note 4)** |
| | | with TTL Buffer | 0.25VDD + 0.8V | — | 5.5 | V | **(Note 4)** |
| | | with Schmitt Trigger Buffer | 0.8 VDD | — | 5.5 | V | **(Note 4)** |
| DI25 | | $\overline{MCLR}$ | 0.8 VDD | — | VDD | V | **(Note 4)** |
| DI26 | | OSC1 (XT mode) | 0.7 VDD | — | VDD | V | **(Note 4)** |
| DI27 | | OSC1 (HS mode) | 0.7 VDD | — | VDD | V | **(Note 4)** |
| DI28 | | SDAx, SCLx | 0.7 VDD | — | 5.5 | V | SMBus disabled **(Note 4)** |
| DI29 | | SDAx, SCLx | 2.1 | — | 5.5 | V | SMBus enabled, 2.3V ≤VPIN ≤5.5 **(Note 4)** |
| DI30 | ICNPU | **CNxx Pull up Current** | 50 | 250 | 400 | µA | VDD = 3.3V, VPIN = VSS |
| | IIL | **Input Leakage Current** | | | | | **(Note 3)** |
| DI50 | | I/O Ports | — | — | ±1 | µA | VSS ≤VPIN ≤VDD, Pin at high-impedance |
| DI51 | | Analog Input Pins | — | — | ±1 | µA | VSS ≤VPIN ≤VDD, Pin at high-impedance |
| DI55 | | $\overline{MCLR}$ | — | — | ±1 | µA | VSS ≤VPIN ≤VDD |
| DI56 | | OSC1 | — | — | ±1 | µA | VSS ≤VPIN ≤VDD, XT and HS modes |

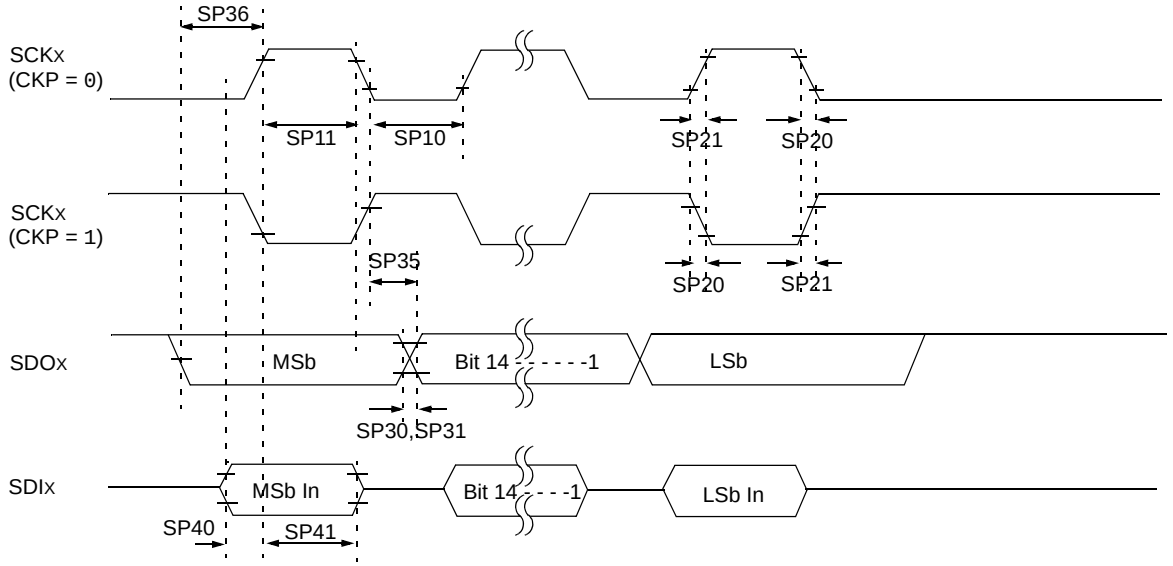
**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as current sourced by the pin.

**4:** This parameter is characterized, but not tested in manufacturing.

**FIGURE 29-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 29-1 for load conditions.

**TABLE 29-29: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | TscL | SCKx Output Low Time(3) | Tsck/2 | — | — | ns | — |
| SP11 | TscH | SCKx Output High Time(3) | Tsck/2 | — | — | ns | — |
| SP20 | TscF | SCKx Output Fall Time(4) | — | — | — | ns | See parameter DO32 |
| SP21 | TscR | SCKx Output Rise Time(4) | — | — | — | ns | See parameter DO31 |
| SP30 | TdoF | SDOx Data Output Fall Time(4) | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time(4) | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 15 | ns | VDD > 2.7V |
| | | | — | — | 20 | ns | VDD < 2.7V |
| SP36 | TdoV2sc, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 15 | — | — | ns | — |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 15 | — | — | ns | VDD > 2.7V |
| | | | 20 | — | — | ns | VDD < 2.7V |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 15 | — | — | ns | VDD > 2.7V |
| | | | 20 | — | — | ns | VDD < 2.7V |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

**FIGURE 29-23: EJTAG TIMING CHARACTERISTICS**

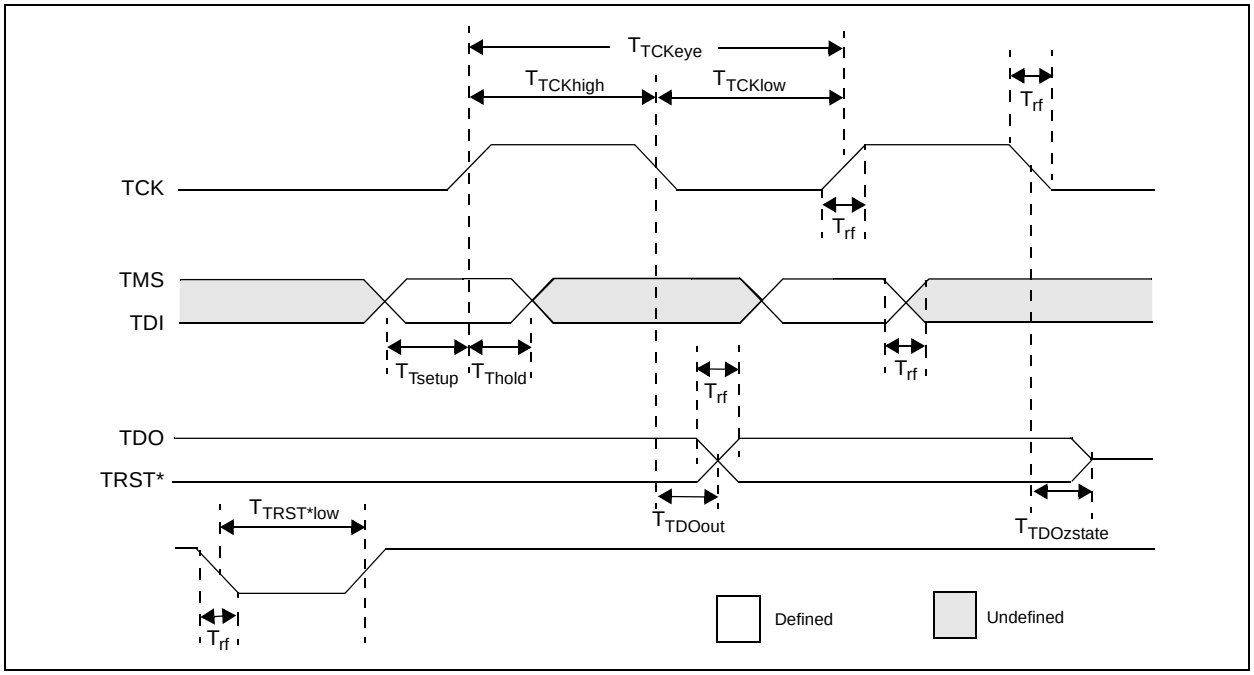


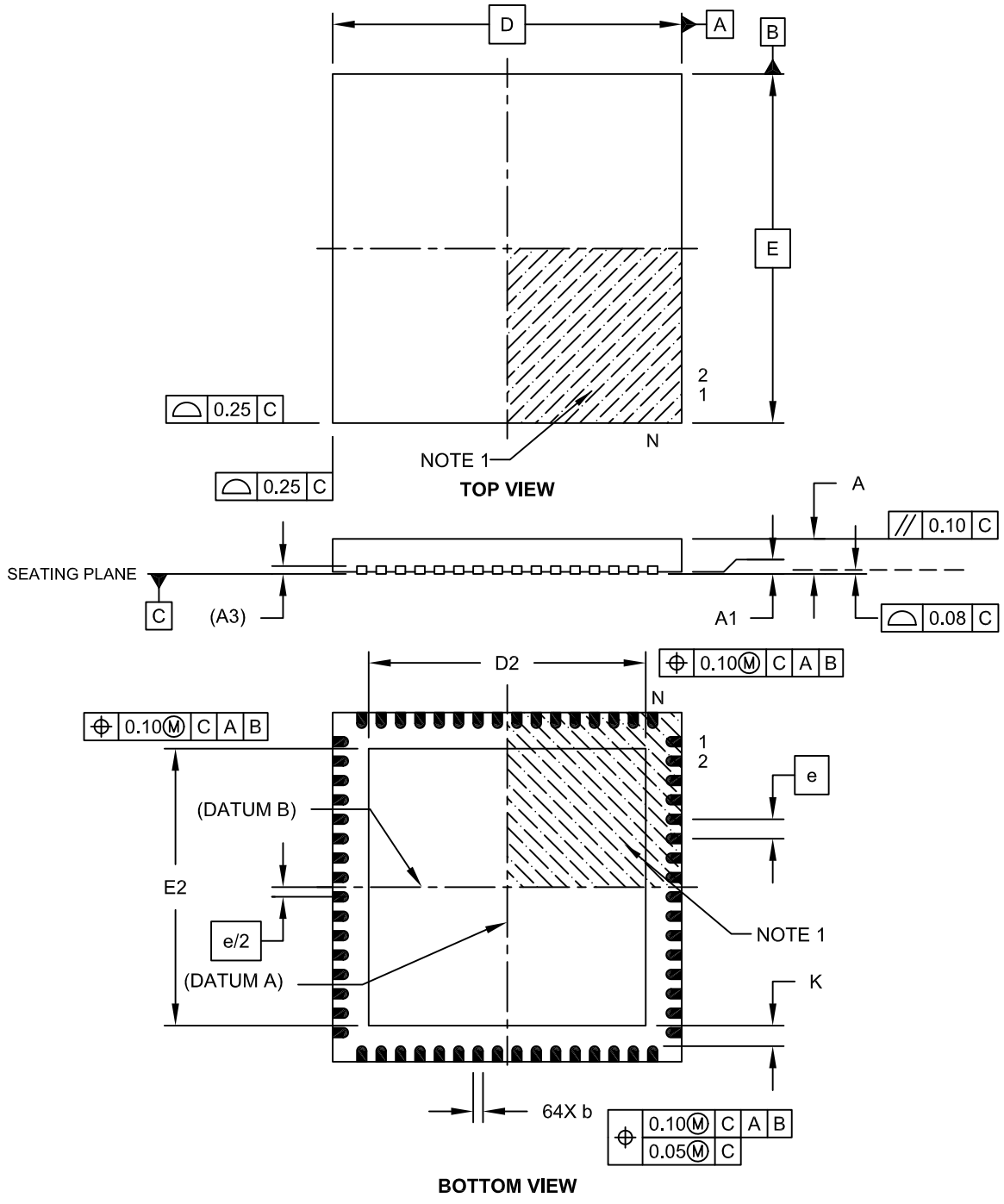

**TABLE 29-41: EJTAG TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+105°C for V-Temp | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Description(1)** | **Min.** | **Max.** | **Units** | **Conditions** |
| EJ1 | TTCKCYC | TCK Cycle Time | 25 | — | ns | — |
| EJ2 | TTCKHIGH | TCK High Time | 10 | — | ns | — |
| EJ3 | TTCKLOW | TCK Low Time | 10 | — | ns | — |
| EJ4 | TTSETUP | TAP Signals Setup Time Before Rising TCK | 5 | — | ns | — |
| EJ5 | TTHOLD | TAP Signals Hold Time After Rising TCK | 3 | — | ns | — |
| EJ6 | TTDOOUT | TDO Output Delay Time from Falling TCK | — | 5 | ns | — |
| EJ7 | TTDOZSTATE | TDO 3-State Delay Time from Falling TCK | — | 5 | ns | — |
| EJ8 | TTRSTLOW | TRST Low Time | 25 | — | ns | — |
| EJ9 | TRF | TAP Signals Rise/Fall Time, All Input and Output | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]**
**With 7.15 x 7.15 Exposed Pad [QFN]**

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




Microchip Technology Drawing C04-149C Sheet 1 of 2