

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFl

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	•
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx440f512h-80v-mr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 2: PIC32MX USB – FEATURES

					US	SB									
Device	Pins	Packages ⁽²⁾	MHz	Program Memory (KB)	Data Memory (KB)	Timers/Capture/Compare	Programmable DMA Channels	Dedicated USB DMA Channels	VREG	Trace	EUART/SPI/I ² C™	10-bit ADC (ch)	Comparators	PMP/PSP	JTAG
PIC32MX420F032H	64	PT, MR	40	32 + 12 ⁽¹⁾	8	5/5/5	0	2	Yes	No	2/1/2	16	2	Yes	Yes
PIC32MX440F128H	64	PT, MR	80	128 + 12 ⁽¹⁾	32	5/5/5	4	2	Yes	No	2/1/2	16	2	Yes	Yes
PIC32MX440F256H	64	PT, MR	80	256 + 12 ⁽¹⁾	32	5/5/5	4	2	Yes	No	2/1/2	16	2	Yes	Yes
PIC32MX440F512H	64	PT, MR	80	512 + 12 ⁽¹⁾	32	5/5/5	4	2	Yes	No	2/1/2	16	2	Yes	Yes
	100	PT		(1)											
PIC32MX440F128L	121	BG	80	128 + 12 ⁽¹⁾	32	5/5/5	4	2	Yes	No	2/2/2	16	2	Yes	Yes
	100	PT													
PIC32MX460F256L	121	BG	80	256 + 12 ⁽¹⁾	32	5/5/5	4	2	Yes	Yes	2/2/2	16	2	Yes	Yes
	100	PT													
PIC32MX460F512L	121	BG	80	512 + 12 ⁽¹⁾	32	5/5/5	4	2	Yes	Yes	2/2/2	16	2	Yes	Yes

Legend: PT = TQFP MR = QFN BG = XBGA

Note 1: This device features 12 KB Boot Flash memory.

2: See Legend for an explanation of the acronyms. See Section 30.0 "Packaging Information" for details.

Pin Diagrams (Continued)



NOTES:

3.3 Power Management

The MIPS32[®] M4K[®] Processor Core offers a number of power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or halting the clocks, which reduces system power consumption during idle periods.

3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking power-down mode is through execution of the WAIT instruction. For more information on power management, see Section 25.0 "Power-Saving Features".

3.3.2 LOCAL CLOCK GATING

The majority of the power consumed by the PIC32MX3XX/4XX family core is in the clock tree and clocking registers. The PIC32MX family uses extensive use of local gated-clocks to reduce this dynamic power consumption.

3.4 EJTAG Debug Support

The MIPS32[®] M4K[®] Processor Core provides for an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard user mode and kernel modes of operation, the core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a debug exception return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define what registers are selected and how they are used.

TABLE 4-27: PORTE REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L, PIC32MX360F512L, PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY⁽¹⁾

ess										Bi	ts								
Virtual Addr (BF88_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6100	TDICE	31:16	_	-	-	—	—	-	—		—	-		-	—	—	_	—	0000
0100	TRISE	15:0	-	_	—	—	—	—	TRISE9	TRISE8	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	03FF
6110	DODTE	31:16	—	_	_	—	—	_	—	—	—	—	—	—	—	—	_	_	0000
6110	PURIE	15:0	—	—	—	—	—	_	RE9	RE8	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
6100		31:16	_	_	—	—	—	—	—	—	_	—	—	—	—	—	—	—	0000
6120	LATE	15:0	—	_	_	—	—	_	LATE9	LATE8	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
6120	ODCE	31:16	-	_	—	—	—	—	—	—	_	—	—	—	—	—	—	—	0000
0130	ODCE	15:0	_	_	_	_	_		ODCE9	ODCE8	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

PORTE REGISTERS MAP FOR PIC32MX320F032H, PIC32MX320F064H, PIC32MX320F128H, PIC32MX340F128H, **TABLE 4-28:** PIC32MX340F256H, PIC32MX340F512H, PIC32MX420F032H, PIC32MX440F128H, PIC32MX440F256H AND PIC32MX440F512H **DEVICES ONLY⁽¹⁾**

ess										В	its								
Virtual Addr (BF88_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6100	TDICE	31:16	_	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0100	IRISE	15:0	_	—	—	—	—	—	—	_	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	00FF
6110	DODTE	31:16	—	—	—	_	_	_	—	—	_	_	_	—	—	_	_	_	0000
6110	PURIE	15:0	_	—	—	—	—	—	—	—	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
6120		31:16	—	—	—	_	_	_	—	—	_	_	_	—	—	_	_	_	0000
0120	LATE	15:0	—	—	—	_	_	_	—	—	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
6120	ODCE	31:16	_	—	—	_	_	—	—	_	—	—	—	—	—	—	—	—	0000
0130	ODCE	15:0	_	—	—				—	_	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000

Legend

unimplemented, read as '0'. Reset values are shown in hexadecimal

All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more Note 1: information.

TABLE 4-29: PORTF REGISTERS MAP FOR PIC32MX320F128L, PIC32MX340F128L, PIC32MX360F256L AND PIC32MX360F512L DEVICES ONLY⁽¹⁾

ess										В	its								
Virtual Addr (BF88_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6140	TDICE	31:16		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0140	TRISE	15:0	—	_	TRISF13	TRISF12	—	—	_	TRISF8	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	31FF
6150	DODTE	31:16	_	_	-	—	—	—	_	—	—	—	—	—	—	—	—	_	0000
0150	FURIF	15:0	—	_	RF13	RF12	—	—	_	RF8	RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
6160		31:16	—	_	—	—	—	—	_	_	_	—	—	—	—	_	_	_	0000
0100	LAIF	15:0	—	—	LATF13	LATF12	—	—	—	LATF8	LATF7	LATF6	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
6170	ODCE	31:16	—		—	—	—	—	—		—	—	—	—	—	—	—		0000
0170	ODCF	15:0	_	_	ODCF13	ODCF12	—	—	_	ODCF8	ODCF7	ODCF6	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-30: PORTF REGISTERS MAP FOR PIC32MX440F128L, PIC32MX460F256L AND PIC32MX460F512L DEVICES ONLY⁽¹⁾

ess										Bi	its								
Virtual Addr (BF88_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6140	TDICE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0140	TRISE	15:0	—	—	TRISF13	TRISF12	—	—	_	TRISF8	—	—	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	313F
6150	DODTE	31:16	—	—	_	—	—	_	_	_	—	—	—	—	—	—	—	—	0000
0150	FURIF	15:0	—	-	RF13	RF12	-	-	_	RF8	-	-	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
6160		31:16	—	—	_	—	—	—	_	_	—	—	—	—	—	—	—	_	0000
0100	LAIF	15:0	—	—	LATF13	LATF12	—	_	_	LATF8	—	—	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
6170	ODCE	31:16	_	_	—	—	—	_	_	—	—	—	—	—	—	_	_	—	0000
0170	ODCF	15:0	_	_	ODCF13	ODCF12	—	_		ODCF8	—	—	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.1.1 "CLR, SET and INV Registers" for more information.

TABLE 4-42: DEVICE AND REVISION ID SUMMARY

ess										В	ts								ő
Virtual Addr (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
5000		31:16		VER	<3:0>							DEVID	<27:16>						xxxx
F220	DEVID	15:0								DEVID	<15:0>								xxxx
Legend	1: x = u	nknowr	value on R	eset, = ur	nimplemente	d, read as '0	'. Reset valu	ues are shov	vn in hexade	ecimal.									

NOTES:

TABLE 7-1: INTERRUPT IRQ AND VECTOR LOCATION

Interrupt Source ⁽¹⁾	IRQ	Vector Number		Interrupt	Bit Location	
Highest Natural Order F	Priority		Flag	Enable	Priority	Subpriority
CT – Core Timer Interrupt	0	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>
CS0 – Core Software Interrupt 0	1	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>
CS1 – Core Software Interrupt 1	2	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>
INT0 – External Interrupt 0	3	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>
T1 – Timer1	4	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>
IC1 – Input Capture 1	5	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>
OC1 – Output Compare 1	6	6	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>
INT1 – External Interrupt 1	7	7	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>
T2 – Timer2	8	8	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>
IC2 – Input Capture 2	9	9	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>
OC2 – Output Compare 2	10	10	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>
INT2 – External Interrupt 2	11	11	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>
T3 – Timer3	12	12	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>
IC3 – Input Capture 3	13	13	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>
OC3 – Output Compare 3	14	14	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>
INT3 – External Interrupt 3	15	15	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>
T4 – Timer4	16	16	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>
IC4 – Input Capture 4	17	17	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>
OC4 – Output Compare 4	18	18	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>
INT4 – External Interrupt 4	19	19	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>
T5 – Timer5	20	20	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>
IC5 – Input Capture 5	21	21	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>
OC5 – Output Compare 5	22	22	IFS0<22>	IEC0<22>	IPC5<20:18>	IPC5<17:16>
SPI1E – SPI1 Fault	23	23	IFS0<23>	IEC0<23>	IPC5<28:26>	IPC5<25:24>
SPI1TX – SPI1 Transfer Done	24	23	IFS0<24>	IEC0<24>	IPC5<28:26>	IPC5<25:24>
SPI1RX – SPI1 Receive Done	25	23	IFS0<25>	IEC0<25>	IPC5<28:26>	IPC5<25:24>
U1E – UART1 Error	26	24	IFS0<26>	IEC0<26>	IPC6<4:2>	IPC6<1:0>
U1RX – UART1 Receiver	27	24	IFS0<27>	IEC0<27>	IPC6<4:2>	IPC6<1:0>
U1TX – UART1 Transmitter	28	24	IFS0<28>	IEC0<28>	IPC6<4:2>	IPC6<1:0>
I2C1B – I2C1 Bus Collision Event	29	25	IFS0<29>	IEC0<29>	IPC6<12:10>	IPC6<9:8>
I2C1S – I2C1 Slave Event	30	25	IFS0<30>	IEC0<30>	IPC6<12:10>	IPC6<9:8>
I2C1M – I2C1 Master Event	31	25	IFS0<31>	IEC0<31>	IPC6<12:10>	IPC6<9:8>
CN – Input Change Interrupt	32	26	IFS1<0>	IEC1<0>	IPC6<20:18>	IPC6<17:16>
AD1 – ADC1 Convert Done	33	27	IFS1<1>	IEC1<1>	IPC6<28:26>	IPC6<25:24>
PMP – Parallel Master Port	34	28	IFS1<2>	IEC1<2>	IPC7<4:2>	IPC7<1:0>
CMP1 – Comparator Interrupt	35	29	IFS1<3>	IEC1<3>	IPC7<12:10>	IPC7<9:8>
CMP2 – Comparator Interrupt	36	30	IFS1<4>	IEC1<4>	IPC7<20:18>	IPC7<17:16>

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: "PIC32MX General Purpose – Features" and TABLE 2: "PIC32MX USB – Features" for available peripherals.

Interrupt Source ⁽¹⁾	IRQ	Vector Number		Interrupt	Bit Location				
Highest Natural Order F	Priority		Flag	Enable	Priority	Subpriority			
SPI2E – SPI2 Fault	37	31	IFS1<5>	IEC1<5>	IPC7<28:26>	IPC7<25:24>			
SPI2TX – SPI2 Transfer Done	38	31	IFS1<6>	IEC1<6>	IPC7<28:26>	IPC7<25:24>			
SPI2RX – SPI2 Receive Done	39	31	IFS1<7>	IEC1<7>	IPC7<28:26>	IPC7<25:24>			
U2E – UART2 Error	40	32	IFS1<8>	IEC1<8>	IPC8<4:2>	IPC8<1:0>			
U2RX – UART2 Receiver	41	32	IFS1<9>	IEC1<9>	IPC8<4:2>	IPC8<1:0>			
U2TX – UART2 Transmitter	42	32	IFS1<10>	IEC1<10>	IPC8<4:2>	IPC8<1:0>			
I2C2B – I2C2 Bus Collision Event	43	33	IFS1<11>	IEC1<11>	IPC8<12:10>	IPC8<9:8>			
I2C2S – I2C2 Slave Event	44	33	IFS1<12>	IEC1<12>	IPC8<12:10>	IPC8<9:8>			
I2C2M – I2C2 Master Event	45	33	IFS1<13>	IEC1<13>	IPC8<12:10>	IPC8<9:8>			
FSCM – Fail-Safe Clock Monitor	46	34	IFS1<14>	IEC1<14>	IPC8<20:18>	IPC8<17:16>			
RTCC – Real-Time Clock and Calendar	47	35	IFS1<15>	IEC1<15>	IPC8<28:26>	IPC8<25:24>			
DMA0 – DMA Channel 0	48	36	IFS1<16>	IEC1<16>	IPC9<4:2>	IPC9<1:0>			
DMA1 – DMA Channel 1	49	37	IFS1<17>	IEC1<17>	IPC9<12:10>	IPC9<9:8>			
DMA2 – DMA Channel 2	50	38	IFS1<18>	IEC1<18>	IPC9<20:18>	IPC9<17:16>			
DMA3 – DMA Channel 3	51	39	IFS1<19>	IEC1<19>	IPC9<28:26>	IPC9<25:24>			
FCE – Flash Control Event	56	44	IFS1<24>	IEC1<24>	IPC11<4:2>	IPC11<1:0>			
USB	57	45	IFS1<25>	IEC1<25>	IPC11<12:10>	IPC11<9:8>			
Lowest Natural Order Priority									

TABLE 7-1: INTERRUPT IRQ AND VECTOR LOCATION (CONTINUED)

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: "PIC32MX General Purpose – Features" and TABLE 2: "PIC32MX USB – Features" for available peripherals.







FIGURE 19-5: UART RECEPTION WITH RECEIVE OVERRUN



26.3 On-Chip Voltage Regulator

All PIC32MX3XX/4XX device's core and digital logic are designed to operate at a nominal 1.8V. To simplify system designs, most devices in the PIC32MX3XX/4XX incorporate an on-chip regulator providing the required core logic voltage from VDD.

The internal 1.8V regulator is controlled by the ENVREG pin. Tying this pin to VDD enables the regulator, which in turn provides power to the core. A low ESR capacitor (such as tantalum) must be connected to the VCORE/VCAP pin (Figure 26-2). This helps to maintain the stability of the regulator. The recommended value for the filer capacitor is provided in **Section 29.1 "DC Characteristics"**.

Note:	It is important that the low ESR capacitor
	is placed as close as possible to the
	VCORE/VCAP pin.

Tying the ENVREG pin to Vss disables the regulator. In this case, separate power for the core logic at a nominal 1.8V must be supplied to the device on the VCORE/VCAP pin.

Alternatively, the VCORE/VCAP and VDD pins can be tied together to operate at a lower nominal voltage. Refer to Figure 26-2 for possible configurations.

26.3.1 ON-CHIP REGULATOR AND POR

When the voltage regulator is enabled, it takes fixed delay for it to generate output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

If the regulator is disabled, a separate Power-up Timer (PWRT) is automatically enabled. The PWRT adds a fixed delay of TPWRT at device start-up. See **Section 29.0 "Electrical Characteristics"** for more information on TPU AND TPWRT.

26.3.2 ON-CHIP REGULATOR AND BOR

When the on-chip regulator is enabled, PIC32MX3XX/4XX devices also have a simple brownout capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **Section 29.1** "**DC Characteristics**".

26.3.3 POWER-UP REQUIREMENTS

The on-chip regulator is designed to meet the power-up requirements for the device. If the application does not use the regulator, then strict power-up conditions must be adhered to. While powering up, VCORE must never exceed VDD by 0.3 volts.

FIGURE 26-2: CONNECTIONS FOR THE ON-CHIP REGULATOR



Instruction	Description	Function
TGE	Trap if Greater Than or Equal	if (int)Rs >= (int)Rt TrapException
TGEI	Trap if Greater Than or Equal Immediate	<pre>if (int)Rs >= (int)Immed TrapException</pre>
TGEIU	Trap if Greater Than or Equal Immediate Unsigned	<pre>if (uns)Rs >= (uns)Immed TrapException</pre>
TGEU	Trap if Greater Than or Equal Unsigned	<pre>if (uns)Rs >= (uns)Rt TrapException</pre>
TLT	Trap if Less Than	if (int)Rs < (int)Rt TrapException
TLTI	Trap if Less Than Immediate	if (int)Rs < (int)Immed TrapException
TLTIU	Trap if Less Than Immediate Unsigned	if (uns)Rs < (uns)Immed TrapException
TLTU	Trap if Less Than Unsigned	if (uns)Rs < (uns)Rt TrapException
TNE	Trap if Not Equal	if Rs != Rt TrapException
TNEI	Trap if Not Equal Immediate	if Rs != (int)Immed TrapException
WAIT	Wait for Interrupt	Go to a low power mode and stall until interrupt occurs
WRPGPR	Write to GPR in Previous Shadow Set	SGPR[SRSCtl _{PSS} , Rd> = Rt
WSBH	Word Swap Bytes Within Halfwords	Rd = Rt ₂₃₁₆ Rt ₃₁₂₄ Rt ₇₀ Rt ₁₅₈
XOR	Exclusive OR	Rd = Rs ^ Rt
XORI	Exclusive OR Immediate	Rt = Rs ^ (uns)Immed

TABLE 27-1:	MIPS32 [®] INSTRUCTION SET	(CONTINUED)
IADLL ZI-I.	WIFSSZ INSTRUCTION SET	

Note 1: This instruction is deprecated and should not be used.

28.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit[™] 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows[®] programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit[™] 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

28.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

28.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM[™] and dsPICDEM[™] demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ[®] security ICs, CAN, IrDA[®], PowerSmart battery management, SEEVAL[®] evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+105°C for V-Temp				
Parameter No.	Typical ⁽²⁾	Max.	Units	Conditions			
Module Dif	ferential Cu	irrent (Cor	tinued)				
DC43	—	1100	μA	-40°C	2.5V		
DC43a	—	1100	μA	+25°C			
DC43b	—	1000	μΑ	+85°C		ADC. AIADC (Notes 3, 4, 6)	
DC43h	—	1200	μA	+105⁰C			
DC43c	880	_	μA	—	—	ADC: ΔIADC (Notes 3, 4)	
DC43e	—	1100	μA	-40°C			
DC43f	—	1100	μA	+25°C	2.61/	ADC: ΔIADC (Notes 3, 4)	
DC43g	—	1000	μA	+85°C	3.67		
DC43i	_	1200	μA	+105⁰C			

TABLE 29-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD) (CONTINUED)

Note 1: Base IPD is measured with all digital peripheral modules disabled. All I/Os are configured as inputs and pulled low. WDT and FSCM are disabled.

2: Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

4: Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

5: Data is characterized at +70°C and not tested. Parameter is for design guidance only.

6: This parameter is characterized, but not tested in manufacturing.







64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimensior	MIN	NOM	MAX	
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B

100-Lead Plastic Thin Quad Flatpack (PT)-12x12x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	Е		0.40 BSC	
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100B

Product Identification System

To order or obtain informat	tion, e.g., on pricing or delivery, refer to the factory or the li	isted sales office.		
Microchip Brand Architecture Product Groups Flash Memory Family_ Program Memory Size Pin Count Tape and Reel Flag (if Speed Temperature Range Package Pattern	PIC32 MX 3XX F 512 H T - 80 I / PT - XXX (KB) applicable)	Examples: PIC32MX320F032H-40I/PT: General purpose PIC32MX, 32 KB program memory, 64-pin, Industrial temperature, TQFP package. PIC32MX360F256L-80I/PT: General purpose PIC32MX, 256 KB program memory, 100-pin, Industrial temperature, TQFP package.		
Flash Memory Family				
Architecture	MX = 32-bit RISC MCU core			
Product Groups	3XX = General purpose microcontroller family 4XX = USB			
Flash Memory Family	F = Flash program memory			
Program Memory Size	32 = 32K 64 = 64K 128 = 128K 256 = 256K 512 = 512K			
Speed	40 = 40 MHz 80 = 80 MHz			
Pin Count	H = 64-pin L = 100-pin			
Temperature Range	I = -40° C to $+85^{\circ}$ C (Industrial) V = -40° C to $+105^{\circ}$ C (V-Temp)			
Package	PT = 64-Lead (10x10x1 mm) TQFP (Thin Quad Flatpack) PT = 100-Lead (12x12x1 mm) TQFP (Thin Quad Flatpack) MR = 64-Lead (9x9x0.9 mm) QFN (Plastic Quad Flat) BG = 121-Lead (10x10x1.1 mm) XBGA (Plastic Thin Profile Ball Grid Array)			
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES = Engineering Sample			