AMD Xilinx - XC6VHX255T-2FFG1923C Datasheet

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Details	
Product Status	Active
Number of LABs/CLBs	19800
Number of Logic Elements/Cells	253440
Total RAM Bits	19021824
Number of I/O	480
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1924-BBGA, FCBGA
Supplier Device Package	1924-FCBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vhx255t-2ffg1923c

Important Note

Typical values for quiescent supply current are specified at nominal voltage, 85°C junction temperatures (T_j). Xilinx recommends analyzing static power consumption at T_j = 85°C because the majority of designs operate near the high end of the commercial temperature range. Quiescent supply current is specified by speed grade for Virtex-6 devices. Use the XPower™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified in Table 4.

Table 4: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed and Temperature Grade						Units
			-3 (C)	-2 (C, E, & I)	-1 (C & I)	-1 (I & M)(2)	-1L (C)	-1L (I)(1)	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC6VLX75T	927	927	927	N/A	656	741	mA
		XC6VLX130T	1563	1563	1563	N/A	1102	1245	mA
		XC6VLX195T	2059	2059	2059	N/A	1441	1628	mA
		XC6VLX240T	2478	2478	2478	N/A	1733	1957	mA
		XC6VLX365T	3001	3001	3001	N/A	2092	2363	mA
		XC6VLX550T(3)	N/A	4515	4515	N/A	3147	3555	mA
		XC6VLX760(3)	N/A	5094	5094	N/A	3471	3921	mA
		XC6VSX315T	3476	3476	3476	N/A	2409	2721	mA
		XC6VSX475T(3)	N/A	5227	5227	N/A	3622	4091	mA
		XC6VHX250T	2906	2906	2906	N/A	N/A	N/A	mA
		XC6VHX255T	2746	2746	2746	N/A	N/A	N/A	mA
		XC6VHX380T(4)	4160	4160	4160	N/A	N/A	N/A	mA
		XC6VHX565T(5)	N/A	5207	5207	N/A	N/A	N/A	mA
		XQ6VLX130T	N/A	1563	N/A	1563	N/A	1245	mA
		XQ6VLX240T	N/A	2478	N/A	2478	N/A	1957	mA
		XQ6VLX550T(7)	N/A	N/A	N/A	4515	N/A	3555	mA
		XQ6VSX315T	N/A	3476	N/A	3476	N/A	2721	mA
		XQ6VSX475T(7)	N/A	N/A	N/A	5227	N/A	4091	mA

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on sequence and ramp rate of the power supply.

The recommended power-on sequence for Virtex-6 devices is V_{CCINT}, V_{CCAUX}, and V_{CCO} to meet the power-up current requirements listed in Table 5. V_{CCINT} can be powered up or down at any time, but power up current specifications can vary from Table 5. The device will have no physical damage or reliability concerns if V_{CCINT}, V_{CCAUX}, and V_{CCO} sequence cannot be followed.

If the recommended power-up sequence cannot be followed and the I/Os must remain 3-stated throughout configuration, then V_{CCAUX} must be powered prior to V_{CCO} or V_{CCAUX} and V_{CCO} must be powered by the same supply. Similarly, for power-down, the reverse V_{CCAUX} and V_{CCO} sequence is recommended if the I/Os are to remain 3-stated.

The GTH transceiver supplies must be powered using a MGTHAVCC, MGTHAVCCRX, MGTHAVCCPLL, and MGTHAVTT sequence. There are no sequencing requirement for these supplies with respect to the other FPGA supply voltages. For more detail see Table 27: *GTH Transceiver Power Supply Sequencing*. There are no sequencing requirements for the GTX transceivers power supplies.

Table 5 shows the minimum current, in addition to I_{CCQ}, that are required by Virtex-6 devices for proper power-on and configuration. If the current minimums shown in Table 4 and Table 5 are met, the device powers on after all three supplies have passed through their power-on reset threshold voltages. The FPGA must be configured after applying V_{CCINT}, V_{CCAUX}, and V_{CCO} for the appropriate configuration banks. Once initialized and configured, use the XPE tools to estimate current drain on these supplies.

Table 5: **Power-On Current for Virtex-6 Devices**

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	Units
	Typ(1)	Typ(1)	Typ(1)	
XC6VLX75T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 10	I_{CCOQ} + 30 mA per bank	mA
XC6VLX130T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 10	I_{CCOQ} + 30 mA per bank	mA
XC6VLX195T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VLX240T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VLX365T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VLX550T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VLX760	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VSX315T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VSX475T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 50	I_{CCOQ} + 30 mA per bank	mA
XC6VHX250T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VHX255T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VHX380T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VHX565T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XQ6VLX130T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 100	I_{CCOQ} + 30 mA per bank	mA
XQ6VLX240T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 100	I_{CCOQ} + 30 mA per bank	mA
XQ6VLX550T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 100	I_{CCOQ} + 30 mA per bank	mA
XQ6VSX315T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 100	I_{CCOQ} + 40 mA per bank	mA
XQ6VSX475T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 100	I_{CCOQ} + 40 mA per bank	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Use the XPower Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.

HT DC Specifications (HT_25)

Table 8: **HT DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage for XC devices	R_T = 100 Ω across Q and $\overline{Q}$ signals	480	600	885	mV
	Differential Output Voltage for XQ devices		480	600	930	mV
ΔV_{OD}	Change in V_{OD} Magnitude		–15	–	15	mV
V_{OCM}	Output Common Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	440	600	760	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		–15	–	15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		–15	–	15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		–15	–	15	mV

LVDS DC Specifications (LVDS_25)

Table 9: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage for XC devices	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
	Output Common-Mode Voltage for XQ devices		1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 10: **Extended LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.715	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High for XC devices	R_T = 100 Ω across Q and $\overline{Q}$ signals	350	–	840	mV
	Differential Output Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High for XQ devices		350	–	850	mV
V_{OCM}	Output Common-Mode Voltage for XC devices	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
	Output Common-Mode Voltage for XQ devices		1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	–	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 13: **Absolute Maximum Ratings for GTX Transceivers(1)**

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	–0.5	1.1	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	–0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 14: **Recommended Operating Conditions for GTX Transceivers(1)(2)**

Symbol	Description	Speed Grade	PLL Frequency	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	-3, -2(3)	> 2.7 GHz	1.0	1.03	1.06	V
		-3, -2(3)	≤ 2.7 GHz	0.95	1.0	1.06	V
		-1	≤ 2.7 GHz	0.95	1.0	1.06	V
		-1L	≤ 2.7 GHz	0.95	1.0	1.05	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	All	–	1.14	1.2	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	All	–	1.14	1.2	1.26	V

Notes:

1. Each voltage listed requires the filter circuit described in UG366: *Virtex-6 FPGA GTX Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +100°C for all XC devices and T_j = –55°C to +125°C for the XQ devices
3. If a GTX Quad contains transceivers operating with a mixture of PLL frequencies above and below 2.7 GHz, the MGTAVCC voltage supply must be in the range of 1.0V to 1.06V.

Table 15: **GTX Transceiver Supply Current (per Lane) (1)(2)**

Symbol	Description	Typ	Max	Units
$I_{MGTAVTT}$	MGTAVTT supply current for one GTX transceiver	55.9	Note 2	mA
$I_{MGTAVCC}$	MGTAVCC supply current for one GTX transceiver	56.1		mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	100.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
2. Values for currents of other transceiver configurations and conditions can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

Table 21: **GTX Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		62.5	–	650	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	200	µs

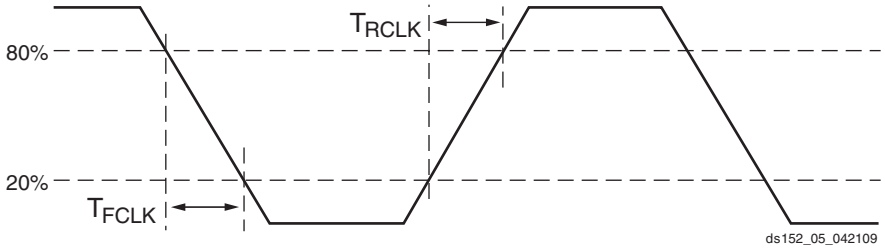

Figure 3: **Reference Clock Timing Parameters**

Table 22: **GTX Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1	-1L	
F_{TXOUT}	TXOUTCLK maximum frequency	Internal 20-bit data path	330	330	250	250	MHz
		Internal 16-bit data path	412.5	412.5	312.5	250	MHz
F_{RXREC}	RXRECCLK maximum frequency	Internal 20-bit data path	330	330	250	250	MHz
		Internal 16-bit data path	412.5	412.5	312.5	250	MHz
T_{RX}	RXUSRCLK maximum frequency		412.5(2)	412.5(2)	312.5	250	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	376	376	312.5	250	MHz
		2 byte interface	406.25	406.25	312.5	250	MHz
		4 byte interface	206.25	206.25	156.25	125	MHz
T_{TX}	TXUSRCLK maximum frequency		412.5(3)	412.5(3)	312.5	250	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	376	376	312.5	250	MHz
		2 byte interface	406.25	406.25	312.5	250	MHz
		4 byte interface	206.25	206.25	156.25	125	MHz

Notes:

1. Clocking must be implemented as described in UG366: *Virtex-6 FPGA GTX Transceivers User Guide*.
2. 406.25 MHz when the RX elastic buffer is bypassed.
3. 406.25 MHz when the TX buffer is bypassed.

Figure 4 shows the timing parameters in Table 27.

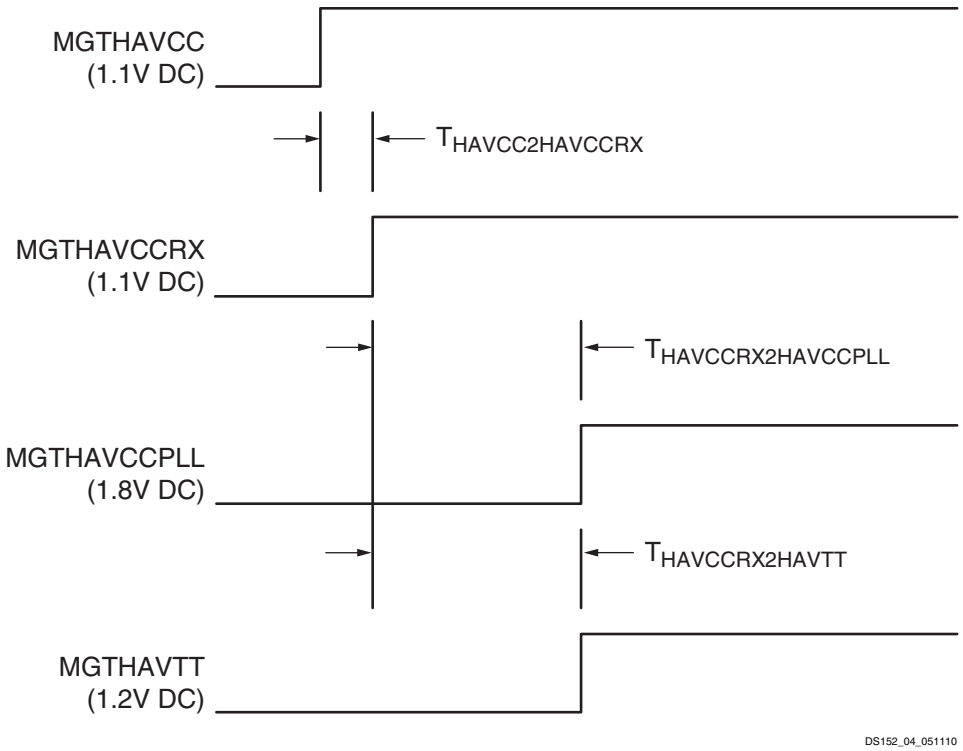

Figure 4: **GTH Transceiver Power Supply Power-On Sequencing**

Table 28: **GTH Transceiver Supply Current**

Symbol	Description	Typ(1)	Max	Units
$I_{MGTHAVCC}$	MGTHAVCC supply current for one GTH Quad (4 lanes)	571	Note 2	mA
$I_{MGTHAVCCRX}$	MGTHAVCCRX supply current for a GTH Quad (4 lanes)	254	Note 2	mA
$I_{MGTHAVTT}$	MGTHAVTT supply current for one GTH Quad (4 lanes)	93	Note 2	mA
$I_{MGTHAVCCPLL}$	MGTHAVCCPLL supply current for one GTH Quad (4 lanes)	219	Note 2	mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	1000.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 10.3125 Gb/s line rate.
2. Values for currents other than the values specified in this table can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

Table 29: **GTH Transceiver Quiescent Supply Current(1)(2)**

Symbol	Description	Typ(3)	Max	Units
$I_{MGTHAVCCQ}$	Quiescent MGTHAVCC Supply Current for one GTH Quad (4 lanes)	65	Note 4	mA
$I_{MGTHAVCCRXQ}$	Quiescent MGTHAVCCRX Supply Current for one GTH Quad (4 lanes)	17	Note 4	mA
$I_{MGTHAVTTQ}$	Quiescent MGTHAVTT Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA
$I_{MGTHAVCCPLLQ}$	Quiescent MGTHAVCCPLL Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA

Notes:

1. Device powered and unconfigured.
2. GTH transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTH transceivers.
3. Typical values are specified at nominal voltage, 25°C.
4. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.

GTH Transceiver DC Input and Output Levels

Table 30 summarizes the DC output specifications of the GTH transceivers in Virtex-6 FPGAs. Consult UG371: *Virtex-6 FPGA GTH Transceivers User Guide* for further details.

Table 30: **GTH Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
D_{VPPIN}	Differential peak-to-peak input voltage	External AC coupled	175	–	1200	mV
D_{VPPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to maximum setting	800	–	1200	mV
R_{IN}	Differential input resistance		80	100	120	Ω
R_{OUT}	Differential output resistance		80	100	120	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	–	ps
C_{EXT}	Recommended external AC coupling capacitor(2)		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG371: *Virtex-6 FPGA GTH Transceivers User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 31 summarizes the DC specifications of the clock input of the GTH transceiver. Consult UG371: *Virtex-6 FPGA GTH Transceivers User Guide* for further details.

Table 31: **GTH Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	≤ 600 MHz	500	–	1600	mV
		> 600 MHz	600	–	1600	mV
R_{IN}	Differential input resistance		80	100	120	Ω
C_{EXT}	Required external AC coupling capacitor		–	100	–	nF

GTH Transceiver Switching Characteristics

Consult UG371: *Virtex-6 FPGA GTH Transceivers User Guide* for further information.

Table 32: **GTH Transceiver Maximum Data Rate and PLL Frequency Range**

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F_{GTHMAX}	Maximum GTH transceiver data rate	PLL Output Divider = 1	11.182	11.182	10.32	Gb/s
		PLL Output Divider = 4	2.795	2.795	2.58	Gb/s
F_{GTHMIN}	Minimum GTH transceiver data rate(1)	PLL Output Divider = 1	9.92	9.92	9.92	Gb/s
		PLL Output Divider = 4	2.48	2.48	2.48	Gb/s
$F_{GPLLMAX}$	Maximum GTH PLL frequency		5.591	5.591	5.16	GHz
$F_{GPLLMIN}$	Minimum GTH PLL frequency		4.96	4.96	4.96	GHz

Notes:

1. Lower data rates can be achieved using FPGA logic based oversampling designs.

Table 33: **GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{GTHDRPCLK}$	GTHDRPCLK maximum frequency	70	70	60	MHz

Table 34: **GTH Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range	-1 speed grade	150	–	645	MHz
		-2 and -3 speed grades	150	–	700	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	CLK	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	2	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	20	µs

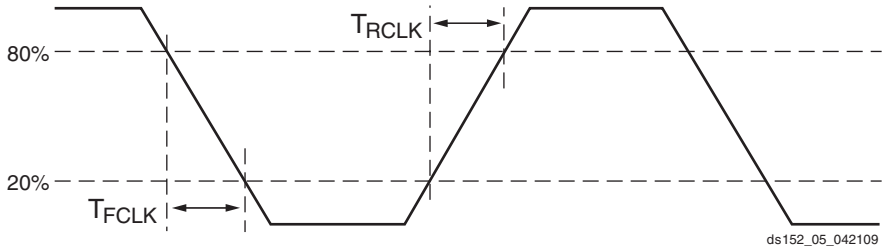

Figure 5: **Reference Clock Timing Parameters**

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

Table 39: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$F_{PIPECLK}$	Pipe clock maximum frequency	250	250	250	250	MHz
$F_{USERCLK}$	User clock maximum frequency	500	500	250	250	MHz
F_{DRPCLK}	DRP clock maximum frequency	250	250	250	250	MHz

System Monitor Analog-to-Digital Converter Specification

Table 40: **Analog-to-Digital Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
AV_{DD} = 2.5V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_j = –55°C to 125°C M-Grade, Typical values at T_j=+35°C						
DC Accuracy: All external input channels. Both unipolar and bipolar modes.						
Resolution			10	–	–	Bits
Integral Nonlinearity	INL		–	–	±1	LSBs
Differential Nonlinearity	DNL	No missing codes (T_{MIN} to T_{MAX}) Guaranteed Monotonic	–	–	±0.9	LSBs
Unipolar Offset Error (1)		Uncalibrated	–	±2	±30	LSBs
Bipolar Offset Error (1)		Uncalibrated measured in bipolar mode	–	±2	±30	LSBs
Gain Error		Uncalibrated - External Reference	–	±0.2	±2	%
		Uncalibrated - Internal Reference	–	±2	–	%
Bipolar Gain Error (1)		Uncalibrated - External Reference	–	±0.2	±2	%
		Uncalibrated - Internal Reference	–	±2	–	%
Total Unadjusted Error (Uncalibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	–	±10	–	LSBs
		Deviation from ideal transfer function. Internal reference	–	±20	–	LSBs
Total Unadjusted Error (Calibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	–	±1	±2	LSBs
Calibrated Gain Temperature Coefficient		Variation of FS code with temperature	–	±0.01	–	LSB/°C
DC Common-Mode Reject	$CMRR_{DC}$	$V_N = V_{CM}$ = 0.5V ± 0.5V, $V_P – V_N$ = 100mV	–	70	–	dB
Conversion Rate(2)						
Conversion Time - Continuous	t_{CONV}	Number of CLK cycles	26	–	32	
Conversion Time - Event	t_{CONV}	Number of CLK cycles	–	–	21	
T/H Acquisition Time	t_{ACQ}	Number of CLK cycles	4	–	–	
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	80	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
CLK Duty cycle			40	–	60	%

Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.17 for -3, -2, and -1; and v1.10 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 42 correlates the current status of each Virtex-6 device on a per speed grade basis.

Table 42: **Virtex-6 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6VLX75T			-3, -2, -1, -1L
XC6VLX130T			-3, -2, -1, -1L
XC6VLX195T			-3, -2, -1, -1L
XC6VLX240T			-3, -2, -1, -1L
XC6VLX365T			-3, -2, -1, -1L
XC6VLX550T			-2, -1, -1L
XC6VLX760			-2, -1, -1L
XC6VSX315T			-3, -2, -1, -1L
XC6VSX475T			-2, -1, -1L
XC6VHX250T			-3, -2, -1
XC6VHX255T			-3, -2, -1
XC6VHX380T			-3, -2, -1
XC6VHX565T			-2, -1
XQ6VLX130T			-2, -1, -1L
XQ6VLX240T			-2, -1, -1L
XQ6VLX550T			-1, -1L
XQ6VSX315T			-2, -1, -1L
XQ6VSX475T			-1, -1L

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 devices.

Table 45: **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVCMOS25, Fast, 16 mA	0.57	0.66	0.70	1.92	2.15	2.08	1.92	2.15	2.08	ns
LVCMOS25, Fast, 24 mA	0.57	0.66	0.70	1.79	2.15	1.96	1.79	2.15	1.96	ns
LVCMOS18, Slow, 2 mA	0.61	0.71	0.73	4.47	4.87	4.30	4.47	4.87	4.30	ns
LVCMOS18, Slow, 4 mA	0.61	0.71	0.73	2.96	3.21	2.94	2.96	3.21	2.94	ns
LVCMOS18, Slow, 6 mA	0.61	0.71	0.73	2.43	2.64	2.47	2.43	2.64	2.47	ns
LVCMOS18, Slow, 8 mA	0.61	0.71	0.73	2.11	2.41	2.24	2.11	2.41	2.24	ns
LVCMOS18, Slow, 12 mA	0.61	0.71	0.73	1.99	2.30	2.10	1.99	2.30	2.10	ns
LVCMOS18, Slow, 16 mA	0.61	0.71	0.73	1.95	2.30	2.04	1.95	2.30	2.04	ns
LVCMOS18, Fast, 2 mA	0.61	0.71	0.73	4.23	4.57	4.08	4.23	4.57	4.08	ns
LVCMOS18, Fast, 4 mA	0.61	0.71	0.73	2.76	2.97	2.74	2.76	2.97	2.74	ns
LVCMOS18, Fast, 6 mA	0.61	0.71	0.73	2.28	2.46	2.32	2.28	2.46	2.32	ns
LVCMOS18, Fast, 8 mA	0.61	0.71	0.73	1.99	2.34	2.14	1.99	2.34	2.14	ns
LVCMOS18, Fast, 12 mA	0.61	0.71	0.73	1.80	2.19	1.88	1.80	2.19	1.88	ns
LVCMOS18, Fast, 16 mA	0.61	0.71	0.73	1.74	2.18	1.88	1.74	2.18	1.88	ns
LVCMOS15, Slow, 2 mA	0.73	0.85	0.85	3.77	4.29	3.91	3.77	4.29	3.91	ns
LVCMOS15, Slow, 4 mA	0.73	0.85	0.85	2.79	3.10	2.93	2.79	3.10	2.93	ns
LVCMOS15, Slow, 6 mA	0.73	0.85	0.85	2.32	2.68	2.50	2.32	2.68	2.50	ns
LVCMOS15, Slow, 8 mA	0.73	0.85	0.85	1.98	2.29	2.24	1.98	2.29	2.24	ns
LVCMOS15, Slow, 12 mA	0.73	0.85	0.85	1.91	2.23	2.07	1.91	2.23	2.07	ns
LVCMOS15, Slow, 16 mA	0.73	0.85	0.85	1.83	2.23	1.98	1.83	2.23	1.98	ns
LVCMOS15, Fast, 2 mA	0.73	0.85	0.85	3.77	4.28	3.91	3.77	4.28	3.91	ns
LVCMOS15, Fast, 4 mA	0.73	0.85	0.85	2.53	2.78	2.66	2.53	2.78	2.66	ns
LVCMOS15, Fast, 6 mA	0.73	0.85	0.85	2.05	2.42	2.16	2.05	2.42	2.16	ns
LVCMOS15, Fast, 8 mA	0.73	0.85	0.85	1.90	2.20	2.04	1.90	2.20	2.04	ns
LVCMOS15, Fast, 12 mA	0.73	0.85	0.85	1.77	2.11	1.90	1.77	2.11	1.90	ns
LVCMOS15, Fast, 16 mA	0.73	0.85	0.85	1.76	2.11	1.92	1.76	2.11	1.92	ns
LVCMOS12, Slow, 2 mA	0.81	0.93	0.95	3.39	3.75	3.54	3.39	3.75	3.54	ns
LVCMOS12, Slow, 4 mA	0.81	0.93	0.95	2.63	2.93	2.79	2.63	2.93	2.79	ns
LVCMOS12, Slow, 6 mA	0.81	0.93	0.95	2.11	2.67	2.26	2.11	2.67	2.26	ns
LVCMOS12, Slow, 8 mA	0.81	0.93	0.95	2.02	2.25	2.17	2.02	2.25	2.17	ns
LVCMOS12, Fast, 2 mA	0.81	0.93	0.95	2.98	3.39	3.11	2.98	3.39	3.11	ns
LVCMOS12, Fast, 4 mA	0.81	0.93	0.95	2.16	2.70	2.31	2.16	2.70	2.31	ns
LVCMOS12, Fast, 6 mA	0.81	0.93	0.95	1.89	2.34	2.05	1.89	2.34	2.05	ns
LVCMOS12, Fast, 8 mA	0.81	0.93	0.95	1.82	2.10	1.98	1.82	2.10	1.98	ns
LVDCI_25	0.57	0.70	0.70	2.14	2.82	2.26	2.14	2.82	2.26	ns
LVDCI_18	0.61	0.71	0.73	2.23	2.78	2.38	2.23	2.78	2.38	ns
LVDCI_15	0.73	0.85	0.85	2.01	2.75	2.18	2.01	2.75	2.18	ns
LVDCI_DV2_25	0.57	0.70	0.70	1.83	2.37	2.00	1.83	2.37	2.00	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 47 shows the test setup parameters used for measuring input delay.

Table 47: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(5)	V_{REF} (1)(3)(5)
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III	HSTL_III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	V_{REF} – 1.00	V_{REF} + 1.00	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
HT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 6.
6. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 6 and Figure 7.

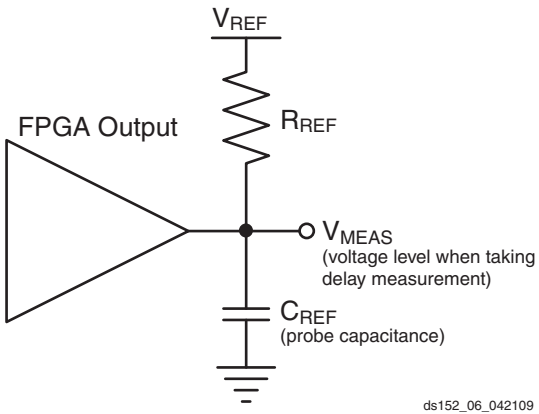

Figure 6: **Single Ended Test Setup**

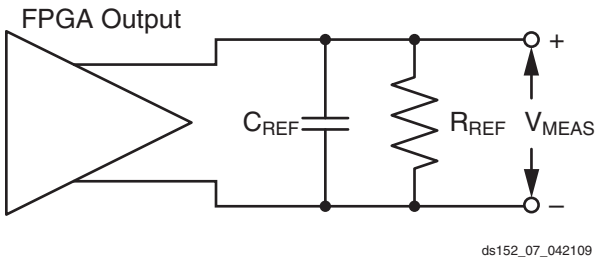

Figure 7: **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 48.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 48: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	100	0	0[2]	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDS_25	100	0	0[2]	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[2]	0

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 55: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Sequential Delays						
T_{SHCKO}	Clock to A – B outputs	0.92	1.10	1.36	1.49	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	1.19	1.40	1.71	1.87	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{DS}/T_{DH}	A – D inputs to CLK	0.62/0.18	0.72/0.20	0.88/0.22	0.98/0.23	ns, Min
T_{AS}/T_{AH}	Address An inputs to clock	0.19/0.52	0.22/0.59	0.27/0.66	0.30/0.75	ns, Min
T_{WS}/T_{WH}	WE input to clock	0.27/0.00	0.32/0.00	0.40/0.00	0.47/–0.03	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.28/–0.01	0.34/–0.01	0.41/–0.01	0.48/–0.05	ns, Min
Clock CLK						
T_{MPW}	Minimum pulse width	0.70	0.82	1.00	1.04	ns, Min
T_{MCP}	Minimum clock period	1.40	1.64	2.00	2.08	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 56: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Sequential Delays						
T_{REG}	Clock to A – D outputs	1.11	1.30	1.58	1.74	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.37	1.60	1.93	2.12	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	1.08	1.27	1.55	1.74	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{WS}/T_{WH}	WE input	0.05/0.00	0.07/0.00	0.09/0.00	0.11/0.03	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.06/–0.01	0.08/–0.01	0.10/–0.01	0.12/0.02	ns, Min
T_{DS}/T_{DH}	A – D inputs to CLK	0.64/0.18	0.76/0.21	0.94/0.24	1.07/0.23	ns, Min
Clock CLK						
T_{MPW}	Minimum pulse width	0.60	0.70	0.85	0.89	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Block RAM and FIFO Switching Characteristics

Table 57: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Block RAM and FIFO Clock-to-Out Delays						
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$[1]	Clock CLK to DOUT output (without output register)[2][3]	1.60	1.79	2.08	2.36	ns, Max
	Clock CLK to DOUT output (with output register)[4][5]	0.60	0.66	0.75	0.83	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register)[2][3]	2.62	2.89	3.30	3.73	ns, Max
	Clock CLK to DOUT output with ECC (with output register)[4][5]	0.71	0.77	0.86	0.94	ns, Max
T_{RCKO_CASC} and $T_{RCKO\_CASC\_REG}$	Clock CLK to DOUT output with Cascade (without output register)[2]	2.49	2.77	3.18	3.61	ns, Max
	Clock CLK to DOUT output with Cascade (with output register)[4]	1.29	1.41	1.58	1.79	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs[6]	0.74	0.81	0.91	0.98	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs[7]	0.90	0.98	1.09	1.21	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (with output register)	0.62	0.68	0.76	0.82	ns, Max
	Clock CLK to BITERR (without output register)	2.21	2.46	2.84	3.23	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	0.86	0.94	1.06	1.18	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.73	0.79	0.90	1.00	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.76	0.82	0.92	1.02	ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs[8]	0.47/ 0.27	0.53/ 0.29	0.62/ 0.32	0.66/ 0.34	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs[9]	0.84/ 0.30	0.95/ 0.32	1.11/ 0.34	1.26/ 0.36	ns, Min
$T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode[9]	0.47/ 0.30	0.52/ 0.32	0.59/ 0.34	0.68/ 0.36	ns, Min
	DIN inputs with block RAM ECC encode only[9]	0.68/ 0.30	0.75/ 0.32	0.85/ 0.34	0.97/ 0.36	ns, Min
	DIN inputs with FIFO ECC in standard mode[9]	0.77/ 0.30	0.87/ 0.32	1.02/ 0.34	1.16/ 0.36	ns, Min
$T_{RCCK\_CLK}/T_{RCKC\_CLK}$	Inject single/double bit error in ECC mode	0.90/ 0.27	1.02/ 0.28	1.20/ 0.29	1.56/ 0.29	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	Block RAM Enable (EN) input	0.31/ 0.26	0.35/ 0.27	0.41/ 0.30	0.44/ 0.31	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.18/ 0.25	0.19/ 0.27	0.22/ 0.31	0.24/ 0.33	ns, Min
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	Synchronous RSTREG input	0.22/ 0.23	0.24/ 0.24	0.28/ 0.26	0.31/ 0.27	ns, Min
$T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$	Synchronous RSTRAM input	0.32/ 0.23	0.36/ 0.24	0.41/ 0.27	0.46/ 0.29	ns, Min

Table 57: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{RCCK_WE}/T_{RCKC_WE}	Write Enable (WE) input (Block RAM only)	0.44/ 0.19	0.47/ 0.25	0.52/ 0.35	0.67/ 0.24	ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN FIFO inputs	0.47/ 0.26	0.50/ 0.27	0.55/ 0.30	0.68/ 0.31	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	RDEN FIFO inputs	0.46/ 0.26	0.50/ 0.27	0.55/ 0.30	0.67/ 0.31	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers(10)	0.90	0.98	1.10	1.23	ns, Max
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	FIFO reset timing(11)	0.22/ 0.23	0.24/ 0.24	0.28/ 0.26	0.31/ 0.27	ns, Min
Maximum Frequency						
F_{MAX}	Block RAM in TDP and SDP modes (Write First and No Change modes)	600	540	450	340	MHz
	Block RAM (Read First mode)	525	475	400	275	MHz
	Block RAM (SDP mode)(12)	525	475	400	275	MHz
$F_{MAX\_CASCADE}$	Block RAM Cascade (Write First and No Change modes)	550	490	400	300	MHz
	Block RAM Cascade (Read First mode)	475	425	350	235	MHz
F_{MAX_FIFO}	FIFO in all modes	600	540	450	340	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	450	400	325	250	MHz

Notes:

1. TRACE will report all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. The FIFO reset must be asserted for at least three positive clock edges.
12. When using ISE software v12.4 or later, if the RDADDR_COLLISION_HWCONFIG attribute is set to PERFORMANCE or the block RAM is in single-port operation, then the faster F_{MAX} for WRITE_FIRST/NO_CHANGE modes apply.

Table 59: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$	DI Setup/Hold	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$	DEN Setup/Hold time	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$	DWE Setup/Hold time	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{MMCMCKO\_DO}$	CLK to out of DO(3)	2.60	3.02	3.64	3.68	ns
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY	0.32	0.34	0.38	0.38	ns

Notes:

1. To support longer delays in configuration, use the design solutions described in UG360: *Virtex-6 FPGA Configuration User Guide*.
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
3. DO will hold until next DRP operation.

Clock Buffers and Networks

Table 60: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-2	-1	-1L	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins Setup/Hold	All	0.11/ 0.00	0.13/ 0.00	0.16/ 0.00	0.13/ 0.00	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins Setup/Hold	All	0.11/ 0.00	0.13/ 0.00	0.16/ 0.00	0.13/ 0.00	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	All	0.07	0.08	0.10	0.10	ns
Maximum Frequency							
F_{MAX}	Global clock tree (BUFG)	All except LX760	800	750	700	667	MHz
		LX760	N/A	700	700	667	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 61: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BIOCKO_O}	Clock to out delay from I to O	0.14	0.16	0.18	0.21	ns
Maximum Frequency						
F_{MAX}	I/O clock tree (BUFIO)	800	800	710	710	MHz

Table 62: **Regional Clock Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BRCKO_O}	Clock to out delay from I to O	0.56	0.62	0.73	0.82	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.28	0.31	0.36	0.41	ns

Table 64: **MMCM Specification *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$RST_{MINPULSE}$	Minimum Reset Pulse Width	1.5	1.5	1.5	1.5	ns
F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized(9)	550	500	450	450	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300	300	300	300	MHz
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	135	135	135	135	MHz
	Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	10	10	10	10	MHz
$T_{FBDELAY}$	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				
$T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$	Setup and Hold of Phase Shift Enable	1.04 0.00	1.04 0.00	1.04 0.00	1.04 0.00	ns
$T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$	Setup and Hold of Phase Shift Increment/Decrement	1.04 0.00	1.04 0.00	1.04 0.00	1.04 0.00	ns
$T_{MMCMCKO\_PSDONE}$	Phase Shift Clock-to-Out of PSDONE	0.32	0.34	0.38	0.38	ns

Notes:

1. When DIVCLK_DIVIDE = 3 or 4, F_{INMAX} is 315 MHz.
2. This duty cycle specification does not apply to the GTH_QUAD (GTH) to MMCM connection. The GTH transceivers drive the MMCMs at the following maximum frequencies: 323 MHz for -1 speed grade devices, 350 MHz for -2 speed grade devices, or 350 MHz for -3 speed grade devices.
3. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. The static offset is measured between any MMCM outputs with identical phase.
5. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
6. Includes global clock buffer.
7. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
8. When CASCADE4_OUT = TRUE, F_{OUTMIN} is 0.036 MHz.
9. In ISE software 12.3 (or earlier versions supporting the Virtex-6 family), the phase frequency detector Optimized bandwidth setting is equivalent to the High bandwidth setting. Starting with ISE software 12.4, the Optimized bandwidth setting is automatically adjusted to Low when the software can determine that the phase frequency detector input is less than 135 MHz.

Table 70: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard.(1)							
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No Delay Clock-capable Clock Input and IFF(2) with MMCM	XC6VLX75T	1.56/ –0.25	1.69/ –0.25	1.86/ –0.25	1.91/ –0.15	ns
		XC6VLX130T	1.64/ –0.25	1.78/ –0.25	1.95/ –0.25	2.00/ –0.14	ns
		XC6VLX195T	1.65/ –0.24	1.79/ –0.24	1.96/ –0.24	2.01/ –0.15	ns
		XC6VLX240T	1.65/ –0.24	1.79/ –0.24	1.96/ –0.24	2.01/ –0.15	ns
		XC6VLX365T	1.66/ –0.25	1.79/ –0.25	1.97/ –0.25	2.02/ –0.15	ns
		XC6VLX550T	N/A	1.97/ –0.24	2.16/ –0.24	2.19/ –0.14	ns
		XC6VLX760	N/A	2.39/ –0.20	2.63/ –0.20	2.21/ –0.10	ns
		XC6VSX315T	1.67/ –0.25	1.80/ –0.25	1.98/ –0.25	2.03/ –0.16	ns
		XC6VSX475T	N/A	1.98/ –0.29	2.17/ –0.29	2.21/ –0.20	ns
		XC6VHX250T	1.63/ –0.24	1.76/ –0.24	1.94/ –0.24	N/A	ns
		XC6VHX255T	1.63/ –0.19	1.76/ –0.19	1.99/ –0.19	N/A	ns
		XC6VHX380T	1.80/ –0.23	1.94/ –0.23	2.13/ –0.23	N/A	ns
		XC6VHX565T	N/A	1.94/ –0.08	2.13/ –0.08	N/A	ns
		XQ6VLX130T	N/A	1.78/ –0.25	1.95/ –0.25	2.00/ –0.14	ns
		XQ6VLX240T	N/A	1.79/ –0.24	1.96/ –0.24	2.01/ –0.15	ns
		XQ6VLX550T	N/A	N/A	2.16/ –0.24	2.19/ –0.14	ns
		XQ6VSX315T	N/A	1.80/ –0.25	1.98/ –0.25	2.03/ –0.16	ns
		XQ6VSX475T	N/A	N/A	2.17/ –0.29	2.21/ –0.20	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 73: **Sample Window**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{SAMP}	Sampling Error at Receiver Pins(1)	All	510	560	610	670	ps
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO(2)	All	300	350	400	440	ps

Notes:

1. This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 74: **Pin-to-Pin Setup/Hold and Clock-to-Out**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO						
T_{PSCS}/T_{PHCS}	Setup/Hold of I/O clock	–0.28/1.09	–0.28/1.16	–0.28/1.33	–0.18/1.79	ns
Pin-to-Pin Clock-to-Out Using BUFIO						
$T_{ICKOFCS}$	Clock-to-Out of I/O clock	4.22	4.59	5.22	5.63	ns

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
07/16/09	1.1	Revised the maximum V_{CCAUX} and V_{IN} numbers in Table 2, page 2. Removed empty column from Table 3, page 3. Revised specifications on Table 20, page 13. Updated Table 38, page 22 and added notes 1 and 2. Revised T_{DLYCCO_RDY}, $T_{IDELAYCTRL\_RPW}$, and $T_{IDELAYPAT\_JIT}$ in Table 53, page 41. Updated Table 58, page 46 to more closely match the DSP48E1 speed specifications. Updated T_{TAPTCK}/T_{TCKTAP} in Table 59, page 49. Updated XC6VLX130T parameters in Table 68 through Table 70, page 59.
08/19/09	1.2	Added values for -1L voltages and speed grade in all pertinent tables. Added V_{FS} and notes to Table 1 and Table 2. Removed DV_{PPIN} from the example in Figure 2. Added networking applications to Table 41, page 25. Changed and added to the block RAM F_{MAX} section in Table 57, page 44 including removing Note 12. Changed F_{PFDMAX} values and corrected units for $T_{STATPHAOFFSET}$ and $T_{OUTDUTY}$ in Table 64, page 52. Updated Table 71, page 60.
09/16/09	2.0	Added Virtex-6 HXT devices to entire document including GTH Transceiver Specifications. Updated speed specifications as described in Switching Characteristics, includes changes in Table 51, Table 57, Table 58, and Table 66 through Table 70. Comprehensive changes to Table 14, Table 15, and Table 16. Added conditions to D_{VPPOUT} and revised description of T_{OSKEW} in Table 17. Removed V_{ISE} specification and note from Table 18. Added note 3 to Table 23. Updated note 3 in Table 24. Updated LVCMOS25 delays in Table 44. Updated specification for T_{IOTPHZ} in Table 46. Removed $T_{BUFHSKEW}$ from Table 71, page 60 and added values for $T_{BUFIOSKEW}$. Added values in Table 74.