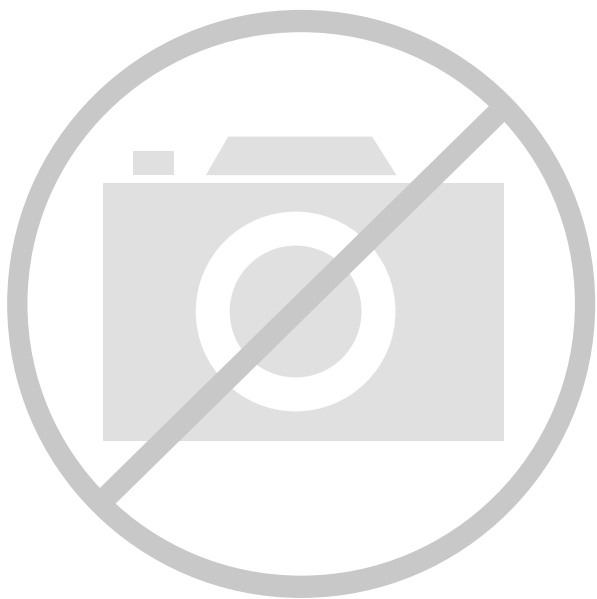




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	29880
Number of Logic Elements/Cells	382464
Total RAM Bits	28311552
Number of I/O	720
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1924-BBGA, FCBGA
Supplier Device Package	1924-FCBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vhx380t-2ff1923c

Table 4: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed and Temperature Grade						Units
			-3 (C)	-2 (C, E, & I)	-1 (C & I)	-1 (I & M) ⁽²⁾	-1L (C)	-1L (I) ⁽¹⁾	
I _{CCOQ}	Quiescent V _{CCO} supply current	XC6VLX75T	1	1	1	N/A	1	1	mA
		XC6VLX130T	1	1	1	N/A	1	1	mA
		XC6VLX195T	1	1	1	N/A	1	1	mA
		XC6VLX240T	2	2	2	N/A	2	2	mA
		XC6VLX365T	2	2	2	N/A	2	2	mA
		XC6VLX550T ⁽³⁾	N/A	3	3	N/A	3	3	mA
		XC6VLX760 ⁽³⁾	N/A	3	3	N/A	3	3	mA
		XC6VSX315T	2	2	2	N/A	2	2	mA
		XC6VSX475T ⁽³⁾	N/A	2	2	N/A	2	2	mA
		XC6VHX250T	1	1	1	N/A	N/A	N/A	mA
		XC6VHX255T	1	1	1	N/A	N/A	N/A	mA
		XC6VHX380T ⁽⁴⁾	2	2	2	N/A	N/A	N/A	mA
		XC6VHX565T ⁽⁵⁾	N/A	2	2	N/A	N/A	N/A	mA
		XQ6VLX130T	N/A	1	N/A	1	N/A	1	mA
		XQ6VLX240T	N/A	2	N/A	2	N/A	2	mA
		XQ6VLX550T ⁽⁷⁾	N/A	N/A	N/A	3	N/A	3	mA
		XQ6VSX315T	N/A	2	N/A	2	N/A	2	mA
		XQ6VSX475T ⁽⁷⁾	N/A	N/A	N/A	2	N/A	2	mA

HT DC Specifications (HT_25)

Table 8: HT DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage for XC devices	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	480	600	885	mV
	Differential Output Voltage for XQ devices		480	600	930	mV
ΔV_{OD}	Change in V_{OD} Magnitude		-15	—	15	mV
V_{OCM}	Output Common Mode Voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	440	600	760	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		-15	—	15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		-15	—	15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		-15	—	15	mV

LVDS DC Specifications (LVDS_25)

Table 9: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	—	—	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.825	—	—	V
V_{ODIFF}	Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage for XC devices	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
	Output Common-Mode Voltage for XQ devices		1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 10: Extended LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	—	—	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.715	—	—	V
V_{ODIFF}	Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High for XC devices	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	350	—	840	mV
	Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High for XQ devices		350	—	850	mV
V_{OCM}	Output Common-Mode Voltage for XC devices	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
	Output Common-Mode Voltage for XQ devices		1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	—	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ± 350 mV	0.3	1.2	2.2	V

GTH Transceiver DC Input and Output Levels

Table 30 summarizes the DC output specifications of the GTH transceivers in Virtex-6 FPGAs. Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further details.

Table 30: GTH Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
D_{VPPIN}	Differential peak-to-peak input voltage	External AC coupled	175	–	1200	mV
D_{VPPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	800	–	1200	mV
R_{IN}	Differential input resistance		80	100	120	Ω
R_{OUT}	Differential output resistance		80	100	120	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	–	ps
C_{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 31 summarizes the DC specifications of the clock input of the GTH transceiver. Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further details.

Table 31: GTH Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	≤ 600 MHz	500	–	1600	mV
		> 600 MHz	600	–	1600	mV
R_{IN}	Differential input resistance		80	100	120	Ω
C_{EXT}	Required external AC coupling capacitor		–	100	–	nF

GTH Transceiver Switching Characteristics

Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further information.

Table 32: GTH Transceiver Maximum Data Rate and PLL Frequency Range

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F_{GTHMAX}	Maximum GTH transceiver data rate	PLL Output Divider = 1	11.182	11.182	10.32	Gb/s
		PLL Output Divider = 4	2.795	2.795	2.58	Gb/s
F_{GTHMIN}	Minimum GTH transceiver data rate ⁽¹⁾	PLL Output Divider = 1	9.92	9.92	9.92	Gb/s
		PLL Output Divider = 4	2.48	2.48	2.48	Gb/s
$F_{GPLLMAX}$	Maximum GTH PLL frequency		5.591	5.591	5.16	GHz
$F_{GPLLMIN}$	Minimum GTH PLL frequency		4.96	4.96	4.96	GHz

Notes:

- Lower data rates can be achieved using FPGA logic based oversampling designs.

Table 33: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{GTHDRPCLK}$	GTHDRPCLK maximum frequency	70	70	60	MHz

Table 34: GTH Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range	-1 speed grade	150	—	645	MHz
		-2 and -3 speed grades	150	—	700	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	—	200	—	ps
T_{FCLK}	Reference clock fall time	80% – 20%	—	200	—	ps
T_{DCREF}	Reference clock duty cycle	CLK	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	—	—	2	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	—	—	20	μs

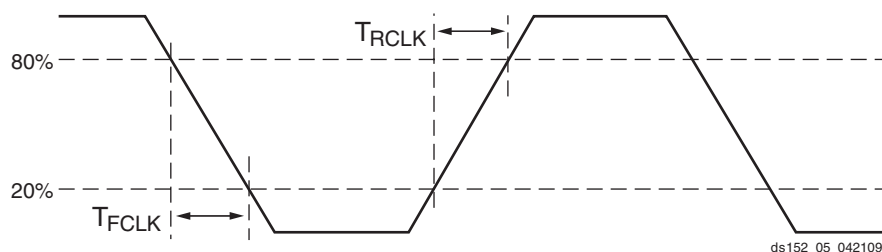


Figure 5: Reference Clock Timing Parameters

Table 35: GTH Transceiver User Clock Switching Characteristics ⁽¹⁾

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F _{TXOUT}	TXUSERCLKOUT maximum frequency		350	350	323	MHz
F _{RXOUT}	RXUSERCLKOUT maximum frequency		350	350	323	MHz
F _{TXIN}	TXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz
F _{RXIN}	RXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz

Notes:

1. Clocking must be implemented as described in [UG371](#): Virtex-6 FPGA GTH Transceivers User Guide.

Table 36: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
T _{RTX}	TX Rise time	20%–80%	–	50 ⁽³⁾	–	ps
T _{FTX}	TX Fall time	80%–20%	–	50 ⁽³⁾	–	ps
T _{LLSKEW}	TX lane-to-lane skew	within one GTH Quad	–	–	300	ps
Transmitter Output Jitter⁽¹⁾⁽²⁾						
TJ _{11.18}	Total Jitter	11.181 Gb/s	–	–	0.280	UI
DJ _{11.18}	Deterministic Jitter		–	–	0.170	UI
TJ _{10.3125}	Total Jitter	10.3125 Gb/s	–	–	0.280	UI
DJ _{10.3125}	Deterministic Jitter		–	–	0.170	UI
TJ _{9.953}	Total Jitter	9.953 Gb/s	–	–	0.280	UI
DJ _{9.953}	Deterministic Jitter		–	–	0.170	UI
TJ _{2.667}	Total Jitter	2.667 Gb/s	–	–	0.110	UI
DJ _{2.667}	Deterministic Jitter		–	–	0.060	UI
TJ _{2.488}	Total Jitter	2.488 Gb/s	–	–	0.110	UI
DJ _{2.488}	Deterministic Jitter		–	–	0.060	UI

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit-error ratio of 1e⁻¹².
3. Rise and fall times are specified at the transmitter package balls.

Table 37: GTH Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
R _{XRL}	Run length (CID)		8000	–	–	UI
R _{XPPMTOL}	Data/REFCLK PPM offset tolerance		–200	–	200	ppm
SJ Jitter Tolerance ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾						
JT_SJ _{11.18}	Sinusoidal Jitter	11.18 Gb/s	0.3	–	–	UI
JT_SJ _{10.32}	Sinusoidal Jitter	10.32 Gb/s	0.3	–	–	UI
JT_SJ _{9.95}	Sinusoidal Jitter	9.95 Gb/s	0.3	–	–	UI
JT_SJ _{2.667}	Sinusoidal Jitter	2.667 Gb/s	0.5	–	–	UI
JT_SJ _{2.48}	Sinusoidal Jitter	2.48 Gb/s	0.5	–	–	UI

Notes:

- These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit error ratio of 1e⁻¹².
- The frequency of the injected sinusoidal jitter is 80 MHz.
- High-frequency jitter tolerance including 6 db of channel loss at a high frequency of the data rate divided by two.

Ethernet MAC Switching Characteristics

Consult [UG368: Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide](#) for further information.

Table 38: Maximum Ethernet MAC Performance

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1	-1L	
F _{TEMACCLIENT}	Client interface maximum frequency	10 Mb/s – 8-bit width	2.5 ⁽¹⁾	2.5 ⁽¹⁾	2.5 ⁽¹⁾	2.5 ⁽¹⁾	MHz
		100 Mb/s – 8-bit width	25 ⁽²⁾	25 ⁽²⁾	25 ⁽²⁾	25 ⁽²⁾	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		1000 Mb/s – 16-bit width	62.5	62.5	62.5	62.5	MHz
		2000 Mb/s – 16-bit width	125	125	125	N/A	MHz
		2500 Mb/s – 16-bit width	156.25	156.25	156.25	N/A	MHz
F _{TEMACPHY}	Physical interface maximum frequency	10 Mb/s – 4-bit width	2.5	2.5	2.5	2.5	MHz
		100 Mb/s – 4-bit width	25	25	25	25	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		2000 Mb/s – 8-bit width	250	250	250	N/A	MHz
		2500 Mb/s – 8-bit width	312.5	312.5	312.5	N/A	MHz

Notes:

- When not using clock enable, the F_{MAX} is lowered to 1.25 MHz.
- When not using clock enable, the F_{MAX} is lowered to 12.5 MHz.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label ([Advance](#), [Preliminary](#), [Production](#)). Any labeling discrepancies are corrected in subsequent speed specification releases.

[Table 43](#) lists the production released Virtex-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE® software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 43: Virtex-6 Device Production Software and Speed Specification Release

Device	Speed Grade Designations			
	-3	-2	-1	-1L
XC6VLX75T	ISE 12.2 v1.08			ISE 12.3 v1.07 Patch
XC6VLX130T	ISE 12.1 v1.06	ISE 11.5 v1.05 ⁽²⁾	ISE 11.5 v1.05 ⁽²⁾	ISE 12.2 v1.05
XC6VLX195T	ISE 12.1 v1.06	ISE 12.1 v1.06	ISE 12.1 v1.06	ISE 12.2 v1.04
XC6VLX240T	ISE 12.1 v1.06	ISE 11.4.1 v1.04 ⁽²⁾	ISE 11.4.1 v1.04 ⁽²⁾	ISE 12.2 v1.04
XC6VLX365T	ISE 12.2 v1.08			ISE 12.2 v1.04
XC6VLX550T	N/A	ISE 12.2 v1.07		ISE 12.2 v1.04
XC6VLX760	N/A	ISE 12.2 v1.08		ISE 12.3 v1.07 Patch
XC6VSX315T	ISE 12.2 v1.08	ISE 12.1 v1.06		ISE 12.3 v1.07 Patch
XC6VSX475T	N/A	ISE 12.2 v1.08		ISE 12.3 v1.07 Patch
XC6VHX250T	ISE 12.4 v1.10			N/A
XC6VHX255T	ISE 13.1 v1.14 using the ISE 13.1 software update			N/A
XC6VHX380T	ISE 12.4 v1.10			N/A
XC6VHX565T	N/A	ISE 13.1 v1.14 using the ISE 13.1 software update		N/A
XQ6VLX130T	N/A	ISE 13.3 v1.17 Patch		ISE 13.3 v1.10
XQ6VLX240T	N/A	ISE 13.3 v1.17 Patch		ISE 13.3 v1.10
XQ6VLX550T	N/A	N/A	ISE 13.3 v1.17 Patch	ISE 13.3 v1.10
XQ6VSX315T	N/A	ISE 13.3 v1.17 Patch		ISE 13.3 v1.10
XQ6VSX475T	N/A	N/A	ISE 13.3 v1.17 Patch	ISE 13.3 v1.10

Notes:

- Blank entries indicate a device and/or speed grade in advance or preliminary status.
- Designs utilizing the GTX transceivers must use the software version ISE 12.1 v1.06 or later.

IOB Pad Input/Output/3-State Switching Characteristics

Table 44 (for commercial (XC) Virtex-6 devices) and **Table 45** (for the Defense-grade (XQ) Virtex-6 devices) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 46 summarizes the value of T_{IOTPHZ} . T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDS_25	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
LVDSEXT_25	0.85	0.94	1.09	1.08	1.53	1.65	1.84	1.73	1.53	1.65	1.84	1.73	ns
HT_25	0.85	0.94	1.09	1.08	1.51	1.62	1.78	1.69	1.51	1.62	1.78	1.69	ns
BLVDS_25	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.65	1.39	1.50	1.67	1.65	ns
RSDS_25 (point to point)	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
HSTL_I	0.81	0.91	1.06	1.06	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns
HSTL_II	0.81	0.91	1.06	1.06	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
HSTL_III	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
HSTL_I_18	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
HSTL_II_18	0.81	0.91	1.06	1.06	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
HSTL_III_18	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
SSTL2_I	0.81	0.91	1.06	1.06	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
SSTL2_II	0.81	0.91	1.06	1.06	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
LVC MOS25, Slow, 2 mA	0.51	0.57	0.66	0.70	5.09	5.46	6.01	5.63	5.09	5.46	6.01	5.63	ns
LVC MOS25, Slow, 4 mA	0.51	0.57	0.66	0.70	3.30	3.49	3.79	3.65	3.30	3.49	3.79	3.65	ns
LVC MOS25, Slow, 6 mA	0.51	0.57	0.66	0.70	2.62	2.81	3.08	2.95	2.62	2.81	3.08	2.95	ns
LVC MOS25, Slow, 8 mA	0.51	0.57	0.66	0.70	2.21	2.41	2.72	2.59	2.21	2.41	2.72	2.59	ns
LVC MOS25, Slow, 12 mA	0.51	0.57	0.66	0.70	1.80	1.95	2.17	2.10	1.80	1.95	2.17	2.10	ns
LVC MOS25, Slow, 16 mA	0.51	0.57	0.66	0.70	1.89	2.05	2.29	2.21	1.89	2.05	2.29	2.21	ns
LVC MOS25, Slow, 24 mA	0.51	0.57	0.66	0.70	1.68	1.82	2.02	1.98	1.68	1.82	2.02	1.98	ns
LVC MOS25, Fast, 2 mA	0.51	0.57	0.66	0.70	5.12	5.49	6.04	5.62	5.12	5.49	6.04	5.62	ns
LVC MOS25, Fast, 4 mA	0.51	0.57	0.66	0.70	3.28	3.50	3.82	3.65	3.28	3.50	3.82	3.65	ns
LVC MOS25, Fast, 6 mA	0.51	0.57	0.66	0.70	2.56	2.73	2.99	2.88	2.56	2.73	2.99	2.88	ns
LVC MOS25, Fast, 8 mA	0.51	0.57	0.66	0.70	2.11	2.33	2.65	2.53	2.11	2.33	2.65	2.53	ns
LVC MOS25, Fast, 12 mA	0.51	0.57	0.66	0.70	1.74	1.88	2.08	2.03	1.74	1.88	2.08	2.03	ns
LVC MOS25, Fast, 16 mA	0.51	0.57	0.66	0.70	1.77	1.92	2.13	2.08	1.77	1.92	2.13	2.08	ns

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDCI_DV2_25	0.51	0.57	0.66	0.70	1.71	1.83	2.01	2.00	1.71	1.83	2.01	2.00	ns
LVDCI_DV2_18	0.55	0.61	0.71	0.73	1.69	1.81	2.00	1.98	1.69	1.81	2.00	1.98	ns
LVDCI_DV2_15	0.64	0.73	0.85	0.85	1.68	1.77	1.91	1.98	1.68	1.77	1.91	1.98	ns
LVPECL_25	0.85	0.94	1.09	1.08	1.38	1.49	1.65	1.64	1.38	1.49	1.65	1.64	ns
HSTL_I_12	0.81	0.91	1.06	1.06	1.48	1.60	1.78	1.74	1.48	1.60	1.78	1.74	ns
HSTL_I_DCI	0.81	0.91	1.06	1.06	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
HSTL_II_DCI	0.81	0.91	1.06	1.06	1.37	1.49	1.68	1.66	1.37	1.49	1.68	1.66	ns
HSTL_II_T_DCI	0.81	0.91	1.06	1.06	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
HSTL_III_DCI	0.81	0.91	1.06	1.06	1.34	1.45	1.62	1.61	1.34	1.45	1.62	1.61	ns
HSTL_I_DCI_18	0.81	0.91	1.06	1.06	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
HSTL_II_DCI_18	0.81	0.91	1.06	1.06	1.36	1.46	1.62	1.59	1.36	1.46	1.62	1.59	ns
HSTL_II_T_DCI_18	0.81	0.91	1.06	1.06	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
HSTL_III_DCI_18	0.81	0.91	1.06	1.06	1.43	1.54	1.69	1.67	1.43	1.54	1.69	1.67	ns
DIFF_HSTL_I_18	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
DIFF_HSTL_I_DCI_18	0.85	0.94	1.09	1.08	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
DIFF_HSTL_I	0.85	0.94	1.09	1.08	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns
DIFF_HSTL_I_DCI	0.85	0.94	1.09	1.08	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
DIFF_HSTL_II_18	0.85	0.94	1.09	1.08	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
DIFF_HSTL_II_DCI_18	0.85	0.94	1.09	1.08	1.36	1.46	1.62	1.59	1.36	1.46	1.62	1.59	ns
DIFF_HSTL_II_T_DCI_18	0.85	0.94	1.09	1.08	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
DIFF_HSTL_II	0.85	0.94	1.09	1.08	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
DIFF_HSTL_II_DCI	0.85	0.94	1.09	1.08	1.37	1.49	1.68	1.66	1.37	1.49	1.68	1.66	ns
SSTL2_I_DCI	0.81	0.91	1.06	1.06	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
SSTL2_II_DCI	0.81	0.91	1.06	1.06	1.39	1.50	1.67	1.69	1.39	1.50	1.67	1.69	ns
SSTL2_II_T_DCI	0.81	0.91	1.06	1.06	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
SSTL18_I	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
SSTL18_II	0.81	0.91	1.06	1.06	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
SSTL18_I_DCI	0.81	0.91	1.06	1.06	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
SSTL18_II_DCI	0.81	0.91	1.06	1.06	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
SSTL18_II_T_DCI	0.81	0.91	1.06	1.06	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL2_I	0.85	0.94	1.09	1.08	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
DIFF_SSTL2_I_DCI	0.85	0.94	1.09	1.08	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
DIFF_SSTL2_II	0.85	0.94	1.09	1.08	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
DIFF_SSTL2_II_DCI	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.69	1.39	1.50	1.67	1.69	ns
DIFF_SSTL2_II_T_DCI	0.85	0.94	1.09	1.08	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
DIFF_SSTL18_I	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
DIFF_SSTL18_I_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL18_II	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
DIFF_SSTL18_II_DCI	0.85	0.94	1.09	1.08	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
DIFF_SSTL18_II_T_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
DIFF_SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVDS_25	0.94	1.09	1.08	1.54	2.16	1.62	1.54	2.16	1.62	ns
LVDSEXT_25	0.94	1.09	1.08	1.65	2.20	1.73	1.65	2.20	1.73	ns
HT_25	0.94	1.09	1.08	1.62	2.20	1.69	1.62	2.20	1.69	ns
BLVDS_25	0.94	1.09	1.08	1.50	3.18	1.65	1.50	3.18	1.65	ns
RSDS_25 (point to point)	0.94	1.09	1.08	1.54	2.22	1.62	1.54	2.22	1.62	ns
HSTL_I	0.91	1.06	1.06	1.56	2.44	1.71	1.56	2.44	1.71	ns
HSTL_II	0.91	1.06	1.06	1.56	2.21	1.72	1.56	2.21	1.72	ns
HSTL_III	0.91	1.06	1.06	1.54	2.50	1.69	1.54	2.50	1.69	ns
HSTL_I_18	0.91	1.06	1.06	1.58	2.43	1.72	1.58	2.43	1.72	ns
HSTL_II_18	0.91	1.06	1.06	1.62	2.30	1.78	1.62	2.30	1.78	ns
HSTL_III_18	0.91	1.06	1.06	1.54	2.49	1.69	1.54	2.49	1.69	ns
SSTL2_I	0.91	1.06	1.06	1.60	2.50	1.74	1.60	2.50	1.74	ns
SSTL2_II	0.91	1.06	1.06	1.54	2.49	1.71	1.54	2.49	1.71	ns
SSTL15	0.91	1.06	1.06	1.54	2.07	1.69	1.54	2.07	1.69	ns
LVC MOS25, Slow, 2 mA	0.57	0.66	0.70	5.46	6.01	5.63	5.46	6.01	5.63	ns
LVC MOS25, Slow, 4 mA	0.57	0.66	0.70	3.49	3.79	3.65	3.49	3.79	3.65	ns
LVC MOS25, Slow, 6 mA	0.57	0.66	0.70	2.81	3.08	2.95	2.81	3.08	2.95	ns
LVC MOS25, Slow, 8 mA	0.57	0.66	0.70	2.41	2.72	2.59	2.41	2.72	2.59	ns
LVC MOS25, Slow, 12 mA	0.57	0.66	0.70	1.95	2.23	2.10	1.95	2.23	2.10	ns
LVC MOS25, Slow, 16 mA	0.57	0.66	0.70	2.05	2.29	2.21	2.05	2.29	2.21	ns
LVC MOS25, Slow, 24 mA	0.57	0.66	0.70	1.82	2.24	1.98	1.82	2.24	1.98	ns
LVC MOS25, Fast, 2 mA	0.57	0.66	0.70	5.49	6.04	5.62	5.49	6.04	5.62	ns
LVC MOS25, Fast, 4 mA	0.57	0.66	0.70	3.50	3.82	3.65	3.50	3.82	3.65	ns
LVC MOS25, Fast, 6 mA	0.57	0.66	0.70	2.73	2.99	2.88	2.73	2.99	2.88	ns
LVC MOS25, Fast, 8 mA	0.57	0.66	0.70	2.33	2.65	2.53	2.33	2.65	2.53	ns
LVC MOS25, Fast, 12 mA	0.57	0.66	0.70	1.88	2.08	2.03	1.88	2.08	2.03	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
DIFF_SSTL18_II	0.94	1.09	1.08	1.50	2.27	1.66	1.50	2.27	1.66	ns
DIFF_SSTL18_II_DCI	0.94	1.09	1.08	1.47	2.20	1.62	1.47	2.20	1.62	ns
DIFF_SSTL18_II_T_DCI	0.94	1.09	1.08	1.51	2.30	1.65	1.51	2.30	1.65	ns
DIFF_SSTL15	0.91	1.06	1.06	1.54	2.25	1.69	1.54	2.25	1.69	ns
DIFF_SSTL15_DCI	0.91	1.06	1.06	1.52	2.25	1.66	1.52	2.25	1.66	ns
DIFF_SSTL15_T_DCI	0.91	1.06	1.06	1.52	2.25	1.66	1.52	2.25	1.66	ns

Table 46: IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{IOTPHZ}	T input to Pad high-impedance	0.86	0.92	0.99	0.99	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 47 shows the test setup parameters used for measuring input delay.

Table 47: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)(2)}$	$V_H^{(1)(2)}$	$V_{MEAS}^{(1)(4)(5)}$	$V_{REF}^{(1)(3)(5)}$
LVC MOS, 2.5V	LVC MOS25	0	2.5	1.25	—
LVC MOS, 1.8V	LVC MOS18	0	1.8	0.9	—
LVC MOS, 1.5V	LVC MOS15	0	1.5	0.75	—
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL, Class III	HSTL_III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	$V_{REF} - 1.00$	$V_{REF} + 1.00$	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	$1.2 - 0.125$	$1.2 + 0.125$	$0^{(6)}$	—
LVDS EXT (LVDS Extended Mode), 2.5V	LVDS EXT_25	$1.2 - 0.125$	$1.2 + 0.125$	$0^{(6)}$	—
HT (HyperTransport), 2.5V	LDT_25	$0.6 - 0.125$	$0.6 + 0.125$	$0^{(6)}$	—

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVC MOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H .
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 6.
6. The value given is the differential input voltage.

Table 48: Output Delay Measurement Methodology (Cont'd)

Description	I/O Standard Attribute	R _{REF} (Ω)	C _{REF} ⁽¹⁾ (pF)	V _{MEAS} (V)	V _{REF} (V)
HT (HyperTransport), 2.5V	LDT_25	100	0	0 ⁽²⁾	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	100	0	0 ⁽²⁾	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V _{REF}	0.75
HSTL, Class III, with DCI	HSTL_III_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V _{REF}	0.9
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termini.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V _{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V _{REF}	1.25

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 49: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Setup/Hold						
T _{ICE1CK} /T _{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.21/ 0.03	0.25/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T _{ISRCK} /T _{ICKSR}	SR pin Setup/Hold with respect to CLK	0.66/ −0.08	0.78/ −0.08	0.96/ −0.08	1.09/ −0.11	ns
T _{IDOCK} /T _{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.07/ 0.41	0.08/ 0.46	0.10/ 0.54	0.11/ 0.64	ns
T _{IDOCKD} /T _{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.10/ 0.32	0.12/ 0.36	0.14/ 0.42	0.16/ 0.50	ns
Combinatorial						
T _{IDI}	D pin to O pin propagation delay, no Delay	0.15	0.17	0.20	0.23	ns
T _{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.19	0.22	0.25	0.28	ns
Sequential Delays						
T _{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.48	0.54	0.64	0.73	ns
T _{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.52	0.58	0.68	0.78	ns
T _{ICKQ}	CLK to Q outputs	0.54	0.61	0.70	0.93	ns
T _{RQ_ILOGIC}	SR pin to OQ/TQ out	0.85	0.97	1.15	1.32	ns
T _{GSRQ_ILOGIC}	Global Set/Reset to Q outputs	7.60	7.60	10.51	10.51	ns
Set/Reset						
T _{RPW_ILOGIC}	Minimum Pulse Width, SR inputs	0.78	0.95	1.20	1.30	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 51: ISERDES Switching Characteristics

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup/Hold for Control Lines							
T _{ISCKK_BITSIP} / T _{ISCKC_BITSIP}	BITSLIP pin Setup/Hold with respect to CLKDIV	0.07/ 0.15	0.08/ 0.16	0.09/ 0.17	0.09/ 0.17	0.14/ 0.17	ns
T _{ISCKK_CE} / T _{ISCKC_CE} ⁽²⁾	CE pin Setup/Hold with respect to CLK (for CE1)	0.20/ 0.03	0.25/ 0.04	0.27/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T _{ISCKK_CE2} / T _{ISCKC_CE2} ⁽²⁾	CE pin Setup/Hold with respect to CLKDIV (for CE2)	0.01/ 0.27	0.01 0.29	0.01/ 0.31	0.01/ 0.31	−0.05/ 0.35	ns
Setup/Hold for Data Lines							
T _{ISDCK_D} / T _{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.07/ 0.08	0.08/ 0.09	0.09/ 0.11	0.09/ 0.11	0.11/ 0.19	ns
T _{ISDCK_DDLY} / T _{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY) ⁽¹⁾	0.10/ 0.05	0.12/ 0.06	0.14/ 0.07	0.14/ 0.07	0.16/ 0.15	ns
T _{ISDCK_D_DDR} / T _{ISCKD_D_DDR}	D pin Setup/Hold with respect to CLK at DDR mode	0.07/ 0.08	0.08/ 0.09	0.09/ 0.11	0.09/ 0.11	0.11/ 0.19	ns
T _{ISDCK_DDLY_DDR} / T _{ISCKD_DDLY_DDR}	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY) ⁽¹⁾	0.10/ 0.05	0.12/ 0.06	0.14/ 0.07	0.14/ 0.07	0.16/ 0.15	ns
Sequential Delays							
T _{ISCKO_Q}	CLKDIV to out at Q pin	0.57	0.66	0.75	0.80	0.88	ns
Propagation Delays							
T _{ISDO_DO}	D input to DO output pin	0.19	0.22	0.25	0.25	0.28	ns

Notes:

- Recorded at 0 tap value.
- T_{ISCK_CE2} and T_{ISCK_CE2} are reported as $T_{ISCK_CE} / T_{ISCK_CE}$ in TRACE report.

Input/Output Delay Switching Characteristics

Table 53: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
IDELAYCTRL						
T _{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3.00	3.00	3.00	3.25	μs
F _{IDELAYCTRL_REF}	REFCLK frequency = 200.0 ⁽¹⁾	200	200	200	200	MHz
	REFCLK frequency = 300.0 ⁽¹⁾	300	300	–	–	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
T _{IDELAYCTRL_RPW}	Minimum Reset pulse width	50.00	50.00	50.00	52.50	ns
IODELAY						
T _{IDELAYRESOLUTION}	IODELAY Chain Delay Resolution	1/(32 x 2 x F _{REF})				ps
T _{IDELAYPAT_JIT}	Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾	0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). ⁽³⁾	±5	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). ⁽⁴⁾	±9	±9	±9	±9	ps per tap
T _{IODELAY_CLK_MAX}	Maximum frequency of CLK input to IODELAY	500.00	420.00	300.00	300.00	MHz
T _{IODCCK_CE} / T _{IODCKC_CE}	CE pin Setup/Hold with respect to CK	0.45/ –0.09	0.53/ –0.09	0.65/ –0.09	0.84/ –0.14	ns
T _{IODCK_INC} / T _{IODCKC_INC}	INC pin Setup/Hold with respect to CK	0.23/ –0.02	0.27/ –0.01	0.31/ 0.00	0.27/ –0.04	ns
T _{IODCCK_RST} / T _{IODCKC_RST}	RST pin Setup/Hold with respect to CK	0.57/ –0.08	0.62/ –0.08	0.69/ –0.08	0.74/ –0.13	ns
T _{IODDO_T}	TSCONTROL delay to MUXE/MUXF switching and through IODELAY	Note 5	Note 5	Note 5	Note 5	ps
T _{IODDO_IDATAIN}	Propagation delay through IODELAY	Note 5	Note 5	Note 5	Note 5	ps
T _{IODDO_ODATAIN}	Propagation delay through IODELAY	Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See TRACE report for actual values.

CLB Switching Characteristics

Table 54: CLB Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Combinatorial Delays						
T _{ILO}	An – Dn LUT address to A	0.06	0.07	0.07	0.09	ns, Max
	An – Dn LUT address to AMUX/CMUX	0.18	0.20	0.22	0.25	ns, Max
	An – Dn LUT address to BMUX_A	0.28	0.31	0.36	0.40	ns, Max

DSP48E1 Switching Characteristics

Table 58: DSP48E1 Switching Characteristics

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock							
$T_{\text{DSPDCK}_{\{A, \text{ACIN}; B, \text{BCIN}\}}_{\{\text{AREG}; \text{BREG}\}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}; B, \text{BCIN}\}}_{\{\text{AREG}; \text{BREG}\}}}$	{A, ACIN, B, BCIN} input to {A, B} register CLK	0.25/ 0.27	0.29/ 0.30	0.35/ 0.34	0.36/ 0.34	0.46/ 0.39	ns
$T_{\text{DSPDCK}_{\text{C_CREG}}/T_{\text{DSPCKD}_{\text{C_CREG}}}}$	C input to C register CLK	0.16/ 0.20	0.19/ 0.22	0.22/ 0.24	0.25/ 0.24	0.33/ 0.30	ns
$T_{\text{DSPDCK}_{\text{D_DREG}}/T_{\text{DSPCKD}_{\text{D_DREG}}}}$	D input to D register CLK	0.07/ 0.31	0.10/ 0.34	0.15/ 0.39	0.16/ 0.39	0.24/ 0.45	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock							
$T_{\text{DSPDCK}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{MREG_MULT}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{MREG_MULT}}}$	{A, ACIN, B, BCIN} input to M register CLK	2.36/ 0.04	2.70/ 0.04	3.21/ 0.04	3.21/ 0.04	3.66/ 0.02	ns
$T_{\text{DSPDCK}_{\{A, D\}}_{\text{ADREG}}/T_{\text{DSPCKD}_{\{A, D\}}_{\text{ADREG}}}$	{A, D} input to AD register CLK	1.24/ 0.10	1.42/ 0.12	1.69/ 0.13	1.69/ 0.13	1.91/ 0.16	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock							
$T_{\text{DSPDCK}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG_MULT}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG_MULT}}}$	{A, ACIN, B, BCIN} input to P register CLK using multiplier	3.83/ −0.13	4.37/ −0.13	5.20/ −0.13	5.20/ −0.13	5.94/ −0.24	ns
$T_{\text{DSPDCK}_{\text{D_PREG_MULT}}/T_{\text{DSPCKD}_{\text{D_PREG_MULT}}}}$	D input to P register CLK	3.62/ −0.47	4.13/ −0.47	4.90/ −0.47	4.90/ −0.47	5.61/ −0.77	ns
$T_{\text{DSPDCK}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG}}}$	{A, ACIN, B, BCIN} input to P register CLK not using multiplier	1.59/ −0.13	1.81/ −0.13	2.15/ −0.13	2.15/ −0.13	2.44/ −0.24	ns
$T_{\text{DSPDCK}_{\text{C_PREG}}/T_{\text{DSPCKD}_{\text{C_PREG}}}}$	C input to P register CLK	1.42/ −0.10	1.61/ −0.10	1.91/ −0.10	1.91/ −0.10	2.16/ −0.19	ns
$T_{\text{DSPDCK}_{\{\text{PCIN}, \text{CARRYCASCIN}, \text{MULTSIGNIN}\}}_{\text{PREG}}/T_{\text{DSPCKD}_{\{\text{PCIN}, \text{CARRYCASCIN}, \text{MULTSIGNIN}\}}_{\text{PREG}}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK	1.23/ −0.02	1.41/ −0.02	1.67/ −0.02	1.67/ −0.02	1.91/ −0.07	ns
Setup and Hold Times of the CE Pins							
$T_{\text{DSPDCK}_{\{\text{CEA}; \text{CEB}\}}_{\{\text{AREG}; \text{BREG}\}}/T_{\text{DSPCKD}_{\{\text{CEA}; \text{CEB}\}}_{\{\text{AREG}; \text{BREG}\}}}$	{CEA; CEB} input to {A; B} register CLK	0.14/ 0.19	0.17/ 0.22	0.22/ 0.25	0.22/ 0.25	0.30/ 0.28	ns
$T_{\text{DSPDCK}_{\text{CEC_CREG}}/T_{\text{DSPCKD}_{\text{CEC_CREG}}}}$	CEC input to C register CLK	0.15/ 0.18	0.18/ 0.20	0.24/ 0.23	0.24/ 0.23	0.31/ 0.26	ns
$T_{\text{DSPDCK}_{\text{CED_DREG}}/T_{\text{DSPCKD}_{\text{CED_DREG}}}}$	CED input to D register CLK	0.20/ 0.12	0.24/ 0.13	0.31/ 0.14	0.31/ 0.14	0.43/ 0.16	ns
$T_{\text{DSPDCK}_{\text{CEM_MREG}}/T_{\text{DSPCKD}_{\text{CEM_MREG}}}}$	CEM input to M register CLK	0.16/ 0.19	0.20/ 0.21	0.26/ 0.25	0.26/ 0.25	0.32/ 0.28	ns
$T_{\text{DSPDCK}_{\text{CEP_PREG}}/T_{\text{DSPCKD}_{\text{CEP_PREG}}}}$	CEP input to P register CLK	0.32/ 0.02	0.38/ 0.02	0.46/ 0.03	0.46/ 0.03	0.54/ 0.04	ns
Setup and Hold Times of the RST Pins							
$T_{\text{DSPDCK}_{\{\text{RSTA}; \text{RSTB}\}}_{\{\text{AREG}; \text{BREG}\}}/T_{\text{DSPCKD}_{\{\text{RSTA}; \text{RSTB}\}}_{\{\text{AREG}; \text{BREG}\}}}$	{RSTA, RSTB} input to {A, B} register CLK	0.27/ 0.17	0.31/ 0.19	0.38/ 0.22	0.38/ 0.22	0.41/ 0.25	ns
$T_{\text{DSPDCK}_{\text{RSTC_CREG}}/T_{\text{DSPCKD}_{\text{RSTC_CREG}}}}$	RSTC input to C register CLK	0.18/ 0.08	0.20/ 0.08	0.23/ 0.09	0.23/ 0.09	0.27/ 0.11	ns
$T_{\text{DSPDCK}_{\text{RSTD_DREG}}/T_{\text{DSPCKD}_{\text{RSTD_DREG}}}}$	RSTD input to D register CLK	0.28/ 0.15	0.32/ 0.16	0.38/ 0.19	0.38/ 0.19	0.45/ 0.21	ns
$T_{\text{DSPDCK}_{\text{RSTM_MREG}}/T_{\text{DSPCKD}_{\text{RSTM_MREG}}}}$	RSTM input to M register CLK	0.20/ 0.24	0.23/ 0.26	0.26/ 0.30	0.26/ 0.30	0.29/ 0.34	ns

Table 62: Regional Clock Switching Characteristics (BUFR) (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T _{BRDO_O}	Propagation delay from CLR to O	0.69	0.74	0.80	1.12	ns
Maximum Frequency						
F _{MAX} ⁽¹⁾	Regional clock tree (BUFR)	500	420	300	300	MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

Table 63: Horizontal Clock Buffer Switching Characteristics (BUFH)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T _{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	0.15	ns
T _{BHCK_CE} /T _{BHCKC_CE}	CE pin Setup and Hold	0.04/ 0.04	0.04/ 0.04	0.05/ 0.05	0.04/ 0.04	ns
Maximum Frequency						
F _{MAX}	Horizontal clock buffer (BUFH)	800	750	700	667	MHz

MMCM Switching Characteristics

Table 64: MMCM Specification

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F _{INMAX}	Maximum Input Clock Frequency ⁽¹⁾	800	750	700	700	MHz
F _{INMIN}	Minimum Input Clock Frequency	10	10	10	10	MHz
F _{INJITTER}	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
F _{INDUTY} ⁽²⁾	Allowable Input Duty Cycle: 10—49 MHz	25/75				%
	Allowable Input Duty Cycle: 50—199 MHz	30/70				%
	Allowable Input Duty Cycle: 200—399 MHz	35/65				%
	Allowable Input Duty Cycle: 400—499 MHz	40/60				%
	Allowable Input Duty Cycle: >500 MHz	45/55				%
F _{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	0.01	0.01	MHz
F _{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	550	500	450	450	MHz
F _{VCOMIN}	Minimum MMCM VCO Frequency	600	600	600	600	MHz
F _{VCOMAX}	Maximum MMCM VCO Frequency	1600	1440	1200	1200	MHz
F _{BANDWIDTH}	Low MMCM Bandwidth at Typical ⁽³⁾	1.00	1.00	1.00	1.00	MHz
	High MMCM Bandwidth at Typical ⁽³⁾	4.00	4.00	4.00	4.00	MHz
T _{STATPHAOFFSET}	Static Phase Offset of the MMCM Outputs ⁽⁴⁾	0.12	0.12	0.12	0.12	ns
T _{OUTJITTER}	MMCM Output Jitter ⁽⁵⁾	Note 3				
T _{OUTDUTY}	MMCM Output Clock Duty Cycle Precision ⁽⁶⁾	0.15	0.20	0.20	0.20	ns
T _{LOCKMAX}	MMCM Maximum Lock Time	100	100	100	100	μs
F _{OUTMAX}	MMCM Maximum Output Frequency	800	750	700	700	MHz
F _{OUTMIN}	MMCM Minimum Output Frequency ⁽⁷⁾⁽⁸⁾	4.69	4.69	4.69	4.69	MHz
T _{EXTFDVAR}	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				

Table 69: Global Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T _{PSMMCMGC} / T _{PHMMCMGC}	No Delay Global Clock Input and IFF(2) with MMCM	XC6VLX75T	1.45/ −0.18	1.57/ −0.18	1.72/ −0.18	1.78/ −0.08	ns
		XC6VLX130T	1.53/ −0.18	1.65/ −0.18	1.81/ −0.18	1.87/ −0.07	ns
		XC6VLX195T	1.54/ −0.17	1.66/ −0.17	1.82/ −0.17	1.87/ −0.08	ns
		XC6VLX240T	1.54/ −0.17	1.66/ −0.17	1.82/ −0.17	1.87/ −0.08	ns
		XC6VLX365T	1.55/ −0.18	1.67/ −0.18	1.83/ −0.18	1.87/ −0.07	ns
		XC6VLX550T	N/A	1.84/ −0.17	2.02/ −0.17	2.06/ −0.06	ns
		XC6VLX760	N/A	2.26/ −0.13	2.49/ −0.13	2.06/ −0.03	ns
		XC6VSX315T	1.56/ −0.18	1.68/ −0.18	1.84/ −0.18	1.89/ −0.08	ns
		XC6VSX475T	N/A	1.85/ −0.23	2.03/ −0.23	2.07/ −0.13	ns
		XC6VHX250T	1.52/ −0.17	1.64/ −0.17	1.80/ −0.17	N/A	ns
		XC6VHX255T	1.52/ −0.12	1.64/ −0.12	1.85/ −0.12	N/A	ns
		XC6VHX380T	1.68/ −0.16	1.81/ −0.16	1.99/ −0.16	N/A	ns
		XC6VHX565T	N/A	1.81/ −0.01	1.99/ −0.01	N/A	ns
		XQ6VLX130T	N/A	1.65/ −0.18	1.81/ −0.18	1.87/ −0.07	ns
		XQ6VLX240T	N/A	1.66/ −0.17	1.82/ −0.17	1.87/ −0.08	ns
		XQ6VLX550T	N/A	N/A	2.02/ −0.17	2.06/ −0.06	ns
		XQ6VSX315T	N/A	1.68/ −0.18	1.84/ −0.18	1.89/ −0.08	ns
		XQ6VSX475T	N/A	N/A	2.03/ −0.23	2.07/ −0.13	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 FPGA clock transmitter and receiver data-valid windows.

Table 71: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion ⁽¹⁾	All	0.12	0.12	0.12	0.12	ns
T_{CKSKEW}	Global Clock Tree Skew ⁽²⁾	XC6VLX75T	0.15	0.16	0.18	0.17	ns
		XC6VLX130T	0.25	0.26	0.29	0.28	ns
		XC6VLX195T	0.26	0.27	0.31	0.30	ns
		XC6VLX240T	0.26	0.27	0.31	0.30	ns
		XC6VLX365T	0.28	0.29	0.31	0.31	ns
		XC6VLX550T	N/A	0.50	0.54	0.54	ns
		XC6VLX760	N/A	0.51	0.56	0.56	ns
		XC6VSX315T	0.27	0.28	0.32	0.30	ns
		XC6VSX475T	N/A	0.39	0.44	0.42	ns
		XC6VHX250T	0.25	0.26	0.29	N/A	ns
		XC6VHX255T	0.35	0.37	0.41	N/A	ns
		XC6VHX380T	0.45	0.47	0.52	N/A	ns
		XC6VHX565T	N/A	0.46	0.51	N/A	ns
		XQ6VLX130T	N/A	0.26	0.29	0.28	ns
		XQ6VLX240T	N/A	0.27	0.31	0.30	ns
		XQ6VLX550T	N/A	N/A	0.54	0.54	ns
		XQ6VSX315T	N/A	0.28	0.32	0.30	ns
		XQ6VSX475T	N/A	N/A	0.44	0.42	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.08	0.08	0.08	0.08	ns
T_{BUFIO_SKEW}	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	0.02	ns
T_{BUFIO_SKEW2}	I/O clock tree skew across three clock regions	All	0.10	0.12	0.23	0.12	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 73: Sample Window

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{SAMP}	Sampling Error at Receiver Pins ⁽¹⁾	All	510	560	610	670	ps
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO ⁽²⁾	All	300	350	400	440	ps

Notes:

1. This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 MMCM jitter
 - MMCM accuracy (phase offset)
 - MMCM phase shift resolution
These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 74: Pin-to-Pin Setup/Hold and Clock-to-Out

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO						
T _{PSCS} /T _{PHCS}	Setup/Hold of I/O clock	−0.28/1.09	−0.28/1.16	−0.28/1.33	−0.18/1.79	ns
Pin-to-Pin Clock-to-Out Using BUFIO						
T _{ICKOFC}	Clock-to-Out of I/O clock	4.22	4.59	5.22	5.63	ns

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
07/16/09	1.1	Revised the maximum V_{CCAUX} and V_{IN} numbers in Table 2, page 2 . Removed empty column from Table 3, page 3 . Revised specifications on Table 20, page 13 . Updated Table 38, page 22 and added notes 1 and 2. Revised T_{DLYCCO_RDY} , $T_{IDELAYCTRL_RPW}$, and $T_{IDELAYPAT_JIT}$ in Table 53, page 41 . Updated Table 58, page 46 to more closely match the DSP48E1 speed specifications. Updated T_{TAPTCK}/T_{TCKTAP} in Table 59, page 49 . Updated XC6VLX130T parameters in Table 68 through Table 70, page 59 .
08/19/09	1.2	Added values for -1L voltages and speed grade in all pertinent tables. Added V_{FS} and notes to Table 1 and Table 2 . Removed DV_{PPIN} from the example in Figure 2 . Added networking applications to Table 41, page 25 . Changed and added to the block RAM F_{MAX} section in Table 57, page 44 including removing Note 12. Changed F_{PFDMAX} values and corrected units for $T_{STATPHAOFFSET}$ and $T_{OUTDUTY}$ in Table 64, page 52 . Updated Table 71, page 60 .
09/16/09	2.0	Added Virtex-6 HXT devices to entire document including GTH Transceiver Specifications . Updated speed specifications as described in Switching Characteristics , includes changes in Table 51 , Table 57 , Table 58 , and Table 66 through Table 70 . Comprehensive changes to Table 14 , Table 15 , and Table 16 . Added conditions to DV_{PPOUT} and revised description of T_{OSKEW} in Table 17 . Removed V_{ISE} specification and note from Table 18 . Added note 3 to Table 23 . Updated note 3 in Table 24 . Updated LVCMOS25 delays in Table 44 . Updated specification for T_{IOTPHZ} in Table 46 . Removed $T_{BUFHSKEW}$ from Table 71, page 60 and added values for $T_{BUFIOSKEW}$. Added values in Table 74 .