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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	29880
Number of Logic Elements/Cells	382464
Total RAM Bits	28311552
Number of I/O	720
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1924-BBGA, FCBGA
Supplier Device Package	1924-FCBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vhx380t-2ff1923ces9945

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on sequence and ramp rate of the power supply.

The recommended power-on sequence for Virtex-6 devices is V_{CCINT} , V_{CCAUX} , and V_{CCO} to meet the power-up current requirements listed in Table 5. V_{CCINT} can be powered up or down at any time, but power up current specifications can vary from Table 5. The device will have no physical damage or reliability concerns if V_{CCINT} , V_{CCAUX} , and V_{CCO} sequence cannot be followed.

If the recommended power-up sequence cannot be followed and the I/Os must remain 3-stated throughout configuration, then V_{CCAUX} must be powered prior to V_{CCO} or V_{CCAUX} and V_{CCO} must be powered by the same supply. Similarly, for power-down, the reverse V_{CCAUX} and V_{CCO} sequence is recommended if the I/Os are to remain 3-stated.

The GTH transceiver supplies must be powered using a MGTHAVCC, MGTHAVCCR_X, MGTHAVCCPLL, and MGTHAVTT sequence. There are no sequencing requirement for these supplies with respect to the other FPGA supply voltages. For more detail see Table 27: *GTH Transceiver Power Supply Sequencing*. There are no sequencing requirements for the GTX transceivers power supplies.

Table 5 shows the minimum current, in addition to I_{CCQ} , that are required by Virtex-6 devices for proper power-on and configuration. If the current minimums shown in Table 4 and Table 5 are met, the device powers on after all three supplies have passed through their power-on reset threshold voltages. The FPGA must be configured after applying V_{CCINT} , V_{CCAUX} , and V_{CCO} for the appropriate configuration banks. Once initialized and configured, use the XPE tools to estimate current drain on these supplies.

Table 5: Power-On Current for Virtex-6 Devices

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	Units
	Typ ⁽¹⁾	Typ ⁽¹⁾	Typ ⁽¹⁾	
XC6VLX75T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 10$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VLX130T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 10$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VLX195T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VLX240T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VLX365T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VLX550T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VLX760	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VSX315T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VSX475T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 50$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VHX250T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VHX255T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VHX380T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VHX565T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XQ6VLX130T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 100$	$I_{CCOQ} + 30$ mA per bank	mA
XQ6VLX240T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 100$	$I_{CCOQ} + 30$ mA per bank	mA
XQ6VLX550T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 100$	$I_{CCOQ} + 30$ mA per bank	mA
XQ6VSX315T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 100$	$I_{CCOQ} + 40$ mA per bank	mA
XQ6VSX475T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 100$	$I_{CCOQ} + 40$ mA per bank	mA

Notes:

- Typical values are specified at nominal voltage, 25°C.
- Use the XPower Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate maximum power-on currents.

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 13: Absolute Maximum Ratings for GTX Transceivers⁽¹⁾

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	−0.5	1.1	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	−0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	−0.5	1.32	V
V _{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	−0.5	1.32	V
V _{MGTREFCLK}	Reference clock absolute input voltage	−0.5	1.32	V

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 14: Recommended Operating Conditions for GTX Transceivers⁽¹⁾⁽²⁾

Symbol	Description	Speed Grade	PLL Frequency	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	-3, -2 ⁽³⁾	> 2.7 GHz	1.0	1.03	1.06	V
		-3, -2 ⁽³⁾	≤ 2.7 GHz	0.95	1.0	1.06	V
		-1	≤ 2.7 GHz	0.95	1.0	1.06	V
		-1L	≤ 2.7 GHz	0.95	1.0	1.05	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	All	—	1.14	1.2	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	All	—	1.14	1.2	1.26	V

Notes:

- Each voltage listed requires the filter circuit described in [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#).
- Voltages are specified for the temperature range of T_j = −40°C to +100°C for all XC devices and T_j = −55°C to +125°C for the XQ devices.
- If a GTX Quad contains transceivers operating with a mixture of PLL frequencies above and below 2.7 GHz, the MGTAVCC voltage supply must be in the range of 1.0V to 1.06V.

Table 15: GTX Transceiver Supply Current (per Lane) ⁽¹⁾⁽²⁾

Symbol	Description	Typ	Max	Units
I _{MGTAVTT}	MGTAVTT supply current for one GTX transceiver	55.9	Note 2	mA
I _{MGTAVCC}	MGTAVCC supply current for one GTX transceiver	56.1		mA
MGTR _{REF}	Precision reference resistor for internal calibration termination	100.0 ± 1% tolerance		Ω

Notes:

- Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
- Values for currents of other transceiver configurations and conditions can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

Table 21: GTX Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		62.5	–	650	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	200	μ s

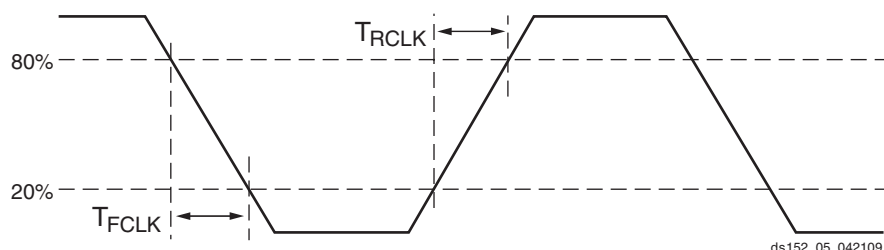


Figure 3: Reference Clock Timing Parameters

Table 22: GTX Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1	-1L	
F_{TXOUT}	TXOUTCLK maximum frequency	Internal 20-bit data path	330	330	250	250	MHz
		Internal 16-bit data path	412.5	412.5	312.5	250	MHz
F_{RXREC}	RXRECCLK maximum frequency	Internal 20-bit data path	330	330	250	250	MHz
		Internal 16-bit data path	412.5	412.5	312.5	250	MHz
T_{RX}	RXUSRCLK maximum frequency		412.5 ⁽²⁾	412.5 ⁽²⁾	312.5	250	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	376	376	312.5	250	MHz
		2 byte interface	406.25	406.25	312.5	250	MHz
		4 byte interface	206.25	206.25	156.25	125	MHz
T_{TX}	TXUSRCLK maximum frequency		412.5 ⁽³⁾	412.5 ⁽³⁾	312.5	250	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	376	376	312.5	250	MHz
		2 byte interface	406.25	406.25	312.5	250	MHz
		4 byte interface	206.25	206.25	156.25	125	MHz

Notes:

1. Clocking must be implemented as described in [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#).
2. 406.25 MHz when the RX elastic buffer is bypassed.
3. 406.25 MHz when the TX buffer is bypassed.

Table 23: GTX Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTXTX}	Serial data rate range		0.480	–	F _{GTXMAX}	Gb/s
T _{RTX}	TX Rise time	20%–80%	–	120	–	ps
T _{FTX}	TX Fall time	80%–20%	–	120	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	350	ps
V _{TXOOBVDPP}	Electrical idle amplitude		–	–	15	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		–	–	75	ns
TJ _{6.5}	Total Jitter ⁽²⁾⁽³⁾	6.5 Gb/s	–	–	0.33	UI
DJ _{6.5}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.17	UI
TJ _{5.0}	Total Jitter ⁽²⁾⁽³⁾	5.0 Gb/s	–	–	0.33	UI
DJ _{5.0}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.15	UI
TJ _{4.25}	Total Jitter ⁽²⁾⁽³⁾	4.25 Gb/s	–	–	0.33	UI
DJ _{4.25}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.14	UI
TJ _{3.75}	Total Jitter ⁽²⁾⁽³⁾	3.75 Gb/s	–	–	0.34	UI
DJ _{3.75}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.16	UI
TJ _{3.125}	Total Jitter ⁽²⁾⁽³⁾	3.125 Gb/s	–	–	0.2	UI
DJ _{3.125}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.1	UI
TJ _{3.125L}	Total Jitter ⁽²⁾⁽³⁾	3.125 Gb/s ⁽⁴⁾	–	–	0.35	UI
DJ _{3.125L}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.16	UI
TJ _{2.5}	Total Jitter ⁽²⁾⁽³⁾	2.5 Gb/s ⁽⁵⁾	–	–	0.20	UI
DJ _{2.5}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.08	UI
TJ _{1.25}	Total Jitter ⁽²⁾⁽³⁾	1.25 Gb/s ⁽⁶⁾	–	–	0.15	UI
DJ _{1.25}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.06	UI
TJ ₆₀₀	Total Jitter ⁽²⁾⁽³⁾	600 Mb/s	–	–	0.1	UI
DJ ₆₀₀	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.03	UI
TJ ₄₈₀	Total Jitter ⁽²⁾⁽³⁾	480 Mb/s	–	–	0.1	UI
DJ ₄₈₀	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
- Using PLL_DIVSEL_FB = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 1e⁻¹².
- PLL frequency at 1.5625 GHz and OUTDIV = 1.
- PLL frequency at 2.5 GHz and OUTDIV = 2.
- PLL frequency at 2.5 GHz and OUTDIV = 4.

GTH Transceiver Specifications

GTH Transceiver DC Characteristics

Table 25: Absolute Maximum Ratings for GTH Transceivers⁽¹⁾

Symbol	Description	Min	Max	Units
MGTHAVCC	Analog supply voltage for the GTH transmitter, receiver, and common analog circuits	−0.5	1.125	V
MGTHAVCCR _X	Analog supply voltage for the GTH receiver circuits and common analog circuits	−0.5	1.125	V
MGTHAVTT	Analog supply voltage for the GTH transmitter termination circuits	−0.5	1.32	V
MGTHAVCCPLL	Analog supply voltage for the GTH receiver and PLL circuits	−0.5	1.935	V
V _{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	−0.5	1.125	V
V _{MGTREFCLK}	Reference clock absolute input voltage	−0.5	1.935	V

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 26: Recommended Operating Conditions for GTH Transceivers ⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
MGTHAVCC	Analog supply voltage for the GTH transmitter, receiver, and common analog circuits	1.075	1.1	1.125	V
MGTHAVCCR _X	Analog supply voltage for the GTH receiver circuits and common analog circuits	1.075	1.1	1.125	V
MGTHAVTT	Analog supply voltage for the GTH transmitter termination circuits	1.140	1.2	1.26	V
MGTHAVCCPLL	Analog supply voltage for the GTH receiver and PLL circuit	1.710	1.8	1.89	V

Notes:

- Each voltage listed requires the filter circuit described in [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#).
- Voltages are specified for the temperature range of T_j = −40°C to +100°C.

Table 27: GTH Transceiver Power Supply Sequencing ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Description	Min	Max	Units
T _{HAVCC2HAVCCR_X}	Maximum time between powering MGTHAVCC to when MGTHAVCCR _X must be powered.	0	5	ms
T _{HAVCCR_X2HAVCCPLL}	Minimum time between powering MGTHAVCCR _X to when MGTHAVCCPLL can be powered.	10	—	μs
T _{HAVCCR_X2HAVTT}	Minimum time between powering MGTHAVCCR _X to when MGTHAVTT can be powered.	10	—	μs

Notes:

- MGTHAVCCR_X must be powered simultaneously or within T_{HAVCC2HAVCCR_X} of MGTHAVCC, but it must not precede MGTHAVCC.
- MGTHAVCC and MGTHAVCCR_X must be powered before MGTHAVCCPLL and MGTHAVTT. This minimum time is defined by T_{HAVCCR_X2HAVCCPLL} and T_{HAVCCR_X2HAVTT}.
- At any time, the condition of MGTHAVCC being present and MGTHAVCCR_X not being present should not occur for more than the maximum T_{HAVCC2HAVCCR_X}.

Figure 4 shows the timing parameters in Table 27.

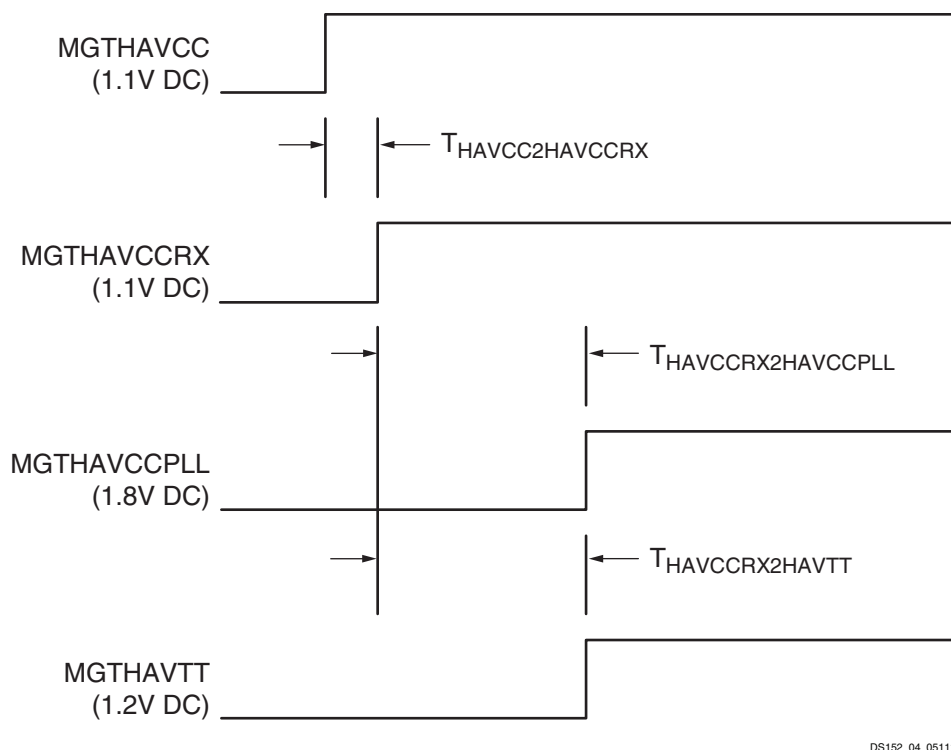


Figure 4: GTH Transceiver Power Supply Power-On Sequencing

Table 28: GTH Transceiver Supply Current

Symbol	Description	Typ ⁽¹⁾	Max	Units
$I_{MGTHAVCC}$	MGTHAVCC supply current for one GTH Quad (4 lanes)	571	Note 2	mA
$I_{MGTHAVCCR}$	MGTHAVCCR supply current for a GTH Quad (4 lanes)	254	Note 2	mA
$I_{MGTHAVTT}$	MGTHAVTT supply current for one GTH Quad (4 lanes)	93	Note 2	mA
$I_{MGTHAVCCPLL}$	MGTHAVCCPLL supply current for one GTH Quad (4 lanes)	219	Note 2	mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	1000.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 10.3125 Gb/s line rate.
2. Values for currents other than the values specified in this table can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

Table 29: GTH Transceiver Quiescent Supply Current⁽¹⁾⁽²⁾

Symbol	Description	Typ ⁽³⁾	Max	Units
$I_{MGTHAVCCQ}$	Quiescent MGTHAVCC Supply Current for one GTH Quad (4 lanes)	65	Note 4	mA
$I_{MGTHAVCCRQ}$	Quiescent MGTHAVCCR Supply Current for one GTH Quad (4 lanes)	17	Note 4	mA
$I_{MGTHAVTTQ}$	Quiescent MGTHAVTT Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA
$I_{MGTHAVCCPLLQ}$	Quiescent MGTHAVCCPLL Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA

Notes:

1. Device powered and unconfigured.
2. GTH transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTH transceivers.
3. Typical values are specified at nominal voltage, 25°C.
4. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.

GTH Transceiver Switching Characteristics

Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further information.

Table 32: GTH Transceiver Maximum Data Rate and PLL Frequency Range

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F_{GTHMAX}	Maximum GTH transceiver data rate	PLL Output Divider = 1	11.182	11.182	10.32	Gb/s
		PLL Output Divider = 4	2.795	2.795	2.58	Gb/s
F_{GTHMIN}	Minimum GTH transceiver data rate ⁽¹⁾	PLL Output Divider = 1	9.92	9.92	9.92	Gb/s
		PLL Output Divider = 4	2.48	2.48	2.48	Gb/s
$F_{GPLLMAX}$	Maximum GTH PLL frequency		5.591	5.591	5.16	GHz
$F_{GPLLMIN}$	Minimum GTH PLL frequency		4.96	4.96	4.96	GHz

Notes:

- Lower data rates can be achieved using FPGA logic based oversampling designs.

Table 33: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{GTHDRPCLK}$	GTHDRPCLK maximum frequency	70	70	60	MHz

Table 34: GTH Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range	-1 speed grade	150	—	645	MHz
		-2 and -3 speed grades	150	—	700	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	—	200	—	ps
T_{FCLK}	Reference clock fall time	80% – 20%	—	200	—	ps
T_{DCREF}	Reference clock duty cycle	CLK	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	—	—	2	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	—	—	20	μs

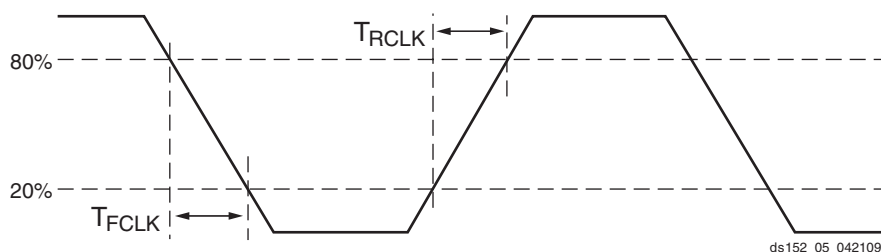


Figure 5: Reference Clock Timing Parameters

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 39: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F _{PIPECLK}	Pipe clock maximum frequency	250	250	250	250	MHz
F _{USERCLK}	User clock maximum frequency	500	500	250	250	MHz
F _{DRPCLK}	DRP clock maximum frequency	250	250	250	250	MHz

System Monitor Analog-to-Digital Converter Specification

Table 40: Analog-to-Digital Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
AV _{DD} = 2.5V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 5.2 MHz, T _j = -55°C to 125°C M-Grade, Typical values at T _j = +35°C						
DC Accuracy: All external input channels. Both unipolar and bipolar modes.						
Resolution			10	—	—	Bits
Integral Nonlinearity	INL		—	—	±1	LSBs
Differential Nonlinearity	DNL	No missing codes (T _{MIN} to T _{MAX}) Guaranteed Monotonic	—	—	±0.9	LSBs
Unipolar Offset Error ⁽¹⁾		Uncalibrated	—	±2	±30	LSBs
Bipolar Offset Error ⁽¹⁾		Uncalibrated measured in bipolar mode	—	±2	±30	LSBs
Gain Error		Uncalibrated - External Reference	—	±0.2	±2	%
		Uncalibrated - Internal Reference	—	±2	—	%
Bipolar Gain Error ⁽¹⁾		Uncalibrated - External Reference	—	±0.2	±2	%
		Uncalibrated - Internal Reference	—	±2	—	%
Total Unadjusted Error (Uncalibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	—	±10	—	LSBs
		Deviation from ideal transfer function. Internal reference	—	±20	—	LSBs
Total Unadjusted Error (Calibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	—	±1	±2	LSBs
Calibrated Gain Temperature Coefficient		Variation of FS code with temperature	—	±0.01	—	LSB/°C
DC Common-Mode Reject	CMRR _{DC}	V _N = V _{CM} = 0.5V ± 0.5V, V _P - V _N = 100mV	—	70	—	dB
Conversion Rate ⁽²⁾						
Conversion Time - Continuous	t _{CONV}	Number of CLK cycles	26	—	32	
Conversion Time - Event	t _{CONV}	Number of CLK cycles	—	—	21	
T/H Acquisition Time	t _{ACQ}	Number of CLK cycles	4	—	—	
DRP Clock Frequency	DCLK	DRP clock frequency	8	—	80	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	—	5.2	MHz
CLK Duty cycle			40	—	60	%

Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.17 for -3, -2, and -1; and v1.10 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 42 correlates the current status of each Virtex-6 device on a per speed grade basis.

Table 42: Virtex-6 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6VLX75T			-3, -2, -1, -1L
XC6VLX130T			-3, -2, -1, -1L
XC6VLX195T			-3, -2, -1, -1L
XC6VLX240T			-3, -2, -1, -1L
XC6VLX365T			-3, -2, -1, -1L
XC6VLX550T			-2, -1, -1L
XC6VLX760			-2, -1, -1L
XC6VSX315T			-3, -2, -1, -1L
XC6VSX475T			-2, -1, -1L
XC6VHX250T			-3, -2, -1
XC6VHX255T			-3, -2, -1
XC6VHX380T			-3, -2, -1
XC6VHX565T			-2, -1
XQ6VLX130T			-2, -1, -1L
XQ6VLX240T			-2, -1, -1L
XQ6VLX550T			-1, -1L
XQ6VSX315T			-2, -1, -1L
XQ6VSX475T			-1, -1L

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 devices.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label ([Advance](#), [Preliminary](#), [Production](#)). Any labeling discrepancies are corrected in subsequent speed specification releases.

[Table 43](#) lists the production released Virtex-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE® software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 43: Virtex-6 Device Production Software and Speed Specification Release

Device	Speed Grade Designations			
	-3	-2	-1	-1L
XC6VLX75T	ISE 12.2 v1.08			ISE 12.3 v1.07 Patch
XC6VLX130T	ISE 12.1 v1.06	ISE 11.5 v1.05 ⁽²⁾	ISE 11.5 v1.05 ⁽²⁾	ISE 12.2 v1.05
XC6VLX195T	ISE 12.1 v1.06	ISE 12.1 v1.06	ISE 12.1 v1.06	ISE 12.2 v1.04
XC6VLX240T	ISE 12.1 v1.06	ISE 11.4.1 v1.04 ⁽²⁾	ISE 11.4.1 v1.04 ⁽²⁾	ISE 12.2 v1.04
XC6VLX365T	ISE 12.2 v1.08			ISE 12.2 v1.04
XC6VLX550T	N/A	ISE 12.2 v1.07		ISE 12.2 v1.04
XC6VLX760	N/A	ISE 12.2 v1.08		ISE 12.3 v1.07 Patch
XC6VSX315T	ISE 12.2 v1.08	ISE 12.1 v1.06		ISE 12.3 v1.07 Patch
XC6VSX475T	N/A	ISE 12.2 v1.08		ISE 12.3 v1.07 Patch
XC6VHX250T	ISE 12.4 v1.10			N/A
XC6VHX255T	ISE 13.1 v1.14 using the ISE 13.1 software update			N/A
XC6VHX380T	ISE 12.4 v1.10			N/A
XC6VHX565T	N/A	ISE 13.1 v1.14 using the ISE 13.1 software update		N/A
XQ6VLX130T	N/A	ISE 13.3 v1.17 Patch		ISE 13.3 v1.10
XQ6VLX240T	N/A	ISE 13.3 v1.17 Patch		ISE 13.3 v1.10
XQ6VLX550T	N/A	N/A	ISE 13.3 v1.17 Patch	ISE 13.3 v1.10
XQ6VSX315T	N/A	ISE 13.3 v1.17 Patch		ISE 13.3 v1.10
XQ6VSX475T	N/A	N/A	ISE 13.3 v1.17 Patch	ISE 13.3 v1.10

Notes:

- Blank entries indicate a device and/or speed grade in advance or preliminary status.
- Designs utilizing the GTX transceivers must use the software version ISE 12.1 v1.06 or later.

IOB Pad Input/Output/3-State Switching Characteristics

Table 44 (for commercial (XC) Virtex-6 devices) and **Table 45** (for the Defense-grade (XQ) Virtex-6 devices) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 46 summarizes the value of T_{IOTPHZ} . T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDS_25	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
LVDSEXT_25	0.85	0.94	1.09	1.08	1.53	1.65	1.84	1.73	1.53	1.65	1.84	1.73	ns
HT_25	0.85	0.94	1.09	1.08	1.51	1.62	1.78	1.69	1.51	1.62	1.78	1.69	ns
BLVDS_25	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.65	1.39	1.50	1.67	1.65	ns
RSDS_25 (point to point)	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
HSTL_I	0.81	0.91	1.06	1.06	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns
HSTL_II	0.81	0.91	1.06	1.06	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
HSTL_III	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
HSTL_I_18	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
HSTL_II_18	0.81	0.91	1.06	1.06	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
HSTL_III_18	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
SSTL2_I	0.81	0.91	1.06	1.06	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
SSTL2_II	0.81	0.91	1.06	1.06	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
LVC MOS25, Slow, 2 mA	0.51	0.57	0.66	0.70	5.09	5.46	6.01	5.63	5.09	5.46	6.01	5.63	ns
LVC MOS25, Slow, 4 mA	0.51	0.57	0.66	0.70	3.30	3.49	3.79	3.65	3.30	3.49	3.79	3.65	ns
LVC MOS25, Slow, 6 mA	0.51	0.57	0.66	0.70	2.62	2.81	3.08	2.95	2.62	2.81	3.08	2.95	ns
LVC MOS25, Slow, 8 mA	0.51	0.57	0.66	0.70	2.21	2.41	2.72	2.59	2.21	2.41	2.72	2.59	ns
LVC MOS25, Slow, 12 mA	0.51	0.57	0.66	0.70	1.80	1.95	2.17	2.10	1.80	1.95	2.17	2.10	ns
LVC MOS25, Slow, 16 mA	0.51	0.57	0.66	0.70	1.89	2.05	2.29	2.21	1.89	2.05	2.29	2.21	ns
LVC MOS25, Slow, 24 mA	0.51	0.57	0.66	0.70	1.68	1.82	2.02	1.98	1.68	1.82	2.02	1.98	ns
LVC MOS25, Fast, 2 mA	0.51	0.57	0.66	0.70	5.12	5.49	6.04	5.62	5.12	5.49	6.04	5.62	ns
LVC MOS25, Fast, 4 mA	0.51	0.57	0.66	0.70	3.28	3.50	3.82	3.65	3.28	3.50	3.82	3.65	ns
LVC MOS25, Fast, 6 mA	0.51	0.57	0.66	0.70	2.56	2.73	2.99	2.88	2.56	2.73	2.99	2.88	ns
LVC MOS25, Fast, 8 mA	0.51	0.57	0.66	0.70	2.11	2.33	2.65	2.53	2.11	2.33	2.65	2.53	ns
LVC MOS25, Fast, 12 mA	0.51	0.57	0.66	0.70	1.74	1.88	2.08	2.03	1.74	1.88	2.08	2.03	ns
LVC MOS25, Fast, 16 mA	0.51	0.57	0.66	0.70	1.77	1.92	2.13	2.08	1.77	1.92	2.13	2.08	ns

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
DIFF_SSTL18_I	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
DIFF_SSTL18_I_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL18_II	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
DIFF_SSTL18_II_DCI	0.85	0.94	1.09	1.08	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
DIFF_SSTL18_II_T_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
DIFF_SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVDS_25	0.94	1.09	1.08	1.54	2.16	1.62	1.54	2.16	1.62	ns
LVDSEXT_25	0.94	1.09	1.08	1.65	2.20	1.73	1.65	2.20	1.73	ns
HT_25	0.94	1.09	1.08	1.62	2.20	1.69	1.62	2.20	1.69	ns
BLVDS_25	0.94	1.09	1.08	1.50	3.18	1.65	1.50	3.18	1.65	ns
RSDS_25 (point to point)	0.94	1.09	1.08	1.54	2.22	1.62	1.54	2.22	1.62	ns
HSTL_I	0.91	1.06	1.06	1.56	2.44	1.71	1.56	2.44	1.71	ns
HSTL_II	0.91	1.06	1.06	1.56	2.21	1.72	1.56	2.21	1.72	ns
HSTL_III	0.91	1.06	1.06	1.54	2.50	1.69	1.54	2.50	1.69	ns
HSTL_I_18	0.91	1.06	1.06	1.58	2.43	1.72	1.58	2.43	1.72	ns
HSTL_II_18	0.91	1.06	1.06	1.62	2.30	1.78	1.62	2.30	1.78	ns
HSTL_III_18	0.91	1.06	1.06	1.54	2.49	1.69	1.54	2.49	1.69	ns
SSTL2_I	0.91	1.06	1.06	1.60	2.50	1.74	1.60	2.50	1.74	ns
SSTL2_II	0.91	1.06	1.06	1.54	2.49	1.71	1.54	2.49	1.71	ns
SSTL15	0.91	1.06	1.06	1.54	2.07	1.69	1.54	2.07	1.69	ns
LVC MOS25, Slow, 2 mA	0.57	0.66	0.70	5.46	6.01	5.63	5.46	6.01	5.63	ns
LVC MOS25, Slow, 4 mA	0.57	0.66	0.70	3.49	3.79	3.65	3.49	3.79	3.65	ns
LVC MOS25, Slow, 6 mA	0.57	0.66	0.70	2.81	3.08	2.95	2.81	3.08	2.95	ns
LVC MOS25, Slow, 8 mA	0.57	0.66	0.70	2.41	2.72	2.59	2.41	2.72	2.59	ns
LVC MOS25, Slow, 12 mA	0.57	0.66	0.70	1.95	2.23	2.10	1.95	2.23	2.10	ns
LVC MOS25, Slow, 16 mA	0.57	0.66	0.70	2.05	2.29	2.21	2.05	2.29	2.21	ns
LVC MOS25, Slow, 24 mA	0.57	0.66	0.70	1.82	2.24	1.98	1.82	2.24	1.98	ns
LVC MOS25, Fast, 2 mA	0.57	0.66	0.70	5.49	6.04	5.62	5.49	6.04	5.62	ns
LVC MOS25, Fast, 4 mA	0.57	0.66	0.70	3.50	3.82	3.65	3.50	3.82	3.65	ns
LVC MOS25, Fast, 6 mA	0.57	0.66	0.70	2.73	2.99	2.88	2.73	2.99	2.88	ns
LVC MOS25, Fast, 8 mA	0.57	0.66	0.70	2.33	2.65	2.53	2.33	2.65	2.53	ns
LVC MOS25, Fast, 12 mA	0.57	0.66	0.70	1.88	2.08	2.03	1.88	2.08	2.03	ns

Table 50: OLOGIC Switching Characteristics

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup/Hold							
T _{ODCK} /T _{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.45/ −0.08	0.50/ −0.08	0.54/ −0.08	0.54/ −0.08	0.69/ −0.11	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.17/ −0.03	0.20/ −0.03	0.22/ −0.03	0.27/ −0.05	0.27/ −0.04	ns
T _{OSRCK} /T _{OCKSR}	SR pin Setup/Hold with respect to CLK	0.59/ −0.24	0.62/ −0.24	0.54/ −0.08	0.54/ −0.08	0.79/ −0.35	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.44/ −0.07	0.51/ −0.07	0.56/ −0.07	0.60/ −0.10	0.68/ −0.13	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.15/ −0.04	0.19/ −0.04	0.21/ −0.04	0.27/ −0.05	0.29/ −0.05	ns
Combinatorial							
T _{DOQ}	D1 to OQ out or T1 to TQ out	0.78	0.87	1.01	1.01	1.15	ns
Sequential Delays							
T _{OCKQ}	CLK to OQ/TQ out	0.54	0.61	0.71	0.71	0.80	ns
T _{RQ}	SR pin to OQ/TQ out	0.80	0.90	1.05	1.05	1.19	ns
T _{GSRQ}	Global Set/Reset to Q outputs	7.60	7.60	10.51	10.51	10.51	ns
Set/Reset							
T _{RPW}	Minimum Pulse Width, SR inputs	0.78	0.95	1.20	1.20	1.30	ns, Min

Input/Output Delay Switching Characteristics

Table 53: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
IDELAYCTRL						
T _{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3.00	3.00	3.00	3.25	μs
F _{IDELAYCTRL_REF}	REFCLK frequency = 200.0 ⁽¹⁾	200	200	200	200	MHz
	REFCLK frequency = 300.0 ⁽¹⁾	300	300	–	–	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
T _{IDELAYCTRL_RPW}	Minimum Reset pulse width	50.00	50.00	50.00	52.50	ns
IODELAY						
T _{IDELAYRESOLUTION}	IODELAY Chain Delay Resolution	1/(32 x 2 x F _{REF})				ps
T _{IDELAYPAT_JIT}	Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾	0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). ⁽³⁾	±5	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). ⁽⁴⁾	±9	±9	±9	±9	ps per tap
T _{IODELAY_CLK_MAX}	Maximum frequency of CLK input to IDELAY	500.00	420.00	300.00	300.00	MHz
T _{IODCCK_CE} / T _{IODCKC_CE}	CE pin Setup/Hold with respect to CK	0.45/ –0.09	0.53/ –0.09	0.65/ –0.09	0.84/ –0.14	ns
T _{IODCK_INC} / T _{IODCKC_INC}	INC pin Setup/Hold with respect to CK	0.23/ –0.02	0.27/ –0.01	0.31/ 0.00	0.27/ –0.04	ns
T _{IODCCK_RST} / T _{IODCKC_RST}	RST pin Setup/Hold with respect to CK	0.57/ –0.08	0.62/ –0.08	0.69/ –0.08	0.74/ –0.13	ns
T _{IODDO_T}	TSCONTROL delay to MUXE/MUXF switching and through IDELAY	Note 5	Note 5	Note 5	Note 5	ps
T _{IODDO_IDATAIN}	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	ps
T _{IODDO_ODATAIN}	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See TRACE report for actual values.

CLB Switching Characteristics

Table 54: CLB Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Combinatorial Delays						
T _{ILO}	An – Dn LUT address to A	0.06	0.07	0.07	0.09	ns, Max
	An – Dn LUT address to AMUX/CMUX	0.18	0.20	0.22	0.25	ns, Max
	An – Dn LUT address to BMUX_A	0.28	0.31	0.36	0.40	ns, Max

Block RAM and FIFO Switching Characteristics

Table 57: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Block RAM and FIFO Clock-to-Out Delays						
T _{RCKO_DO} and T _{RCKO_DO_REG} ⁽¹⁾	Clock CLK to DOUT output (without output register) ⁽²⁾⁽³⁾	1.60	1.79	2.08	2.36	ns, Max
	Clock CLK to DOUT output (with output register) ⁽⁴⁾⁽⁵⁾	0.60	0.66	0.75	0.83	ns, Max
T _{RCKO_DO_ECC} and T _{RCKO_DO_ECC_REG}	Clock CLK to DOUT output with ECC (without output register) ⁽²⁾⁽³⁾	2.62	2.89	3.30	3.73	ns, Max
	Clock CLK to DOUT output with ECC (with output register) ⁽⁴⁾⁽⁵⁾	0.71	0.77	0.86	0.94	ns, Max
T _{RCKO_CASC} and T _{RCKO_CASC_REG}	Clock CLK to DOUT output with Cascade (without output register) ⁽²⁾	2.49	2.77	3.18	3.61	ns, Max
	Clock CLK to DOUT output with Cascade (with output register) ⁽⁴⁾	1.29	1.41	1.58	1.79	ns, Max
T _{RCKO_FLAGS}	Clock CLK to FIFO flags outputs ⁽⁶⁾	0.74	0.81	0.91	0.98	ns, Max
T _{RCKO_POINTERS}	Clock CLK to FIFO pointers outputs ⁽⁷⁾	0.90	0.98	1.09	1.21	ns, Max
T _{RCKO_SDBIT_ECC} and T _{RCKO_SDBIT_ECC_REG}	Clock CLK to BITERR (with output register)	0.62	0.68	0.76	0.82	ns, Max
	Clock CLK to BITERR (without output register)	2.21	2.46	2.84	3.23	ns, Max
T _{RCKO_PARITY_ECC}	Clock CLK to ECCPARITY in ECC encode only mode	0.86	0.94	1.06	1.18	ns, Max
T _{RCKO_RDADDR_ECC} and T _{RCKO_RDADDR_ECC_REG}	Clock CLK to RDADDR output with ECC (without output register)	0.73	0.79	0.90	1.00	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.76	0.82	0.92	1.02	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{RCKC_ADDR} /T _{RCKC_ADDR}	ADDR inputs ⁽⁸⁾	0.47/ 0.27	0.53/ 0.29	0.62/ 0.32	0.66/ 0.34	ns, Min
T _{RDCK_DI} /T _{RCKD_DI}	DIN inputs ⁽⁹⁾	0.84/ 0.30	0.95/ 0.32	1.11/ 0.34	1.26/ 0.36	ns, Min
T _{RDCK_DI_ECC} /T _{RCKD_DI_ECC}	DIN inputs with block RAM ECC in standard mode ⁽⁹⁾	0.47/ 0.30	0.52/ 0.32	0.59/ 0.34	0.68/ 0.36	ns, Min
	DIN inputs with block RAM ECC encode only ⁽⁹⁾	0.68/ 0.30	0.75/ 0.32	0.85/ 0.34	0.97/ 0.36	ns, Min
	DIN inputs with FIFO ECC in standard mode ⁽⁹⁾	0.77/ 0.30	0.87/ 0.32	1.02/ 0.34	1.16/ 0.36	ns, Min
T _{RCKC_CLK} /T _{RCKC_CLK}	Inject single/double bit error in ECC mode	0.90/ 0.27	1.02/ 0.28	1.20/ 0.29	1.56/ 0.29	ns, Min
T _{RCKC_RDEN} /T _{RCKC_RDEN}	Block RAM Enable (EN) input	0.31/ 0.26	0.35/ 0.27	0.41/ 0.30	0.44/ 0.31	ns, Min
T _{RCKC_REGCE} /T _{RCKC_REGCE}	CE input of output register	0.18/ 0.25	0.19/ 0.27	0.22/ 0.31	0.24/ 0.33	ns, Min
T _{RCKC_RSTREG} /T _{RCKC_RSTREG}	Synchronous RSTREG input	0.22/ 0.23	0.24/ 0.24	0.28/ 0.26	0.31/ 0.27	ns, Min
T _{RCKC_RSTRAM} /T _{RCKC_RSTRAM}	Synchronous RSTRAM input	0.32/ 0.23	0.36/ 0.24	0.41/ 0.27	0.46/ 0.29	ns, Min

Table 62: Regional Clock Switching Characteristics (BUFR) (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BRDO_O}	Propagation delay from CLR to O	0.69	0.74	0.80	1.12	ns
Maximum Frequency						
$F_{MAX}^{(1)}$	Regional clock tree (BUFR)	500	420	300	300	MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

Table 63: Horizontal Clock Buffer Switching Characteristics (BUFH)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	0.15	ns
T_{BHCK_CE}/T_{BHCK_CE}	CE pin Setup and Hold	0.04/ 0.04	0.04/ 0.04	0.05/ 0.05	0.04/ 0.04	ns
Maximum Frequency						
F_{MAX}	Horizontal clock buffer (BUFH)	800	750	700	667	MHz

MMCM Switching Characteristics

Table 64: MMCM Specification

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F_{INMAX}	Maximum Input Clock Frequency ⁽¹⁾	800	750	700	700	MHz
F_{INMIN}	Minimum Input Clock Frequency	10	10	10	10	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
$F_{INDUTY}^{(2)}$	Allowable Input Duty Cycle: 10—49 MHz	25/75				%
	Allowable Input Duty Cycle: 50—199 MHz	30/70				%
	Allowable Input Duty Cycle: 200—399 MHz	35/65				%
	Allowable Input Duty Cycle: 400—499 MHz	40/60				%
	Allowable Input Duty Cycle: >500 MHz	45/55				%
F_{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	0.01	0.01	MHz
F_{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	550	500	450	450	MHz
F_{VCOMIN}	Minimum MMCM VCO Frequency	600	600	600	600	MHz
F_{VCOMAX}	Maximum MMCM VCO Frequency	1600	1440	1200	1200	MHz
$F_{BANDWIDTH}$	Low MMCM Bandwidth at Typical ⁽³⁾	1.00	1.00	1.00	1.00	MHz
	High MMCM Bandwidth at Typical ⁽³⁾	4.00	4.00	4.00	4.00	MHz
$T_{STATPHAOFFSET}$	Static Phase Offset of the MMCM Outputs ⁽⁴⁾	0.12	0.12	0.12	0.12	ns
$T_{OUTJITTER}$	MMCM Output Jitter ⁽⁵⁾	Note 3				
$T_{OUTDUTY}$	MMCM Output Clock Duty Cycle Precision ⁽⁶⁾	0.15	0.20	0.20	0.20	ns
$T_{LOCKMAX}$	MMCM Maximum Lock Time	100	100	100	100	μs
F_{OUTMAX}	MMCM Maximum Output Frequency	800	750	700	700	MHz
F_{OUTMIN}	MMCM Minimum Output Frequency ⁽⁷⁾⁽⁸⁾	4.69	4.69	4.69	4.69	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				

Table 66: Global Clock Input to Output Delay With MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> MMCM.							
T _{ICKOFFMMCMGC}	Global Clock Input and OUTFF <i>with</i> MMCM	XC6VLX75T	2.34	2.50	2.77	2.85	ns
		XC6VLX130T	2.35	2.51	2.78	2.87	ns
		XC6VLX195T	2.36	2.52	2.79	2.88	ns
		XC6VLX240T	2.36	2.52	2.79	2.88	ns
		XC6VLX365T	2.37	2.53	2.79	2.89	ns
		XC6VLX550T	N/A	2.55	2.82	2.93	ns
		XC6VLX760	N/A	2.54	2.82	2.92	ns
		XC6VSX315T	2.35	2.51	2.79	2.87	ns
		XC6VSX475T	N/A	2.43	2.70	2.79	ns
		XC6VHX250T	2.36	2.53	2.80	N/A	ns
		XC6VHX255T	2.46	2.63	2.91	N/A	ns
		XC6VHX380T	2.39	2.59	2.83	N/A	ns
		XC6VHX565T	N/A	2.54	2.81	N/A	ns
		XQ6VLX130T	N/A	2.51	2.78	2.87	ns
		XQ6VLX240T	N/A	2.52	2.79	2.88	ns
		XQ6VLX550T	N/A	N/A	2.82	2.93	ns
		XQ6VSX315T	N/A	2.51	2.79	2.87	ns
		XQ6VSX475T	N/A	N/A	2.70	2.79	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 70: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard. ⁽¹⁾							
T _{PSMMCMCC} / T _{PHMMCMCC}	No Delay Clock-capable Clock Input and IFF ⁽²⁾ with MMCM	XC6VLX75T	1.56/ −0.25	1.69/ −0.25	1.86/ −0.25	1.91/ −0.15	ns
		XC6VLX130T	1.64/ −0.25	1.78/ −0.25	1.95/ −0.25	2.00/ −0.14	ns
		XC6VLX195T	1.65/ −0.24	1.79/ −0.24	1.96/ −0.24	2.01/ −0.15	ns
		XC6VLX240T	1.65/ −0.24	1.79/ −0.24	1.96/ −0.24	2.01/ −0.15	ns
		XC6VLX365T	1.66/ −0.25	1.79/ −0.25	1.97/ −0.25	2.02/ −0.15	ns
		XC6VLX550T	N/A	1.97/ −0.24	2.16/ −0.24	2.19/ −0.14	ns
		XC6VLX760	N/A	2.39/ −0.20	2.63/ −0.20	2.21/ −0.10	ns
		XC6VSX315T	1.67/ −0.25	1.80/ −0.25	1.98/ −0.25	2.03/ −0.16	ns
		XC6VSX475T	N/A	1.98/ −0.29	2.17/ −0.29	2.21/ −0.20	ns
		XC6VHX250T	1.63/ −0.24	1.76/ −0.24	1.94/ −0.24	N/A	ns
		XC6VHX255T	1.63/ −0.19	1.76/ −0.19	1.99/ −0.19	N/A	ns
		XC6VHX380T	1.80/ −0.23	1.94/ −0.23	2.13/ −0.23	N/A	ns
		XC6VHX565T	N/A	1.94/ −0.08	2.13/ −0.08	N/A	ns
		XQ6VLX130T	N/A	1.78/ −0.25	1.95/ −0.25	2.00/ −0.14	ns
		XQ6VLX240T	N/A	1.79/ −0.24	1.96/ −0.24	2.01/ −0.15	ns
		XQ6VLX550T	N/A	N/A	2.16/ −0.24	2.19/ −0.14	ns
		XQ6VSX315T	N/A	1.80/ −0.25	1.98/ −0.25	2.03/ −0.16	ns
		XQ6VSX475T	N/A	N/A	2.17/ −0.29	2.21/ −0.20	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 FPGA clock transmitter and receiver data-valid windows.

Table 71: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion ⁽¹⁾	All	0.12	0.12	0.12	0.12	ns
T_{CKSKEW}	Global Clock Tree Skew ⁽²⁾	XC6VLX75T	0.15	0.16	0.18	0.17	ns
		XC6VLX130T	0.25	0.26	0.29	0.28	ns
		XC6VLX195T	0.26	0.27	0.31	0.30	ns
		XC6VLX240T	0.26	0.27	0.31	0.30	ns
		XC6VLX365T	0.28	0.29	0.31	0.31	ns
		XC6VLX550T	N/A	0.50	0.54	0.54	ns
		XC6VLX760	N/A	0.51	0.56	0.56	ns
		XC6VSX315T	0.27	0.28	0.32	0.30	ns
		XC6VSX475T	N/A	0.39	0.44	0.42	ns
		XC6VHX250T	0.25	0.26	0.29	N/A	ns
		XC6VHX255T	0.35	0.37	0.41	N/A	ns
		XC6VHX380T	0.45	0.47	0.52	N/A	ns
		XC6VHX565T	N/A	0.46	0.51	N/A	ns
		XQ6VLX130T	N/A	0.26	0.29	0.28	ns
		XQ6VLX240T	N/A	0.27	0.31	0.30	ns
		XQ6VLX550T	N/A	N/A	0.54	0.54	ns
		XQ6VSX315T	N/A	0.28	0.32	0.30	ns
		XQ6VSX475T	N/A	N/A	0.44	0.42	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.08	0.08	0.08	0.08	ns
T_{BUFIO_SKEW}	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	0.02	ns
T_{BUFIO_SKEW2}	I/O clock tree skew across three clock regions	All	0.10	0.12	0.23	0.12	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	ns

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 72: Package Skew

Symbol	Description	Device	Package	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	XC6VLX75T	FF484	95	ps
			FF784	146	ps
		XC6VLX130T	FF484	95	ps
			FF784	146	ps
			FF1156	165	ps
		XC6VLX195T	FF784	145	ps
			FF1156	182	ps
		XC6VLX240T	FF784	146	ps
			FF1156	182	ps
			FF1759	187	ps
		XC6VLX365T	FF1156	189	ps
			FF1759	184	ps
		XC6VLX550T	FF1759	196	ps
			FF1760	249	ps
		XC6VLX760	FF1760	236	ps
		XC6VSX315T	FF1156	168	ps
			FF1759	190	ps
		XC6VSX475T	FF1156	168	ps
			FF1759	204	ps
		XC6VHX250T	FF1154	166	ps
		XC6VHX255T	FF1155	168	ps
			FF1923	228	ps
		XC6VHX380T	FF1154	159	ps
			FF1155	172	ps
			FF1923	227	ps
			FF1924	220	ps
		XC6VHX565T	FF1923	232	ps
			FF1924	197	ps
		XQ6VLX130T	RF784	146	ps
			RF1156	165	ps
			FFG1156	165	ps
		XQ6VLX240T	RF784	146	ps
			RF1156	182	ps
			FFG1156	182	ps
			RF1759	187	ps
		XQ6VLX550T	RF1759	196	ps
		XQ6VSX315T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	190	ps
		XQ6VSX475T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	204	ps

Notes:

- These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
- Package trace length information is available for these device/package combinations. This information can be used to deskew the package.