# AMD Xilinx - XC6VHX380T-2FFG1923I Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 29880 |
| Number of Logic Elements/Cells | 382464 |
| Total RAM Bits | 28311552 |
| Number of I/O | 720 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.05V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1924-BBGA, FCBGA |
| Supplier Device Package | 1924-FCBGA (45x45) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc6vhx380t-2ffg1923i |

*Table 4:* **Typical Quiescent Supply Current *(Cont'd)***

| Symbol | Description | Device | Speed and Temperature Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | -3 (C) | -2 (C, E, & I) | -1 (C & I) | -1 (I & M)(2) | -1L (C) | -1L (I)(1) | |
| $I_{CCAUXQ}$ | Quiescent $V_{CCAUX}$ supply current | XC6VLX75T | 45 | 45 | 45 | N/A | 45 | 45 | mA |
| | | XC6VLX130T | 75 | 75 | 75 | N/A | 75 | 75 | mA |
| | | XC6VLX195T | 113 | 113 | 113 | N/A | 113 | 113 | mA |
| | | XC6VLX240T | 135 | 135 | 135 | N/A | 135 | 135 | mA |
| | | XC6VLX365T | 191 | 191 | 191 | N/A | 191 | 191 | mA |
| | | XC6VLX550T(3) | N/A | 286 | 286 | N/A | 286 | 286 | mA |
| | | XC6VLX760(3) | N/A | 387 | 387 | N/A | 387 | 387 | mA |
| | | XC6VSX315T | 186 | 186 | 186 | N/A | 186 | 186 | mA |
| | | XC6VSX475T(3) | N/A | 279 | 279 | N/A | 279 | 279 | mA |
| | | XC6VHX250T | 152 | 152 | 152 | N/A | N/A | N/A | mA |
| | | XC6VHX255T | 152 | 152 | 152 | N/A | N/A | N/A | mA |
| | | XC6VHX380T(4) | 227 | 227 | 227 | N/A | N/A | N/A | mA |
| | | XC6VHX565T(5) | N/A | 315 | 315 | N/A | N/A | N/A | mA |
| | | XQ6VLX130T(6) | N/A | 75 | N/A | 75 | N/A | 75 | mA |
| | | XQ6VLX240T(6) | N/A | 135 | N/A | 135 | N/A | 135 | mA |
| | | XQ6VLX550T(7) | N/A | N/A | N/A | 286 | N/A | 286 | mA |
| | | XQ6VSX315T(6) | N/A | 186 | N/A | 186 | N/A | 186 | mA |
| | | XQ6VSX475T(7) | N/A | N/A | N/A | 279 | N/A | 279 | mA |

**Notes:**

1. Typical values are specified at nominal voltage, 85°C junction temperatures ($T_j$). -1 and -2 industrial (I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. -1L industrial temperature range devices have the values specified in this column.
2. Use the XPE tool to calculate 125°C values for -1M temperature range devices.
3. The -2E extended temperature range ($T_j$ = 0°C to +100°C) is only available in these devices. The -2I temperature range ($T_j$ = –40°C to +100°C) is available for all other devices except the XC6VHX565T.
4. The XC6VHX380T is available with both -2E and -2I temperature ranges.
5. The XC6VHX565T is only available in the following temperature ranges: -1C, -1I, -2C, and -2E.
6. The XQ6VLX130T, XQ6VLX240T, and XQ6VSX315T are available in -2I, -1I, -1M, and -1LI temperature ranges.
7. The XQ6VLX550T and the XQ6VSX475T are only available in -1I and -1LI temperature ranges.
8. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
9. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPE or XPower Analyzer (XPA) tools.

## HT DC Specifications (HT_25)

*Table 8:* **HT DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| $V_{OD}$ | Differential Output Voltage for XC devices | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 480 | 600 | 885 | mV |
| | Differential Output Voltage for XQ devices | | 480 | 600 | 930 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ Magnitude | | –15 | – | 15 | mV |
| $V_{OCM}$ | Output Common Mode Voltage | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 440 | 600 | 760 | mV |
| $\Delta V_{OCM}$ | Change in $V_{OCM}$ Magnitude | | –15 | – | 15 | mV |
| $V_{ID}$ | Input Differential Voltage | | 200 | 600 | 1000 | mV |
| $\Delta V_{ID}$ | Change in $V_{ID}$ Magnitude | | –15 | – | 15 | mV |
| $V_{ICM}$ | Input Common Mode Voltage | | 440 | 600 | 780 | mV |
| $\Delta V_{ICM}$ | Change in $V_{ICM}$ Magnitude | | –15 | – | 15 | mV |

## LVDS DC Specifications (LVDS_25)

*Table 9:* **LVDS DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| $V_{OH}$ | Output High Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | – | – | 1.675 | V |
| $V_{OL}$ | Output Low Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 0.825 | – | – | V |
| $V_{ODIFF}$ | Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 247 | 350 | 600 | mV |
| $V_{OCM}$ | Output Common-Mode Voltage for XC devices | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.075 | 1.250 | 1.425 | V |
| | Output Common-Mode Voltage for XQ devices | | 1.000 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | | 100 | 350 | 600 | mV |
| $V_{ICM}$ | Input Common-Mode Voltage | | 0.3 | 1.2 | 2.2 | V |

## Extended LVDS DC Specifications (LVDSEXT_25)

*Table 10:* **Extended LVDS DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| $V_{OH}$ | Output High Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | – | – | 1.785 | V |
| $V_{OL}$ | Output Low Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 0.715 | – | – | V |
| $V_{ODIFF}$ | Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High for XC devices | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 350 | – | 840 | mV |
| | Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High for XQ devices | | 350 | – | 850 | mV |
| $V_{OCM}$ | Output Common-Mode Voltage for XC devices | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.075 | 1.250 | 1.425 | V |
| | Output Common-Mode Voltage for XQ devices | | 1.000 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | Common-mode input voltage = 1.25V | 100 | – | 1000 | mV |
| $V_{ICM}$ | Input Common-Mode Voltage | Differential input voltage = ±350 mV | 0.3 | 1.2 | 2.2 | V |

## LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The $V_{OH}$ levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 11 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see UG361: *Virtex-6 FPGA SelectIO Resources User Guide*.

*Table 11:* **LVPECL DC Specifications**

| Symbol | DC Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | $V_{CC}$ – 1.025 | 1.545 | $V_{CC}$ – 0.88 | V |
| $V_{OL}$ | Output Low Voltage | $V_{CC}$ – 1.81 | 0.795 | $V_{CC}$ – 1.62 | V |
| $V_{ICM}$ | Input Common-Mode Voltage | 0.6 | – | 2.2 | V |
| $V_{IDIFF}$ | Differential Input Voltage(1)(2) | 0.100 | – | 1.5 | V |

**Notes:**

1. Recommended input maximum voltage not to exceed $V_{CCAUX}$ + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

## eFUSE Read Endurance

Table 12 lists the maximum number of read cycle operations expected. For more information, see UG360:*Virtex-6 FPGA Configuration User Guide*.

*Table 12:* **eFUSE Read Endurance**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| DNA_CYCLES | Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations. | 30,000,000 | | | | Read Cycles |
| AES_CYCLES | Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations. | 30,000,000 | | | | Read Cycles |

# GTX Transceiver Specifications

## GTX Transceiver DC Characteristics

*Table 13:* **Absolute Maximum Ratings for GTX Transceivers(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| MGTAVCC | Analog supply voltage for the GTX transmitter and receiver circuits relative to GND | –0.5 | 1.1 | V |
| MGTAVTT | Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND | –0.5 | 1.32 | V |
| MGTAVTTRCAL | Analog supply voltage for the resistor calibration circuit of the GTX transceiver column | –0.5 | 1.32 | V |
| $V_{IN}$ | Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage | –0.5 | 1.32 | V |
| $V_{MGTREFCLK}$ | Reference clock absolute input voltage | –0.5 | 1.32 | V |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

*Table 14:* **Recommended Operating Conditions for GTX Transceivers(1)(2)**

| Symbol | Description | Speed Grade | PLL Frequency | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| MGTAVCC | Analog supply voltage for the GTX transmitter and receiver circuits relative to GND | -3, -2(3) | > 2.7 GHz | 1.0 | 1.03 | 1.06 | V |
| | | -3, -2(3) | ≤ 2.7 GHz | 0.95 | 1.0 | 1.06 | V |
| | | -1 | ≤ 2.7 GHz | 0.95 | 1.0 | 1.06 | V |
| | | -1L | ≤ 2.7 GHz | 0.95 | 1.0 | 1.05 | V |
| MGTAVTT | Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND | All | – | 1.14 | 1.2 | 1.26 | V |
| MGTAVTTRCAL | Analog supply voltage for the resistor calibration circuit of the GTX transceiver column | All | – | 1.14 | 1.2 | 1.26 | V |

**Notes:**

1. Each voltage listed requires the filter circuit described in UG366: *Virtex-6 FPGA GTX Transceivers User Guide*.
2. Voltages are specified for the temperature range of $T_j$ = –40°C to +100°C for all XC devices and $T_j$ = –55°C to +125°C for the XQ devices
3. If a GTX Quad contains transceivers operating with a mixture of PLL frequencies above and below 2.7 GHz, the MGTAVCC voltage supply must be in the range of 1.0V to 1.06V.

*Table 15:* **GTX Transceiver Supply Current (per Lane) (1)(2)**

| Symbol | Description | Typ | Max | Units |
|---|---|---|---|---|
| $I_{MGTAVTT}$ | MGTAVTT supply current for one GTX transceiver | 55.9 | Note 2 | mA |
| $I_{MGTAVCC}$ | MGTAVCC supply current for one GTX transceiver | 56.1 | | mA |
| $MGTR_{REF}$ | Precision reference resistor for internal calibration termination | 100.0 ± 1% tolerance | | Ω |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
2. Values for currents of other transceiver configurations and conditions can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

*Table 23:* **GTX Transceiver Transmitter Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTXTX}$ | Serial data rate range | | 0.480 | – | $F_{GTXMAX}$ | Gb/s |
| $T_{RTX}$ | TX Rise time | 20%–80% | – | 120 | – | ps |
| $T_{FTX}$ | TX Fall time | 80%–20% | – | 120 | – | ps |
| $T_{LLSKEW}$ | TX lane-to-lane skew(1) | | – | – | 350 | ps |
| $V_{TXOOBVDPP}$ | Electrical idle amplitude | | – | – | 15 | mV |
| $T_{TXOOBTRANSITION}$ | Electrical idle transition time | | – | – | 75 | ns |
| $TJ_{6.5}$ | Total Jitter(2)(3) | 6.5 Gb/s | – | – | 0.33 | UI |
| $DJ_{6.5}$ | Deterministic Jitter(2)(3) | | – | – | 0.17 | UI |
| $TJ_{5.0}$ | Total Jitter(2)(3) | 5.0 Gb/s | – | – | 0.33 | UI |
| $DJ_{5.0}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{4.25}$ | Total Jitter(2)(3) | 4.25 Gb/s | – | – | 0.33 | UI |
| $DJ_{4.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.14 | UI |
| $TJ_{3.75}$ | Total Jitter(2)(3) | 3.75 Gb/s | – | – | 0.34 | UI |
| $DJ_{3.75}$ | Deterministic Jitter(2)(3) | | – | – | 0.16 | UI |
| $TJ_{3.125}$ | Total Jitter(2)(3) | 3.125 Gb/s | – | – | 0.2 | UI |
| $DJ_{3.125}$ | Deterministic Jitter(2)(3) | | – | – | 0.1 | UI |
| $TJ_{3.125L}$ | Total Jitter(2)(3) | 3.125 Gb/s(4) | – | – | 0.35 | UI |
| $DJ_{3.125L}$ | Deterministic Jitter(2)(3) | | – | – | 0.16 | UI |
| $TJ_{2.5}$ | Total Jitter(2)(3) | 2.5 Gb/s(5) | – | – | 0.20 | UI |
| $DJ_{2.5}$ | Deterministic Jitter(2)(3) | | – | – | 0.08 | UI |
| $TJ_{1.25}$ | Total Jitter(2)(3) | 1.25 Gb/s(6) | – | – | 0.15 | UI |
| $DJ_{1.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.06 | UI |
| $TJ_{600}$ | Total Jitter(2)(3) | 600 Mb/s | – | – | 0.1 | UI |
| $DJ_{600}$ | Deterministic Jitter(2)(3) | | – | – | 0.03 | UI |
| $TJ_{480}$ | Total Jitter(2)(3) | 480 Mb/s | – | – | 0.1 | UI |
| $DJ_{480}$ | Deterministic Jitter(2)(3) | | – | – | 0.03 | UI |

**Notes:**

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
2. Using PLL_DIVSEL_FB = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 1.5625 GHz and OUTDIV = 1.
5. PLL frequency at 2.5 GHz and OUTDIV = 2.
6. PLL frequency at 2.5 GHz and OUTDIV = 4.

# GTH Transceiver Specifications

## GTH Transceiver DC Characteristics

*Table 25:* **Absolute Maximum Ratings for GTH Transceivers**(1)

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| MGTHAVCC | Analog supply voltage for the GTH transmitter, receiver, and common analog circuits | –0.5 | 1.125 | V |
| MGTHAVCCRX | Analog supply voltage for the GTH receiver circuits and common analog circuits | –0.5 | 1.125 | V |
| MGTHAVTT | Analog supply voltage for the GTH transmitter termination circuits | –0.5 | 1.32 | V |
| MGTHAVCCPLL | Analog supply voltage for the GTH receiver and PLL circuits | –0.5 | 1.935 | V |
| $V_{IN}$ | Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage | –0.5 | 1.125 | V |
| $V_{MGTREFCLK}$ | Reference clock absolute input voltage | –0.5 | 1.935 | V |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

*Table 26:* **Recommended Operating Conditions for GTH Transceivers** (1)(2)

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| MGTHAVCC | Analog supply voltage for the GTH transmitter, receiver, and common analog circuits | 1.075 | 1.1 | 1.125 | V |
| MGTHAVCCRX | Analog supply voltage for the GTH receiver circuits and common analog circuits | 1.075 | 1.1 | 1.125 | V |
| MGTHAVTT | Analog supply voltage for the GTH transmitter termination circuits | 1.140 | 1.2 | 1.26 | V |
| MGTHAVCCPLL | Analog supply voltage for the GTH receiver and PLL circuit | 1.710 | 1.8 | 1.89 | V |

**Notes:**

1. Each voltage listed requires the filter circuit described in UG371: *Virtex-6 FPGA GTH Transceivers User Guide*.
2. Voltages are specified for the temperature range of $T_j$ = –40°C to +100°C.

*Table 27:* **GTH Transceiver Power Supply Sequencing** (1)(2)(3)

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{HAVCC2HAVCCRX}$ | Maximum time between powering MGTHAVCC to when MGTHAVCCRX must be powered. | 0 | 5 | ms |
| $T_{HAVCCRX2HAVCCPLL}$ | Minimum time between powering MGTHAVCCRX to when MGTHAVCCPLL can be powered. | 10 | – | µs |
| $T_{HAVCCRX2HAVTT}$ | Minimum time between powering MGTHAVCCRX to when MGTHAVTT can be powered. | 10 | – | µs |

**Notes:**

1. MGTHAVCCRX must be powered simultaneously or within $T_{HAVCC2HAVCCRX}$ of MGTHAVCC, but it must not precede MGTHAVCC.
2. MGTHAVCC and MGTHAVCCRX must be powered before MGTHAVCCPLL and MGTHAVTT. This minimum time is defined by $T_{HAVCCRX2HAVCCPLL}$ and $T_{HAVCCRX2HAVTT}$.
3. At any time, the condition of MGTHAVCC being present and MGTHAVCCRX not being present should not occur for more than the maximum $T_{HAVCC2HAVCCRX}$.

## GTH Transceiver Switching Characteristics

Consult UG371: *Virtex-6 FPGA GTH Transceivers User Guide* for further information.

*Table 32:* **GTH Transceiver Maximum Data Rate and PLL Frequency Range**

| Symbol | Description | Conditions | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | |
| $F_{GTHMAX}$ | Maximum GTH transceiver data rate | PLL Output Divider = 1 | 11.182 | 11.182 | 10.32 | Gb/s |
| | | PLL Output Divider = 4 | 2.795 | 2.795 | 2.58 | Gb/s |
| $F_{GTHMIN}$ | Minimum GTH transceiver data rate(1) | PLL Output Divider = 1 | 9.92 | 9.92 | 9.92 | Gb/s |
| | | PLL Output Divider = 4 | 2.48 | 2.48 | 2.48 | Gb/s |
| $F_{GPLLMAX}$ | Maximum GTH PLL frequency | | 5.591 | 5.591 | 5.16 | GHz |
| $F_{GPLLMIN}$ | Minimum GTH PLL frequency | | 4.96 | 4.96 | 4.96 | GHz |

**Notes:**

1. Lower data rates can be achieved using FPGA logic based oversampling designs.

*Table 33:* **GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1 | |
| $F_{GTHDRPCLK}$ | GTHDRPCLK maximum frequency | 70 | 70 | 60 | MHz |

*Table 34:* **GTH Transceiver Reference Clock Switching Characteristics**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $F_{GCLK}$ | Reference clock frequency range | -1 speed grade | 150 | – | 645 | MHz |
| | | -2 and -3 speed grades | 150 | – | 700 | MHz |
| $T_{RCLK}$ | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| $T_{FCLK}$ | Reference clock fall time | 80% – 20% | – | 200 | – | ps |
| $T_{DCREF}$ | Reference clock duty cycle | CLK | 45 | 50 | 55 | % |
| $T_{LOCK}$ | Clock recovery frequency acquisition time | Initial PLL lock | – | – | 2 | ms |
| $T_{PHASE}$ | Clock recovery phase acquisition time | Lock to data after PLL has locked to the reference clock | – | – | 20 | µs |

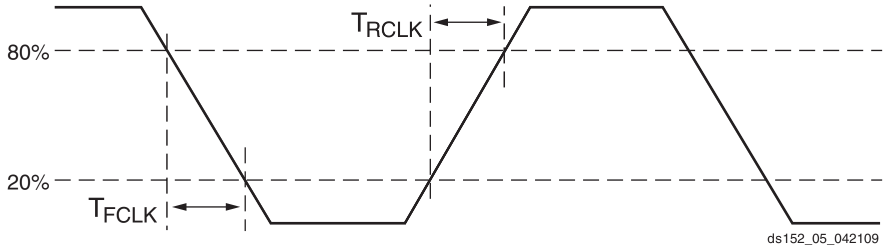

*Figure 5:* **Reference Clock Timing Parameters**

## Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

*Table 39:* **Maximum Performance for PCI Express Designs**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $F_{PIPECLK}$ | Pipe clock maximum frequency | 250 | 250 | 250 | 250 | MHz |
| $F_{USERCLK}$ | User clock maximum frequency | 500 | 500 | 250 | 250 | MHz |
| $F_{DRPCLK}$ | DRP clock maximum frequency | 250 | 250 | 250 | 250 | MHz |

## System Monitor Analog-to-Digital Converter Specification

*Table 40:* **Analog-to-Digital Specifications**

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $AV_{DD}$ = 2.5V ± 5%, $V_{REFP}$ = 1.25V, $V_{REFN}$ = 0V, ADCCLK = 5.2 MHz, $T_j$ = –55°C to 125°C M-Grade, Typical values at $T_j$=+35°C | | | | | | |
| **DC Accuracy:** All external input channels. Both unipolar and bipolar modes. | | | | | | |
| Resolution | | | 10 | – | – | Bits |
| Integral Nonlinearity | INL | | – | – | ±1 | LSBs |
| Differential Nonlinearity | DNL | No missing codes ($T_{MIN}$ to $T_{MAX}$)<br>Guaranteed Monotonic | – | – | ±0.9 | LSBs |
| Unipolar Offset Error (1) | | Uncalibrated | – | ±2 | ±30 | LSBs |
| Bipolar Offset Error (1) | | Uncalibrated measured in bipolar mode | – | ±2 | ±30 | LSBs |
| Gain Error | | Uncalibrated - External Reference | – | ±0.2 | ±2 | % |
| | | Uncalibrated - Internal Reference | – | ±2 | – | % |
| Bipolar Gain Error (1) | | Uncalibrated - External Reference | – | ±0.2 | ±2 | % |
| | | Uncalibrated - Internal Reference | – | ±2 | – | % |
| Total Unadjusted Error (Uncalibrated) | TUE | Deviation from ideal transfer function. External 1.25V reference | – | ±10 | – | LSBs |
| | | Deviation from ideal transfer function. Internal reference | – | ±20 | – | LSBs |
| Total Unadjusted Error (Calibrated) | TUE | Deviation from ideal transfer function. External 1.25V reference | – | ±1 | ±2 | LSBs |
| Calibrated Gain Temperature Coefficient | | Variation of FS code with temperature | – | ±0.01 | – | LSB/°C |
| DC Common-Mode Reject | $CMRR_{DC}$ | $V_N = V_{CM}$ = 0.5V ± 0.5V,<br>$V_P – V_N$ = 100mV | – | 70 | – | dB |
| **Conversion Rate**(2) | | | | | | |
| Conversion Time - Continuous | $t_{CONV}$ | Number of CLK cycles | 26 | – | 32 | |
| Conversion Time - Event | $t_{CONV}$ | Number of CLK cycles | – | – | 21 | |
| T/H Acquisition Time | $t_{ACQ}$ | Number of CLK cycles | 4 | – | – | |
| DRP Clock Frequency | DCLK | DRP clock frequency | 8 | – | 80 | MHz |
| ADC Clock Frequency | ADCCLK | Derived from DCLK | 1 | – | 5.2 | MHz |
| CLK Duty cycle | | | 40 | – | 60 | % |

*Table 40:* **Analog-to-Digital Specifications *(Cont'd)***

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Analog Inputs**[3] | | | | | | |
| Dedicated Analog Inputs Input Voltage Range<br>$V_P$ - $V_N$ | | Unipolar Operation | 0 | – | 1 | Volts |
| | | Bipolar Operation | –0.5 | – | +0.5 | |
| | | Unipolar Common Mode Range (FS input) | 0 | – | +0.5 | |
| | | Bipolar Common Mode Range (FS input) | +0.5 | – | +0.6 | |
| | | Bandwidth | – | 20 | – | MHz |
| Auxiliary Analog Inputs Input Voltage Range<br>$V_{AUXP[0]}$ /$V_{AUXN[0]}$ to $V_{AUXP[15]}$ /$V_{AUXN[15]}$<br>$T_j$ = –55°C to 125°C | | Unipolar Operation | 0 | – | 1 | Volts |
| | | Bipolar Operation | –0.5 | – | +0.5 | |
| | | Unipolar Common Mode Range (FS input) | 0 | – | +0.5 | |
| | | Bipolar Common Mode Range (FS input) | +0.5 | – | +0.6 | |
| | | Bandwidth | – | 10 | – | kHz |
| Input Leakage Current | | A/D not converting, ADCCLK stopped | – | ±1.0 | – | µA |
| Input Capacitance | | | – | 10 | – | pF |
| On-chip Supply Monitor Error | | $V_{CCINT}$ and $V_{CCAUX}$ with calibration enabled. External 1.25V reference $T_j$ = –55°C to 125°C. | – | – | ±1.0 | % Reading |
| | | $V_{CCINT}$ and $V_{CCAUX}$ with calibration enabled. Internal reference $T_j$ = –40°C to 100°C.[4] | – | ±2 | – | % Reading |
| On-chip Temperature Monitor Error | | $T_j$ = –55°C to +125°C with calibration enabled. External 1.25V reference. | – | – | ±4 | °C |
| | | $T_j$ = –40°C to +100°C with calibration enabled. Internal reference.[4] | – | ±5 | – | °C |
| **External Reference Inputs**[5] | | | | | | |
| Positive Reference Input Voltage Range | $V_{REFP}$ | Measured Relative to $V_{REFN}$ | 1.20 | 1.25 | 1.30 | Volts |
| Negative Reference Input Voltage Range | $V_{REFN}$ | Measured Relative to AGND | –50 | 0 | 100 | mV |
| Input current | $I_{REF}$ | ADCCLK = 5.2 MHz | – | – | 100 | µA |
| **Power Requirements** | | | | | | |
| Analog Power Supply | $AV_{DD}$ | Measured Relative to $AV_{SS}$ | 2.375 | 2.5 | 2.625 | Volts |
| Analog Supply Current | $AI_{DD}$ | ADCCLK = 5.2 MHz | – | – | 12 | mA |

**Notes:**

1. Offset errors are removed by enabling the System Monitor automatic gain calibration feature.
2. See "System Monitor Timing" in UG370: *Virtex-6 FPGA System Monitor User Guide*
3. See "Analog Inputs" in UG370: *Virtex-6 FPGA System Monitor User Guide* for a detailed description.
4. These internal references are not specified over the junction temperature operating range for military (M) temperature devices.
5. Any variation in the reference voltage from the nominal $V_{REFP}$ = 1.25V and $V_{REFN}$ = 0V will result in a deviation from the ideal transfer function.This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

## Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 43 lists the production released Virtex-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE® software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

*Table 43:* **Virtex-6 Device Production Software and Speed Specification Release**

| Device | Speed Grade Designations | | | |
|---|---|---|---|---|
| | -3 | -2 | -1 | -1L |
| XC6VLX75T | ISE 12.2 v1.08 | | | ISE 12.3 v1.07 Patch |
| XC6VLX130T | ISE 12.1 v1.06 | ISE 11.5 v1.05(2) | ISE 11.5 v1.05(2) | ISE 12.2 v1.05 |
| XC6VLX195T | ISE 12.1 v1.06 | ISE 12.1 v1.06 | ISE 12.1 v1.06 | ISE 12.2 v1.04 |
| XC6VLX240T | ISE 12.1 v1.06 | ISE 11.4.1 v1.04(2) | ISE 11.4.1 v1.04(2) | ISE 12.2 v1.04 |
| XC6VLX365T | ISE 12.2 v1.08 | | | ISE 12.2 v1.04 |
| XC6VLX550T | N/A | ISE 12.2 v1.07 | | ISE 12.2 v1.04 |
| XC6VLX760 | N/A | ISE 12.2 v1.08 | | ISE 12.3 v1.07 Patch |
| XC6VSX315T | ISE 12.2 v1.08 | ISE 12.1 v1.06 | | ISE 12.3 v1.07 Patch |
| XC6VSX475T | N/A | ISE 12.2 v1.08 | | ISE 12.3 v1.07 Patch |
| XC6VHX250T | ISE 12.4 v1.10 | | | N/A |
| XC6VHX255T | ISE 13.1 v1.14 using the ISE 13.1 software update | | | N/A |
| XC6VHX380T | ISE 12.4 v1.10 | | | N/A |
| XC6VHX565T | N/A | ISE 13.1 v1.14 using the ISE 13.1 software update | | N/A |
| XQ6VLX130T | N/A | ISE 13.3 v1.17 Patch | | ISE 13.3 v1.10 |
| XQ6VLX240T | N/A | ISE 13.3 v1.17 Patch | | ISE 13.3 v1.10 |
| XQ6VLX550T | N/A | N/A | ISE 13.3 v1.17 Patch | ISE 13.3 v1.10 |
| XQ6VSX315T | N/A | ISE 13.3 v1.17 Patch | | ISE 13.3 v1.10 |
| XQ6VSX475T | N/A | N/A | ISE 13.3 v1.17 Patch | ISE 13.3 v1.10 |

**Notes:**

1. Blank entries indicate a device and/or speed grade in advance or preliminary status.
2. Designs utilizing the GTX transceivers must use the software version ISE 12.1 v1.06 or later.

*Table 44:* **IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | |
| DIFF_SSTL18_I | 0.85 | 0.94 | 1.09 | 1.08 | 1.47 | 1.58 | 1.75 | 1.73 | 1.47 | 1.58 | 1.75 | 1.73 | ns |
| DIFF_SSTL18_I_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.40 | 1.51 | 1.67 | 1.65 | 1.40 | 1.51 | 1.67 | 1.65 | ns |
| DIFF_SSTL18_II | 0.85 | 0.94 | 1.09 | 1.08 | 1.39 | 1.50 | 1.67 | 1.66 | 1.39 | 1.50 | 1.67 | 1.66 | ns |
| DIFF_SSTL18_II_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.36 | 1.47 | 1.63 | 1.62 | 1.36 | 1.47 | 1.63 | 1.62 | ns |
| DIFF_SSTL18_II_T_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.40 | 1.51 | 1.67 | 1.65 | 1.40 | 1.51 | 1.67 | 1.65 | ns |
| DIFF_SSTL15 | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.71 | 1.69 | 1.42 | 1.54 | 1.71 | 1.69 | ns |
| DIFF_SSTL15_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.41 | 1.52 | 1.68 | 1.66 | 1.41 | 1.52 | 1.68 | 1.66 | ns |
| DIFF_SSTL15_T_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.41 | 1.52 | 1.68 | 1.66 | 1.41 | 1.52 | 1.68 | 1.66 | ns |

*Table 45:* **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices**

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| LVDS_25 | 0.94 | 1.09 | 1.08 | 1.54 | 2.16 | 1.62 | 1.54 | 2.16 | 1.62 | ns |
| LVDSEXT_25 | 0.94 | 1.09 | 1.08 | 1.65 | 2.20 | 1.73 | 1.65 | 2.20 | 1.73 | ns |
| HT_25 | 0.94 | 1.09 | 1.08 | 1.62 | 2.20 | 1.69 | 1.62 | 2.20 | 1.69 | ns |
| BLVDS_25 | 0.94 | 1.09 | 1.08 | 1.50 | 3.18 | 1.65 | 1.50 | 3.18 | 1.65 | ns |
| RSDS_25 (point to point) | 0.94 | 1.09 | 1.08 | 1.54 | 2.22 | 1.62 | 1.54 | 2.22 | 1.62 | ns |
| HSTL_I | 0.91 | 1.06 | 1.06 | 1.56 | 2.44 | 1.71 | 1.56 | 2.44 | 1.71 | ns |
| HSTL_II | 0.91 | 1.06 | 1.06 | 1.56 | 2.21 | 1.72 | 1.56 | 2.21 | 1.72 | ns |
| HSTL_III | 0.91 | 1.06 | 1.06 | 1.54 | 2.50 | 1.69 | 1.54 | 2.50 | 1.69 | ns |
| HSTL_I_18 | 0.91 | 1.06 | 1.06 | 1.58 | 2.43 | 1.72 | 1.58 | 2.43 | 1.72 | ns |
| HSTL_II_18 | 0.91 | 1.06 | 1.06 | 1.62 | 2.30 | 1.78 | 1.62 | 2.30 | 1.78 | ns |
| HSTL_III_18 | 0.91 | 1.06 | 1.06 | 1.54 | 2.49 | 1.69 | 1.54 | 2.49 | 1.69 | ns |
| SSTL2_I | 0.91 | 1.06 | 1.06 | 1.60 | 2.50 | 1.74 | 1.60 | 2.50 | 1.74 | ns |
| SSTL2_II | 0.91 | 1.06 | 1.06 | 1.54 | 2.49 | 1.71 | 1.54 | 2.49 | 1.71 | ns |
| SSTL15 | 0.91 | 1.06 | 1.06 | 1.54 | 2.07 | 1.69 | 1.54 | 2.07 | 1.69 | ns |
| LVCMOS25, Slow, 2 mA | 0.57 | 0.66 | 0.70 | 5.46 | 6.01 | 5.63 | 5.46 | 6.01 | 5.63 | ns |
| LVCMOS25, Slow, 4 mA | 0.57 | 0.66 | 0.70 | 3.49 | 3.79 | 3.65 | 3.49 | 3.79 | 3.65 | ns |
| LVCMOS25, Slow, 6 mA | 0.57 | 0.66 | 0.70 | 2.81 | 3.08 | 2.95 | 2.81 | 3.08 | 2.95 | ns |
| LVCMOS25, Slow, 8 mA | 0.57 | 0.66 | 0.70 | 2.41 | 2.72 | 2.59 | 2.41 | 2.72 | 2.59 | ns |
| LVCMOS25, Slow, 12 mA | 0.57 | 0.66 | 0.70 | 1.95 | 2.23 | 2.10 | 1.95 | 2.23 | 2.10 | ns |
| LVCMOS25, Slow, 16 mA | 0.57 | 0.66 | 0.70 | 2.05 | 2.29 | 2.21 | 2.05 | 2.29 | 2.21 | ns |
| LVCMOS25, Slow, 24 mA | 0.57 | 0.66 | 0.70 | 1.82 | 2.24 | 1.98 | 1.82 | 2.24 | 1.98 | ns |
| LVCMOS25, Fast, 2 mA | 0.57 | 0.66 | 0.70 | 5.49 | 6.04 | 5.62 | 5.49 | 6.04 | 5.62 | ns |
| LVCMOS25, Fast, 4 mA | 0.57 | 0.66 | 0.70 | 3.50 | 3.82 | 3.65 | 3.50 | 3.82 | 3.65 | ns |
| LVCMOS25, Fast, 6 mA | 0.57 | 0.66 | 0.70 | 2.73 | 2.99 | 2.88 | 2.73 | 2.99 | 2.88 | ns |
| LVCMOS25, Fast, 8 mA | 0.57 | 0.66 | 0.70 | 2.33 | 2.65 | 2.53 | 2.33 | 2.65 | 2.53 | ns |
| LVCMOS25, Fast, 12 mA | 0.57 | 0.66 | 0.70 | 1.88 | 2.08 | 2.03 | 1.88 | 2.08 | 2.03 | ns |

*Table 45:* **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| DIFF_SSTL18_II | 0.94 | 1.09 | 1.08 | 1.50 | 2.27 | 1.66 | 1.50 | 2.27 | 1.66 | ns |
| DIFF_SSTL18_II_DCI | 0.94 | 1.09 | 1.08 | 1.47 | 2.20 | 1.62 | 1.47 | 2.20 | 1.62 | ns |
| DIFF_SSTL18_II_T_DCI | 0.94 | 1.09 | 1.08 | 1.51 | 2.30 | 1.65 | 1.51 | 2.30 | 1.65 | ns |
| DIFF_SSTL15 | 0.91 | 1.06 | 1.06 | 1.54 | 2.25 | 1.69 | 1.54 | 2.25 | 1.69 | ns |
| DIFF_SSTL15_DCI | 0.91 | 1.06 | 1.06 | 1.52 | 2.25 | 1.66 | 1.52 | 2.25 | 1.66 | ns |
| DIFF_SSTL15_T_DCI | 0.91 | 1.06 | 1.06 | 1.52 | 2.25 | 1.66 | 1.52 | 2.25 | 1.66 | ns |

*Table 46:* **IOB 3-state ON Output Switching Characteristics ($T_{IOTPHZ}$)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $T_{IOTPHZ}$ | T input to Pad high-impedance | 0.86 | 0.92 | 0.99 | 0.99 | ns |

*Table 50:* **OLOGIC Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| **Setup/Hold** | | | | | | | |
| $T_{ODCK}/T_{OCKD}$ | D1/D2 pins Setup/Hold with respect to CLK | 0.45/<br>–0.08 | 0.50/<br>–0.08 | 0.54/<br>–0.08 | 0.54/<br>–0.08 | 0.69/<br>–0.11 | ns |
| $T_{OOCECK}/T_{OCKOCE}$ | OCE pin Setup/Hold with respect to CLK | 0.17/<br>–0.03 | 0.20/<br>–0.03 | 0.22/<br>–0.03 | 0.27/<br>–0.05 | 0.27/<br>–0.04 | ns |
| $T_{OSRCK}/T_{OCKSR}$ | SR pin Setup/Hold with respect to CLK | 0.59/<br>–0.24 | 0.62/<br>–0.24 | 0.54/<br>–0.08 | 0.54/<br>–0.08 | 0.79/<br>–0.35 | ns |
| $T_{OTCK}/T_{OCKT}$ | T1/T2 pins Setup/Hold with respect to CLK | 0.44/<br>–0.07 | 0.51/<br>–0.07 | 0.56/<br>–0.07 | 0.60/<br>–0.10 | 0.68/<br>–0.13 | ns |
| $T_{OTCECK}/T_{OCKTCE}$ | TCE pin Setup/Hold with respect to CLK | 0.15/<br>–0.04 | 0.19/<br>–0.04 | 0.21/<br>–0.04 | 0.27/<br>–0.05 | 0.29/<br>–0.05 | ns |
| **Combinatorial** | | | | | | | |
| $T_{DOQ}$ | D1 to OQ out or T1 to TQ out | 0.78 | 0.87 | 1.01 | 1.01 | 1.15 | ns |
| **Sequential Delays** | | | | | | | |
| $T_{OCKQ}$ | CLK to OQ/TQ out | 0.54 | 0.61 | 0.71 | 0.71 | 0.80 | ns |
| $T_{RQ}$ | SR pin to OQ/TQ out | 0.80 | 0.90 | 1.05 | 1.05 | 1.19 | ns |
| $T_{GSRQ}$ | Global Set/Reset to Q outputs | 7.60 | 7.60 | 10.51 | 10.51 | 10.51 | ns |
| **Set/Reset** | | | | | | | |
| $T_{RPW}$ | Minimum Pulse Width, SR inputs | 0.78 | 0.95 | 1.20 | 1.20 | 1.30 | ns, Min |

## Input/Output Delay Switching Characteristics

*Table 53:* **Input/Output Delay Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| **IDELAYCTRL** | | | | | | |
| $T_{DLYCCO\_RDY}$ | Reset to Ready for IDELAYCTRL | 3.00 | 3.00 | 3.00 | 3.25 | µs |
| $F_{IDELAYCTRL\_REF}$ | REFCLK frequency = 200.0(1) | 200 | 200 | 200 | 200 | MHz |
| | REFCLK frequency = 300.0(1) | 300 | 300 | – | – | MHz |
| IDELAYCTRL_REF_PRECISION | REFCLK precision | ±10 | ±10 | ±10 | ±10 | MHz |
| $T_{IDELAYCTRL\_RPW}$ | Minimum Reset pulse width | 50.00 | 50.00 | 50.00 | 52.50 | ns |
| **IODELAY** | | | | | | |
| $T_{IDELAYRESOLUTION}$ | IODELAY Chain Delay Resolution | 1/(32 x 2 x $F_{REF}$) | | | | ps |
| $T_{IDELAYPAT\_JIT}$ | Pattern dependent period jitter in delay chain for clock pattern.(2) | 0 | 0 | 0 | 0 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(3) | ±5 | ±5 | ±5 | ±5 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(4) | ±9 | ±9 | ±9 | ±9 | ps per tap |
| $T_{IODELAY\_CLK\_MAX}$ | Maximum frequency of CLK input to IODELAY | 500.00 | 420.00 | 300.00 | 300.00 | MHz |
| $T_{IODCCK\_CE}$ / $T_{IODCKC\_CE}$ | CE pin Setup/Hold with respect to CK | 0.45/<br>–0.09 | 0.53/<br>–0.09 | 0.65/<br>–0.09 | 0.84/<br>–0.14 | ns |
| $T_{IODCK\_INC}$/ $T_{IODCKC\_INC}$ | INC pin Setup/Hold with respect to CK | 0.23/<br>–0.02 | 0.27/<br>–0.01 | 0.31/<br>0.00 | 0.27/<br>–0.04 | ns |
| $T_{IODCCK\_RST}$/ $T_{IODCKC\_RST}$ | RST pin Setup/Hold with respect to CK | 0.57/<br>–0.08 | 0.62/<br>–0.08 | 0.69/<br>–0.08 | 0.74/<br>–0.13 | ns |
| $T_{IODDO\_T}$ | TSCONTROL delay to MUXE/MUXF switching and through IODELAY | Note 5 | Note 5 | Note 5 | Note 5 | ps |
| $T_{IODDO\_IDATAIN}$ | Propagation delay through IODELAY | Note 5 | Note 5 | Note 5 | Note 5 | ps |
| $T_{IODDO\_ODATAIN}$ | Propagation delay through IODELAY | Note 5 | Note 5 | Note 5 | Note 5 | ps |

**Notes:**

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IODELAY tap setting. See TRACE report for actual values.

## CLB Switching Characteristics

*Table 54:* **CLB Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| **Combinatorial Delays** | | | | | | |
| $T_{ILO}$ | An – Dn LUT address to A | 0.06 | 0.07 | 0.07 | 0.09 | ns, Max |
| | An – Dn LUT address to AMUX/CMUX | 0.18 | 0.20 | 0.22 | 0.25 | ns, Max |
| | An – Dn LUT address to BMUX_A | 0.28 | 0.31 | 0.36 | 0.40 | ns, Max |

*Table 57:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $T_{RCCK\_WE}$/$T_{RCKC\_WE}$ | Write Enable (WE) input (Block RAM only) | 0.44/<br>0.19 | 0.47/<br>0.25 | 0.52/<br>0.35 | 0.67/<br>0.24 | ns, Min |
| $T_{RCCK\_WREN}$/$T_{RCKC\_WREN}$ | WREN FIFO inputs | 0.47/<br>0.26 | 0.50/<br>0.27 | 0.55/<br>0.30 | 0.68/<br>0.31 | ns, Min |
| $T_{RCCK\_RDEN}$/$T_{RCKC\_RDEN}$ | RDEN FIFO inputs | 0.46/<br>0.26 | 0.50/<br>0.27 | 0.55/<br>0.30 | 0.67/<br>0.31 | ns, Min |
| **Reset Delays** | | | | | | |
| $T_{RCO\_FLAGS}$ | Reset RST to FIFO Flags/Pointers(10) | 0.90 | 0.98 | 1.10 | 1.23 | ns, Max |
| $T_{RCCK\_RSTREG}$/$T_{RCKC\_RSTREG}$ | FIFO reset timing(11) | 0.22/<br>0.23 | 0.24/<br>0.24 | 0.28/<br>0.26 | 0.31/<br>0.27 | ns, Min |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | Block RAM in TDP and SDP modes (Write First and No Change modes) | 600 | 540 | 450 | 340 | MHz |
| | Block RAM (Read First mode) | 525 | 475 | 400 | 275 | MHz |
| | Block RAM (SDP mode)(12) | 525 | 475 | 400 | 275 | MHz |
| $F_{MAX\_CASCADE}$ | Block RAM Cascade (Write First and No Change modes) | 550 | 490 | 400 | 300 | MHz |
| | Block RAM Cascade (Read First mode) | 475 | 425 | 350 | 235 | MHz |
| $F_{MAX\_FIFO}$ | FIFO in all modes | 600 | 540 | 450 | 340 | MHz |
| $F_{MAX\_ECC}$ | Block RAM and FIFO in ECC configuration | 450 | 400 | 325 | 250 | MHz |

**Notes:**

1. TRACE will report all of these parameters as $T_{RCKO\_DO}$.
2. $T_{RCKO\_DOR}$ includes $T_{RCKO\_DOW}$, $T_{RCKO\_DOPR}$, and $T_{RCKO\_DOPW}$ as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. $T_{RCKO\_DO}$ includes $T_{RCKO\_DOP}$ as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. $T_{RCKO\_FLAGS}$ includes the following parameters: $T_{RCKO\_AEMPTY}$, $T_{RCKO\_AFULL}$, $T_{RCKO\_EMPTY}$, $T_{RCKO\_FULL}$, $T_{RCKO\_RDERR}$, $T_{RCKO\_WRERR}$.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. $T_{RCKO\_DI}$ includes both A and B inputs as well as the parity inputs of A and B.
10. $T_{RCO\_FLAGS}$ includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. The FIFO reset must be asserted for at least three positive clock edges.
12. When using ISE software v12.4 or later, if the RDADDR_COLLISION_HWCONFIG attribute is set to PERFORMANCE or the block RAM is in single-port operation, then the faster $F_{MAX}$ for WRITE_FIRST/NO_CHANGE modes apply.

*Table 58:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| $T_{\text{DSPDO\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}}$ | {PCIN, CARRYCASCIN, MULTSIGNIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output | 1.28 | 1.46 | 1.72 | 1.72 | 2.06 | ns |
| **Clock to Outs from Output Register Clock to Output Pins** | | | | | | | |
| $T_{\text{DSPCKO\_\{P, CARRYOUT\}\_PREG}}$ | CLK (PREG) to {P, CARRYOUT} output | 0.38 | 0.43 | 0.50 | 0.50 | 0.57 | ns |
| $T_{\text{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_PREG}}$ | CLK (PREG) to {CARRYCASCOUT, PCOUT, MULTSIGNOUT} output | 0.50 | 0.56 | 0.66 | 0.66 | 0.76 | ns |
| **Clock to Outs from Pipeline Register Clock to Output Pins** | | | | | | | |
| $T_{\text{DSPCKO\_\{P, CARRYOUT\}\_MREG}}$ | CLK (MREG) to {P, CARRYOUT} output | 1.72 | 1.96 | 2.30 | 2.30 | 2.69 | ns |
| $T_{\text{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MREG}}$ | CLK (MREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output | 1.81 | 2.06 | 2.43 | 2.43 | 2.88 | ns |
| $T_{\text{DSPCKO\_\{P, CARRYOUT\}\_ADREG\_MULT}}$ | CLK (ADREG) to {P, CARRYOUT} output | 2.79 | 3.16 | 3.72 | 3.72 | 4.32 | ns |
| $T_{\text{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_ADREG\_MULT}}$ | CLK (ADREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output | 2.87 | 3.26 | 3.84 | 3.84 | 4.51 | ns |
| **Clock to Outs from Input Register Clock to Output Pins** | | | | | | | |
| $T_{\text{DSPCKO\_\{P, CARRYOUT\}\_\{AREG, BREG\}\_MULT}}$ | CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier | 3.97 | 4.52 | 5.36 | 5.36 | 6.20 | ns |
| $T_{\text{DSPCKO\_\{P, CARRYOUT\}\_\{AREG, BREG\}}}$ | CLK (AREG, BREG) to {P, CARRYOUT} output not using multiplier | 1.70 | 1.93 | 2.27 | 2.27 | 2.65 | ns |
| $T_{\text{DSPCKO\_\{P, CARRYOUT\}\_CREG}}$ | CLK (CREG) to {P, CARRYOUT} output | 1.70 | 1.93 | 2.27 | 2.27 | 2.80 | ns |
| $T_{\text{DSPCKO\_\{P, CARRYOUT\}\_DREG\_MULT}}$ | CLK (DREG) to {P, CARRYOUT} output | 3.89 | 4.44 | 5.25 | 5.25 | 6.07 | ns |
| **Clock to Outs from Input Register Clock to Cascading Output Pins** | | | | | | | |
| $T_{\text{DSPCKO\_\{ACOUT; BCOUT\}\_\{AREG; BREG\}}}$ | CLK (AREG, BREG) to {P, CARRYOUT} output | 0.66 | 0.76 | 0.89 | 0.89 | 1.01 | ns |
| $T_{\text{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_\{AREG, BREG\}\_MULT}}$ | CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier | 4.05 | 4.63 | 5.49 | 5.49 | 6.39 | ns |
| $T_{\text{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_\{AREG, BREG\}}}$ | CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier | 1.79 | 2.03 | 2.40 | 2.40 | 2.84 | ns |
| $T_{\text{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_DREG\_MULT}}$ | CLK (DREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier | 3.98 | 4.54 | 5.38 | 5.38 | 6.26 | ns |
| $T_{\text{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_CREG}}$ | CLK (CREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output | 1.78 | 2.03 | 2.40 | 2.40 | 2.99 | ns |

*Table 58:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| **Maximum Frequency** | | | | | | | |
| $F_{MAX}$ | With all registers used | 600 | 540 | 450 | 450 | 410 | MHz |
| $F_{MAX\_PATDET}$ | With pattern detector | 551 | 483 | 408 | 408 | 356 | MHz |
| $F_{MAX\_MULT\_NOMREG}$ | Two register multiply without MREG | 356 | 311 | 262 | 262 | 224 | MHz |
| $F_{MAX\_MULT\_NOMREG\_PATDET}$ | Two register multiply without MREG with pattern detect | 327 | 286 | 241 | 241 | 211 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG}$ | Without ADREG | 398 | 347 | 292 | 292 | 254 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$ | Without ADREG with pattern detect | 398 | 347 | 292 | 292 | 254 | MHz |
| $F_{MAX\_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG) | 266 | 233 | 196 | 196 | 171 | MHz |
| $F_{MAX\_NOPIPELINEREG\_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect | 250 | 219 | 184 | 184 | 160 | MHz |

## Configuration Switching Characteristics

*Table 59:* **Configuration Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| **Power-up Timing Characteristics** | | | | | | |
| $T_{PL}$(1) | Program Latency | 5 | 5 | 5 | 5 | ms, Max |
| $T_{POR}$(1) | Power-on-Reset | 15/55 | 15/55 | 15/55 | 15/60 | ms, Min/Max |
| $T_{ICCK}$ | CCLK (output) delay | 400 | 400 | 400 | 400 | ns, Min |
| $T_{PROGRAM}$ | Program Pulse Width | 250 | 250 | 250 | 250 | ns, Min |
| **Master/Slave Serial Mode Programming Switching** | | | | | | |
| $T_{DCCK}/T_{CCKD}$ | DIN Setup/Hold, slave mode | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | 4.5/0.0 | ns, Min |
| $T_{DSCCK}/T_{SCCKD}$ | DIN Setup/Hold, master mode | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | 5.0/0.0 | ns, Min |
| $T_{CCO}$ | DOUT at 2.5V | 6 | 6 | 6 | 7 | ns, Max |
| | DOUT at 1.8V | 6 | 6 | 6 | 7 | ns, Max |
| $F_{MCCK}$ | Maximum CCLK frequency, serial modes | 105 | 105 | 105 | 70 | MHz, Max |
| $F_{MCCKTOL}$ | Frequency Tolerance, master mode with respect to nominal CCLK. | 55 | 55 | 55 | 60 | % |
| $F_{MSCCK}$ | Slave mode external CCLK | 100 | 100 | 100 | 100 | MHz |
| **SelectMAP Mode Programming Switching** | | | | | | |
| $T_{SMDCCK}/T_{SMCCKD}$ | SelectMAP Data Setup/Hold | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | 5.5/0.0 | ns, Min |
| $T_{SMCSCCK}/T_{SMCCKCS}$ | CSI_B Setup/Hold | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | 5.5/0.0 | ns, Min |
| $T_{SMCCKW}/T_{SMWCCK}$ | RDWR_B Setup/Hold | 10.0/0.0 | 10.0/0.0 | 10.0/0.0 | 16.0/0.0 | ns, Min |
| $T_{SMCKCSO}$ | CSO_B clock to out<br>(330 Ω pull-up resistor required) | 6 | 6 | 6 | 7 | ns, Max |
| $T_{SMCO}$ | CCLK to DATA out in readback at 2.5V | 6 | 6 | 6 | 7 | ns, Max |
| | CCLK to DATA out in readback at 1.8V | 6 | 6 | 6 | 7 | ns, Max |

*Table 64:* **MMCM Specification *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $RST_{MINPULSE}$ | Minimum Reset Pulse Width | 1.5 | 1.5 | 1.5 | 1.5 | ns |
| $F_{PFDMAX}$ | Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized(9) | 550 | 500 | 450 | 450 | MHz |
| | Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low | 300 | 300 | 300 | 300 | MHz |
| $F_{PFDMIN}$ | Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized | 135 | 135 | 135 | 135 | MHz |
| | Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to Low | 10 | 10 | 10 | 10 | MHz |
| $T_{FBDELAY}$ | Maximum Delay in the Feedback Path | 3 ns Max or one CLKIN cycle | | | | |
| $T_{MMCMDCK\_PSEN}$/<br>$T_{MMCMCKD\_PSEN}$ | Setup and Hold of Phase Shift Enable | 1.04<br>0.00 | 1.04<br>0.00 | 1.04<br>0.00 | 1.04<br>0.00 | ns |
| $T_{MMCMDCK\_PSINCDEC}$/<br>$T_{MMCMCKD\_PSINCDEC}$ | Setup and Hold of Phase Shift Increment/Decrement | 1.04<br>0.00 | 1.04<br>0.00 | 1.04<br>0.00 | 1.04<br>0.00 | ns |
| $T_{MMCMCKO\_PSDONE}$ | Phase Shift Clock-to-Out of PSDONE | 0.32 | 0.34 | 0.38 | 0.38 | ns |

**Notes:**

1. When DIVCLK_DIVIDE = 3 or 4, $F_{INMAX}$ is 315 MHz.
2. This duty cycle specification does not apply to the GTH_QUAD (GTH) to MMCM connection. The GTH transceivers drive the MMCMs at the following maximum frequencies: 323 MHz for -1 speed grade devices, 350 MHz for -2 speed grade devices, or 350 MHz for -3 speed grade devices.
3. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. The static offset is measured between any MMCM outputs with identical phase.
5. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
6. Includes global clock buffer.
7. Calculated as $F_{VCO}$/128 assuming output duty cycle is 50%.
8. When CASCADE4_OUT = TRUE, $F_{OUTMIN}$ is 0.036 MHz.
9. In ISE software 12.3 (or earlier versions supporting the Virtex-6 family), the phase frequency detector Optimized bandwidth setting is equivalent to the High bandwidth setting. Starting with ISE software 12.4, the Optimized bandwidth setting is automatically adjusted to Low when the software can determine that the phase frequency detector input is less than 135 MHz.

*Table 73:* **Sample Window**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1L | |
| $T_{SAMP}$ | Sampling Error at Receiver Pins(1) | All | 510 | 560 | 610 | 670 | ps |
| $T_{SAMP\_BUFIO}$ | Sampling Error at Receiver Pins using BUFIO(2) | All | 300 | 350 | 400 | 440 | ps |

**Notes:**

1. This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution
   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

*Table 74:* **Pin-to-Pin Setup/Hold and Clock-to-Out**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO** | | | | | | |
| $T_{PSCS}/T_{PHCS}$ | Setup/Hold of I/O clock | –0.28/1.09 | –0.28/1.16 | –0.28/1.33 | –0.18/1.79 | ns |
| **Pin-to-Pin Clock-to-Out Using BUFIO** | | | | | | |
| $T_{ICKOFCS}$ | Clock-to-Out of I/O clock | 4.22 | 4.59 | 5.22 | 5.63 | ns |

## Revision History

The following table shows the revision history for this document:

| Date | Version | Description of Revisions |
|---|---|---|
| 06/24/09 | 1.0 | Initial Xilinx release. |
| 07/16/09 | 1.1 | Revised the maximum $V_{CCAUX}$ and $V_{IN}$ numbers in Table 2, page 2. Removed empty column from Table 3, page 3. Revised specifications on Table 20, page 13. Updated Table 38, page 22 and added notes 1 and 2. Revised $T_{DLYCCO\_RDY}$, $T_{IDELAYCTRL\_RPW}$, and $T_{IDELAYPAT\_JIT}$ in Table 53, page 41. Updated Table 58, page 46 to more closely match the DSP48E1 speed specifications. Updated $T_{TAPTCK}/T_{TCKTAP}$ in Table 59, page 49. Updated XC6VLX130T parameters in Table 68 through Table 70, page 59. |
| 08/19/09 | 1.2 | Added values for -1L voltages and speed grade in all pertinent tables. Added $V_{FS}$ and notes to Table 1 and Table 2. Removed $DV_{PPIN}$ from the example in Figure 2. Added networking applications to Table 41, page 25. Changed and added to the block RAM $F_{MAX}$ section in Table 57, page 44 including removing Note 12. Changed $F_{PFDMAX}$ values and corrected units for $T_{STATPHAOFFSET}$ and $T_{OUTDUTY}$ in Table 64, page 52. Updated Table 71, page 60. |
| 09/16/09 | 2.0 | Added Virtex-6 HXT devices to entire document including GTH Transceiver Specifications. Updated speed specifications as described in Switching Characteristics, includes changes in Table 51, Table 57, Table 58, and Table 66 through Table 70. Comprehensive changes to Table 14, Table 15, and Table 16. Added conditions to $D_{VPPOUT}$ and revised description of $T_{OSKEW}$ in Table 17. Removed $V_{ISE}$ specification and note from Table 18. Added note 3 to Table 23. Updated note 3 in Table 24. Updated LVCMOS25 delays in Table 44. Updated specification for $T_{IOTPHZ}$ in Table 46. Removed $T_{BUFHSKEW}$ from Table 71, page 60 and added values for $T_{BUFIOSKEW}$. Added values in Table 74. |

| Date | Version | Description of Revisions |
|---|---|---|
| 01/18/10 | 2.1 | Changed absolute maximum ratings for both $V_{IN}$ and $V_{TS}$ in Table 1. Added data to Table 3. Added data to Table 5. Updated SSTL15 in Table 7. Updated $V_{OCM}$ and $V_{OD}$ values in Table 8. Added eFUSE endurance Table 12. Added values to $V_{MGTREFCLK}$ and $V_{IN}$ in Table 13, page 11. Added values and updated tables in the GTX Transceiver Specifications and GTH Transceiver Specifications sections. Added Table 27 and Figure 4. Revised parameters and values in Table 39. Updated Table 40, page 23. Added data to Table 41. Updated speed specification to v1.04 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX240T for -1 and -2 speed grades. Speed specification changes and numerous updates also made to Table 44, and Table 49 through Table 71. Added data to Table 73 and Table 74. |
| 02/09/10 | 2.2 | Revised description of $C_{IN}$ in Table 3. Clarified values in Table 5. Fixed SDR LVDS unit error in Table 41. |
| 04/12/10 | 2.3 | Added note 3 and update value of *n* in Table 3. Clarified simultaneous power-down in Power-On Power Supply Requirements. Updated external reference junction temperatures in Table 40, Analog-to-Digital Specifications. Updated speed specification to v1.05 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX130T for -1 and -2 speed grades. Fixed note 4 in Table 48. Increased the -2 specification for $F_{IDELAYCTRL\_REF}$ and clarified units for $T_{IDELAYPAT\_JIT}$ in Table 53. Added note 1 to Table 62. |
| 05/11/10 | 2.4 | Updated $F_{RXREC}$ in Table 22. Revised $F_{IDELAYCTRL\_REF}$ in Table 53. Removed $T_{RCKO\_PARITY\_ECC}$: Clock CLK to ECCPARITY in standard ECC mode row in Table 57. Added XC6VLX130T values to Table 72. |
| 05/26/10 | 2.5 | Added XC6VLX195T data to Table 5. Updated values in Table 22 including adding note 2 and note 3. Updated speed specification to v1.06 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX195T for -1 and -2 speed grades. Added XC6VLX195T values to Table 72. |
| 07/16/10 | 2.6 | Changed Table 42 and Table 43 to production status on the -3 speed grade XC6VLX130T, XC6VLX195T, and XC6VLX240T devices. Added XC6VHX250Tdata to Table 4 and Table 72. Added Note 6 to Table 64. |
| 07/23/10 | 2.7 | Changed Table 42 and Table 43 to production status on the XC6VLX75T, XC6VLX365T, XC6VLX550T, XC6VLX760, XC6VSX315T, and XC6VSX475T devices using ISE 12.2 software with speed specification v1.08. Updated $V_{CMOUTDC}$ equation to MGTAVTT – $D_{VPPOUT}/4$ in Table 17. Updated some -3, -2, -1 specifications in Table 65 through Table 72. Added and updated -1L specifications to Table 41 and for most switching characteristics tables. |
| 07/30/10 | 2.8 | Changed Table 42 and Table 43 to production status on the -1L speed grade for the XC6VLX130T, XC6VLX195T, XC6VLX240T, XC6VLX365T, and XC6VLX550T devices using ISE 12.2 software with current speed specifications. Also updated the speed specifications for XC6VLX75T, XC6VLX550T, and XC6VSX315T. Updated $V_{CCINT}$ specifications for -1L speed grade industrial temperature range devices in Table 2. |
| 09/20/10 | 2.9 | In Table 32, changed $F_{GPLLMAX}$ specification in -3 column from 5.951 to 5.591. In Table 40, changed $F_{MAX}$ for the DCLK from 250 MHz to 80 MHz. |
| 10/18/10 | 2.10 | The specification change in version 2.9, Table 40 is described in XCN10032, *Virtex-6 FPGA: GTX Transceiver User Guide, Family Data Sheet (SYSMON DCLK), and JTAG ID Changes*<br>In this version (2.10), -1L(I) data is added to Table 4 and clarified in Note 2. Changed Table 42 and Table 43 to production status on the -1L speed grade XC6VLX75T, XC6VLX760, XC6VSX315T, and XC6VSX475T devices using ISE 12.3 software with current speed specifications. Revised the XC6VLX760 -1L speed specification for $T_{PHMMCMGC}$ in Table 69 and $T_{PHMMCMCC}$ in Table 70. |
| 01/17/11 | 2.11 | Changed in Table 42 and Table 43 to production status on the XC6VHX250T devices using ISE 12.4 software with current speed specifications.<br>Added industrial temperature range ($T_j$) recommended specifications to Table 2; including specific ranges for the -2I XC6VSX475T, XC6VLX550T, XC6VLX760, and XC6VHX565Tdevices. Added note 3 to Table 36 and maximum total jitter values. Added note 4 to Table 37 and maximum sinusoidal jitter values. Added note 2 to Table 43. Revised $F_{MAX}$ descriptions in Table 57 and added note 12. Added note 8 to $F_{PFDMIN}$ in Table 64.<br>The following revisions are due to specification changes as described in XCN11009, *Virtex-6 FPGA: Data Sheet, User Guides, and JTAG ID Updates*.<br>In Table 59:*Configuration Switching Characteristics*, page 49, revised -1L specifications for $T_{POR}$, $F_{MCCK}$, $F_{MCCKTOL}$, $T_{SMCSCCK}$, $T_{SMCCKW}$, $F_{RBCCK}$, $F_{TCK}$, $F_{TCKB}$, $T_{MCCKL}$, and $T_{MCCKH}$. In Table 64: *MMCM Specification*, added bandwidth settings to $F_{PFDMIN}$ and added note 1. |