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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	128000
Total RAM Bits	9732096
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1156-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vlx130t-1ffg1156i

Important Note

Typical values for quiescent supply current are specified at nominal voltage, 85°C junction temperatures (T_j). Xilinx recommends analyzing static power consumption at $T_j = 85^\circ\text{C}$ because the majority of designs operate near the high end of the commercial temperature range. Quiescent supply current is specified by speed grade for Virtex-6 devices. Use the XPower™ Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified in Table 4.

Table 4: Typical Quiescent Supply Current

Symbol	Description	Device	Speed and Temperature Grade						Units
			-3 (C)	-2 (C, E, & I)	-1 (C & I)	-1 (I & M) ⁽²⁾	-1L (C)	-1L (I) ⁽¹⁾	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC6VLX75T	927	927	927	N/A	656	741	mA
		XC6VLX130T	1563	1563	1563	N/A	1102	1245	mA
		XC6VLX195T	2059	2059	2059	N/A	1441	1628	mA
		XC6VLX240T	2478	2478	2478	N/A	1733	1957	mA
		XC6VLX365T	3001	3001	3001	N/A	2092	2363	mA
		XC6VLX550T ⁽³⁾	N/A	4515	4515	N/A	3147	3555	mA
		XC6VLX760 ⁽³⁾	N/A	5094	5094	N/A	3471	3921	mA
		XC6VSX315T	3476	3476	3476	N/A	2409	2721	mA
		XC6VSX475T ⁽³⁾	N/A	5227	5227	N/A	3622	4091	mA
		XC6VHX250T	2906	2906	2906	N/A	N/A	N/A	mA
		XC6VHX255T	2746	2746	2746	N/A	N/A	N/A	mA
		XC6VHX380T ⁽⁴⁾	4160	4160	4160	N/A	N/A	N/A	mA
		XC6VHX565T ⁽⁵⁾	N/A	5207	5207	N/A	N/A	N/A	mA
		XQ6VLX130T	N/A	1563	N/A	1563	N/A	1245	mA
		XQ6VLX240T	N/A	2478	N/A	2478	N/A	1957	mA
		XQ6VLX550T ⁽⁷⁾	N/A	N/A	N/A	4515	N/A	3555	mA
		XQ6VSX315T	N/A	3476	N/A	3476	N/A	2721	mA
		XQ6VSX475T ⁽⁷⁾	N/A	N/A	N/A	5227	N/A	4091	mA

GTH Transceiver DC Input and Output Levels

Table 30 summarizes the DC output specifications of the GTH transceivers in Virtex-6 FPGAs. Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further details.

Table 30: GTH Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
D_{VPPIN}	Differential peak-to-peak input voltage	External AC coupled	175	–	1200	mV
D_{VPPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	800	–	1200	mV
R_{IN}	Differential input resistance		80	100	120	Ω
R_{OUT}	Differential output resistance		80	100	120	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	–	ps
C_{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 31 summarizes the DC specifications of the clock input of the GTH transceiver. Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further details.

Table 31: GTH Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	≤ 600 MHz	500	–	1600	mV
		> 600 MHz	600	–	1600	mV
R_{IN}	Differential input resistance		80	100	120	Ω
C_{EXT}	Required external AC coupling capacitor		–	100	–	nF

GTH Transceiver Switching Characteristics

Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further information.

Table 32: GTH Transceiver Maximum Data Rate and PLL Frequency Range

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F_{GTHMAX}	Maximum GTH transceiver data rate	PLL Output Divider = 1	11.182	11.182	10.32	Gb/s
		PLL Output Divider = 4	2.795	2.795	2.58	Gb/s
F_{GTHMIN}	Minimum GTH transceiver data rate ⁽¹⁾	PLL Output Divider = 1	9.92	9.92	9.92	Gb/s
		PLL Output Divider = 4	2.48	2.48	2.48	Gb/s
$F_{GPLLMAX}$	Maximum GTH PLL frequency		5.591	5.591	5.16	GHz
$F_{GPLLMIN}$	Minimum GTH PLL frequency		4.96	4.96	4.96	GHz

Notes:

- Lower data rates can be achieved using FPGA logic based oversampling designs.

Table 33: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{GTHDRPCLK}$	GTHDRPCLK maximum frequency	70	70	60	MHz

Table 34: GTH Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range	-1 speed grade	150	—	645	MHz
		-2 and -3 speed grades	150	—	700	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	—	200	—	ps
T_{FCLK}	Reference clock fall time	80% – 20%	—	200	—	ps
T_{DCREF}	Reference clock duty cycle	CLK	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	—	—	2	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	—	—	20	μs

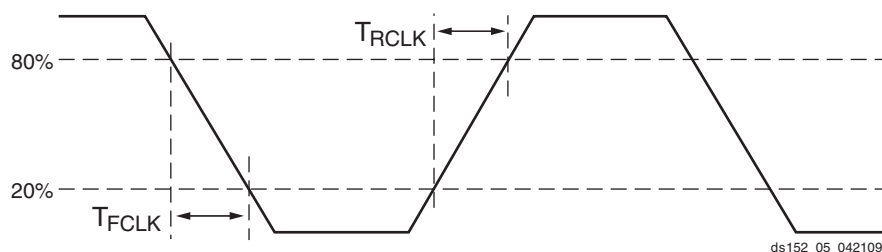


Figure 5: Reference Clock Timing Parameters

Table 37: GTH Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
R _{XRL}	Run length (CID)		8000	–	–	UI
R _{XPPMTOL}	Data/REFCLK PPM offset tolerance		–200	–	200	ppm
SJ Jitter Tolerance ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾						
JT_SJ _{11.18}	Sinusoidal Jitter	11.18 Gb/s	0.3	–	–	UI
JT_SJ _{10.32}	Sinusoidal Jitter	10.32 Gb/s	0.3	–	–	UI
JT_SJ _{9.95}	Sinusoidal Jitter	9.95 Gb/s	0.3	–	–	UI
JT_SJ _{2.667}	Sinusoidal Jitter	2.667 Gb/s	0.5	–	–	UI
JT_SJ _{2.48}	Sinusoidal Jitter	2.48 Gb/s	0.5	–	–	UI

Notes:

- These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit error ratio of 1e⁻¹².
- The frequency of the injected sinusoidal jitter is 80 MHz.
- High-frequency jitter tolerance including 6 db of channel loss at a high frequency of the data rate divided by two.

Ethernet MAC Switching Characteristics

Consult [UG368: Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide](#) for further information.

Table 38: Maximum Ethernet MAC Performance

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1	-1L	
F _{TEMACCLIENT}	Client interface maximum frequency	10 Mb/s – 8-bit width	2.5 ⁽¹⁾	2.5 ⁽¹⁾	2.5 ⁽¹⁾	2.5 ⁽¹⁾	MHz
		100 Mb/s – 8-bit width	25 ⁽²⁾	25 ⁽²⁾	25 ⁽²⁾	25 ⁽²⁾	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		1000 Mb/s – 16-bit width	62.5	62.5	62.5	62.5	MHz
		2000 Mb/s – 16-bit width	125	125	125	N/A	MHz
		2500 Mb/s – 16-bit width	156.25	156.25	156.25	N/A	MHz
F _{TEMACPHY}	Physical interface maximum frequency	10 Mb/s – 4-bit width	2.5	2.5	2.5	2.5	MHz
		100 Mb/s – 4-bit width	25	25	25	25	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		2000 Mb/s – 8-bit width	250	250	250	N/A	MHz
		2500 Mb/s – 8-bit width	312.5	312.5	312.5	N/A	MHz

Notes:

- When not using clock enable, the F_{MAX} is lowered to 1.25 MHz.
- When not using clock enable, the F_{MAX} is lowered to 12.5 MHz.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 39: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F _{PIPECLK}	Pipe clock maximum frequency	250	250	250	250	MHz
F _{USERCLK}	User clock maximum frequency	500	500	250	250	MHz
F _{DRPCLK}	DRP clock maximum frequency	250	250	250	250	MHz

System Monitor Analog-to-Digital Converter Specification

Table 40: Analog-to-Digital Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
AV _{DD} = 2.5V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 5.2 MHz, T _j = -55°C to 125°C M-Grade, Typical values at T _j = +35°C						
DC Accuracy: All external input channels. Both unipolar and bipolar modes.						
Resolution			10	—	—	Bits
Integral Nonlinearity	INL		—	—	±1	LSBs
Differential Nonlinearity	DNL	No missing codes (T _{MIN} to T _{MAX}) Guaranteed Monotonic	—	—	±0.9	LSBs
Unipolar Offset Error ⁽¹⁾		Uncalibrated	—	±2	±30	LSBs
Bipolar Offset Error ⁽¹⁾		Uncalibrated measured in bipolar mode	—	±2	±30	LSBs
Gain Error		Uncalibrated - External Reference	—	±0.2	±2	%
		Uncalibrated - Internal Reference	—	±2	—	%
Bipolar Gain Error ⁽¹⁾		Uncalibrated - External Reference	—	±0.2	±2	%
		Uncalibrated - Internal Reference	—	±2	—	%
Total Unadjusted Error (Uncalibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	—	±10	—	LSBs
		Deviation from ideal transfer function. Internal reference	—	±20	—	LSBs
Total Unadjusted Error (Calibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	—	±1	±2	LSBs
Calibrated Gain Temperature Coefficient		Variation of FS code with temperature	—	±0.01	—	LSB/°C
DC Common-Mode Reject	CMRR _{DC}	V _N = V _{CM} = 0.5V ± 0.5V, V _P - V _N = 100mV	—	70	—	dB
Conversion Rate ⁽²⁾						
Conversion Time - Continuous	t _{CONV}	Number of CLK cycles	26	—	32	
Conversion Time - Event	t _{CONV}	Number of CLK cycles	—	—	21	
T/H Acquisition Time	t _{ACQ}	Number of CLK cycles	4	—	—	
DRP Clock Frequency	DCLK	DRP clock frequency	8	—	80	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	—	5.2	MHz
CLK Duty cycle			40	—	60	%

IOB Pad Input/Output/3-State Switching Characteristics

Table 44 (for commercial (XC) Virtex-6 devices) and **Table 45** (for the Defense-grade (XQ) Virtex-6 devices) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 46 summarizes the value of T_{IOTPHZ} . T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDS_25	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
LVDSEXT_25	0.85	0.94	1.09	1.08	1.53	1.65	1.84	1.73	1.53	1.65	1.84	1.73	ns
HT_25	0.85	0.94	1.09	1.08	1.51	1.62	1.78	1.69	1.51	1.62	1.78	1.69	ns
BLVDS_25	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.65	1.39	1.50	1.67	1.65	ns
RSDS_25 (point to point)	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
HSTL_I	0.81	0.91	1.06	1.06	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns
HSTL_II	0.81	0.91	1.06	1.06	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
HSTL_III	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
HSTL_I_18	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
HSTL_II_18	0.81	0.91	1.06	1.06	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
HSTL_III_18	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
SSTL2_I	0.81	0.91	1.06	1.06	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
SSTL2_II	0.81	0.91	1.06	1.06	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
LVC MOS25, Slow, 2 mA	0.51	0.57	0.66	0.70	5.09	5.46	6.01	5.63	5.09	5.46	6.01	5.63	ns
LVC MOS25, Slow, 4 mA	0.51	0.57	0.66	0.70	3.30	3.49	3.79	3.65	3.30	3.49	3.79	3.65	ns
LVC MOS25, Slow, 6 mA	0.51	0.57	0.66	0.70	2.62	2.81	3.08	2.95	2.62	2.81	3.08	2.95	ns
LVC MOS25, Slow, 8 mA	0.51	0.57	0.66	0.70	2.21	2.41	2.72	2.59	2.21	2.41	2.72	2.59	ns
LVC MOS25, Slow, 12 mA	0.51	0.57	0.66	0.70	1.80	1.95	2.17	2.10	1.80	1.95	2.17	2.10	ns
LVC MOS25, Slow, 16 mA	0.51	0.57	0.66	0.70	1.89	2.05	2.29	2.21	1.89	2.05	2.29	2.21	ns
LVC MOS25, Slow, 24 mA	0.51	0.57	0.66	0.70	1.68	1.82	2.02	1.98	1.68	1.82	2.02	1.98	ns
LVC MOS25, Fast, 2 mA	0.51	0.57	0.66	0.70	5.12	5.49	6.04	5.62	5.12	5.49	6.04	5.62	ns
LVC MOS25, Fast, 4 mA	0.51	0.57	0.66	0.70	3.28	3.50	3.82	3.65	3.28	3.50	3.82	3.65	ns
LVC MOS25, Fast, 6 mA	0.51	0.57	0.66	0.70	2.56	2.73	2.99	2.88	2.56	2.73	2.99	2.88	ns
LVC MOS25, Fast, 8 mA	0.51	0.57	0.66	0.70	2.11	2.33	2.65	2.53	2.11	2.33	2.65	2.53	ns
LVC MOS25, Fast, 12 mA	0.51	0.57	0.66	0.70	1.74	1.88	2.08	2.03	1.74	1.88	2.08	2.03	ns
LVC MOS25, Fast, 16 mA	0.51	0.57	0.66	0.70	1.77	1.92	2.13	2.08	1.77	1.92	2.13	2.08	ns

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVC MOS25, Fast, 24 mA	0.51	0.57	0.66	0.70	1.66	1.79	1.99	1.96	1.66	1.79	1.99	1.96	ns
LVC MOS18, Slow, 2 mA	0.55	0.61	0.71	0.73	4.21	4.47	4.87	4.30	4.21	4.47	4.87	4.30	ns
LVC MOS18, Slow, 4 mA	0.55	0.61	0.71	0.73	2.79	2.96	3.21	2.94	2.79	2.96	3.21	2.94	ns
LVC MOS18, Slow, 6 mA	0.55	0.61	0.71	0.73	2.30	2.43	2.64	2.47	2.30	2.43	2.64	2.47	ns
LVC MOS18, Slow, 8 mA	0.55	0.61	0.71	0.73	2.01	2.11	2.27	2.24	2.01	2.11	2.27	2.24	ns
LVC MOS18, Slow, 12 mA	0.55	0.61	0.71	0.73	1.88	1.99	2.15	2.10	1.88	1.99	2.15	2.10	ns
LVC MOS18, Slow, 16 mA	0.55	0.61	0.71	0.73	1.84	1.95	2.11	2.04	1.84	1.95	2.11	2.04	ns
LVC MOS18, Fast, 2 mA	0.55	0.61	0.71	0.73	4.00	4.23	4.57	4.08	4.00	4.23	4.57	4.08	ns
LVC MOS18, Fast, 4 mA	0.55	0.61	0.71	0.73	2.62	2.76	2.97	2.74	2.62	2.76	2.97	2.74	ns
LVC MOS18, Fast, 6 mA	0.55	0.61	0.71	0.73	2.15	2.28	2.46	2.32	2.15	2.28	2.46	2.32	ns
LVC MOS18, Fast, 8 mA	0.55	0.61	0.71	0.73	1.90	1.99	2.13	2.14	1.90	1.99	2.13	2.14	ns
LVC MOS18, Fast, 12 mA	0.55	0.61	0.71	0.73	1.69	1.80	1.97	1.88	1.69	1.80	1.97	1.88	ns
LVC MOS18, Fast, 16 mA	0.55	0.61	0.71	0.73	1.63	1.74	1.91	1.88	1.63	1.74	1.91	1.88	ns
LVC MOS15, Slow, 2 mA	0.64	0.73	0.85	0.85	3.43	3.77	4.29	3.91	3.43	3.77	4.29	3.91	ns
LVC MOS15, Slow, 4 mA	0.64	0.73	0.85	0.85	2.58	2.79	3.10	2.93	2.58	2.79	3.10	2.93	ns
LVC MOS15, Slow, 6 mA	0.64	0.73	0.85	0.85	2.08	2.32	2.68	2.50	2.08	2.32	2.68	2.50	ns
LVC MOS15, Slow, 8 mA	0.64	0.73	0.85	0.85	1.81	1.98	2.23	2.24	1.81	1.98	2.23	2.24	ns
LVC MOS15, Slow, 12 mA	0.64	0.73	0.85	0.85	1.76	1.91	2.13	2.07	1.76	1.91	2.13	2.07	ns
LVC MOS15, Slow, 16 mA	0.64	0.73	0.85	0.85	1.69	1.83	2.04	1.98	1.69	1.83	2.04	1.98	ns
LVC MOS15, Fast, 2 mA	0.64	0.73	0.85	0.85	3.44	3.77	4.28	3.91	3.44	3.77	4.28	3.91	ns
LVC MOS15, Fast, 4 mA	0.64	0.73	0.85	0.85	2.37	2.53	2.78	2.66	2.37	2.53	2.78	2.66	ns
LVC MOS15, Fast, 6 mA	0.64	0.73	0.85	0.85	1.80	2.05	2.42	2.16	1.80	2.05	2.42	2.16	ns
LVC MOS15, Fast, 8 mA	0.64	0.73	0.85	0.85	1.76	1.90	2.11	2.04	1.76	1.90	2.11	2.04	ns
LVC MOS15, Fast, 12 mA	0.64	0.73	0.85	0.85	1.64	1.77	1.97	1.90	1.64	1.77	1.97	1.90	ns
LVC MOS15, Fast, 16 mA	0.64	0.73	0.85	0.85	1.62	1.76	1.96	1.92	1.62	1.76	1.96	1.92	ns
LVC MOS12, Slow, 2 mA	0.72	0.81	0.93	0.95	3.14	3.39	3.75	3.54	3.14	3.39	3.75	3.54	ns
LVC MOS12, Slow, 4 mA	0.72	0.81	0.93	0.95	2.43	2.63	2.93	2.79	2.43	2.63	2.93	2.79	ns
LVC MOS12, Slow, 6 mA	0.72	0.81	0.93	0.95	1.92	2.11	2.41	2.26	1.92	2.11	2.41	2.26	ns
LVC MOS12, Slow, 8 mA	0.72	0.81	0.93	0.95	1.87	2.02	2.25	2.17	1.87	2.02	2.25	2.17	ns
LVC MOS12, Fast, 2 mA	0.72	0.81	0.93	0.95	2.71	2.98	3.39	3.11	2.71	2.98	3.39	3.11	ns
LVC MOS12, Fast, 4 mA	0.72	0.81	0.93	0.95	1.93	2.16	2.51	2.31	1.93	2.16	2.51	2.31	ns
LVC MOS12, Fast, 6 mA	0.72	0.81	0.93	0.95	1.75	1.89	2.11	2.05	1.75	1.89	2.11	2.05	ns
LVC MOS12, Fast, 8 mA	0.72	0.81	0.93	0.95	1.69	1.82	2.02	1.98	1.69	1.82	2.02	1.98	ns
LVDCI_25	0.51	0.57	0.66	0.70	2.05	2.14	2.26	2.26	2.05	2.14	2.26	2.26	ns
LVDCI_18	0.55	0.61	0.71	0.73	2.07	2.23	2.47	2.38	2.07	2.23	2.47	2.38	ns
LVDCI_15	0.64	0.73	0.85	0.85	1.85	2.01	2.24	2.18	1.85	2.01	2.24	2.18	ns

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
DIFF_SSTL18_I	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
DIFF_SSTL18_I_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL18_II	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
DIFF_SSTL18_II_DCI	0.85	0.94	1.09	1.08	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
DIFF_SSTL18_II_T_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
DIFF_SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVDS_25	0.94	1.09	1.08	1.54	2.16	1.62	1.54	2.16	1.62	ns
LVDSEXT_25	0.94	1.09	1.08	1.65	2.20	1.73	1.65	2.20	1.73	ns
HT_25	0.94	1.09	1.08	1.62	2.20	1.69	1.62	2.20	1.69	ns
BLVDS_25	0.94	1.09	1.08	1.50	3.18	1.65	1.50	3.18	1.65	ns
RSDS_25 (point to point)	0.94	1.09	1.08	1.54	2.22	1.62	1.54	2.22	1.62	ns
HSTL_I	0.91	1.06	1.06	1.56	2.44	1.71	1.56	2.44	1.71	ns
HSTL_II	0.91	1.06	1.06	1.56	2.21	1.72	1.56	2.21	1.72	ns
HSTL_III	0.91	1.06	1.06	1.54	2.50	1.69	1.54	2.50	1.69	ns
HSTL_I_18	0.91	1.06	1.06	1.58	2.43	1.72	1.58	2.43	1.72	ns
HSTL_II_18	0.91	1.06	1.06	1.62	2.30	1.78	1.62	2.30	1.78	ns
HSTL_III_18	0.91	1.06	1.06	1.54	2.49	1.69	1.54	2.49	1.69	ns
SSTL2_I	0.91	1.06	1.06	1.60	2.50	1.74	1.60	2.50	1.74	ns
SSTL2_II	0.91	1.06	1.06	1.54	2.49	1.71	1.54	2.49	1.71	ns
SSTL15	0.91	1.06	1.06	1.54	2.07	1.69	1.54	2.07	1.69	ns
LVC MOS25, Slow, 2 mA	0.57	0.66	0.70	5.46	6.01	5.63	5.46	6.01	5.63	ns
LVC MOS25, Slow, 4 mA	0.57	0.66	0.70	3.49	3.79	3.65	3.49	3.79	3.65	ns
LVC MOS25, Slow, 6 mA	0.57	0.66	0.70	2.81	3.08	2.95	2.81	3.08	2.95	ns
LVC MOS25, Slow, 8 mA	0.57	0.66	0.70	2.41	2.72	2.59	2.41	2.72	2.59	ns
LVC MOS25, Slow, 12 mA	0.57	0.66	0.70	1.95	2.23	2.10	1.95	2.23	2.10	ns
LVC MOS25, Slow, 16 mA	0.57	0.66	0.70	2.05	2.29	2.21	2.05	2.29	2.21	ns
LVC MOS25, Slow, 24 mA	0.57	0.66	0.70	1.82	2.24	1.98	1.82	2.24	1.98	ns
LVC MOS25, Fast, 2 mA	0.57	0.66	0.70	5.49	6.04	5.62	5.49	6.04	5.62	ns
LVC MOS25, Fast, 4 mA	0.57	0.66	0.70	3.50	3.82	3.65	3.50	3.82	3.65	ns
LVC MOS25, Fast, 6 mA	0.57	0.66	0.70	2.73	2.99	2.88	2.73	2.99	2.88	ns
LVC MOS25, Fast, 8 mA	0.57	0.66	0.70	2.33	2.65	2.53	2.33	2.65	2.53	ns
LVC MOS25, Fast, 12 mA	0.57	0.66	0.70	1.88	2.08	2.03	1.88	2.08	2.03	ns

Table 50: OLOGIC Switching Characteristics

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup/Hold							
T _{ODCK} /T _{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.45/ −0.08	0.50/ −0.08	0.54/ −0.08	0.54/ −0.08	0.69/ −0.11	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.17/ −0.03	0.20/ −0.03	0.22/ −0.03	0.27/ −0.05	0.27/ −0.04	ns
T _{OSRCK} /T _{OCKSR}	SR pin Setup/Hold with respect to CLK	0.59/ −0.24	0.62/ −0.24	0.54/ −0.08	0.54/ −0.08	0.79/ −0.35	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.44/ −0.07	0.51/ −0.07	0.56/ −0.07	0.60/ −0.10	0.68/ −0.13	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.15/ −0.04	0.19/ −0.04	0.21/ −0.04	0.27/ −0.05	0.29/ −0.05	ns
Combinatorial							
T _{DOQ}	D1 to OQ out or T1 to TQ out	0.78	0.87	1.01	1.01	1.15	ns
Sequential Delays							
T _{OCKQ}	CLK to OQ/TQ out	0.54	0.61	0.71	0.71	0.80	ns
T _{RQ}	SR pin to OQ/TQ out	0.80	0.90	1.05	1.05	1.19	ns
T _{GSRQ}	Global Set/Reset to Q outputs	7.60	7.60	10.51	10.51	10.51	ns
Set/Reset							
T _{RPW}	Minimum Pulse Width, SR inputs	0.78	0.95	1.20	1.20	1.30	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 51: ISERDES Switching Characteristics

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup/Hold for Control Lines							
T _{ISCKK_BITSIP} / T _{ISCKC_BITSIP}	BITSLIP pin Setup/Hold with respect to CLKDIV	0.07/ 0.15	0.08/ 0.16	0.09/ 0.17	0.09/ 0.17	0.14/ 0.17	ns
T _{ISCKK_CE} / T _{ISCKC_CE} ⁽²⁾	CE pin Setup/Hold with respect to CLK (for CE1)	0.20/ 0.03	0.25/ 0.04	0.27/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T _{ISCKK_CE2} / T _{ISCKC_CE2} ⁽²⁾	CE pin Setup/Hold with respect to CLKDIV (for CE2)	0.01/ 0.27	0.01 0.29	0.01/ 0.31	0.01/ 0.31	−0.05/ 0.35	ns
Setup/Hold for Data Lines							
T _{ISDCK_D} / T _{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.07/ 0.08	0.08/ 0.09	0.09/ 0.11	0.09/ 0.11	0.11/ 0.19	ns
T _{ISDCK_DDLY} / T _{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY) ⁽¹⁾	0.10/ 0.05	0.12/ 0.06	0.14/ 0.07	0.14/ 0.07	0.16/ 0.15	ns
T _{ISDCK_D_DDR} / T _{ISCKD_D_DDR}	D pin Setup/Hold with respect to CLK at DDR mode	0.07/ 0.08	0.08/ 0.09	0.09/ 0.11	0.09/ 0.11	0.11/ 0.19	ns
T _{ISDCK_DDLY_DDR} / T _{ISCKD_DDLY_DDR}	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY) ⁽¹⁾	0.10/ 0.05	0.12/ 0.06	0.14/ 0.07	0.14/ 0.07	0.16/ 0.15	ns
Sequential Delays							
T _{ISCKO_Q}	CLKDIV to out at Q pin	0.57	0.66	0.75	0.80	0.88	ns
Propagation Delays							
T _{ISDO_DO}	D input to DO output pin	0.19	0.22	0.25	0.25	0.28	ns

Notes:

- Recorded at 0 tap value.
- T_{ISCK_CE2} and T_{ISCK_CE2} are reported as $T_{ISCK_CE} / T_{ISCK_CE}$ in TRACE report.

Input/Output Delay Switching Characteristics

Table 53: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
IDELAYCTRL						
T _{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3.00	3.00	3.00	3.25	μs
F _{IDELAYCTRL_REF}	REFCLK frequency = 200.0 ⁽¹⁾	200	200	200	200	MHz
	REFCLK frequency = 300.0 ⁽¹⁾	300	300	–	–	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
T _{IDELAYCTRL_RPW}	Minimum Reset pulse width	50.00	50.00	50.00	52.50	ns
IODELAY						
T _{IDELAYRESOLUTION}	IODELAY Chain Delay Resolution	1/(32 x 2 x F _{REF})				ps
T _{IDELAYPAT_JIT}	Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾	0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). ⁽³⁾	±5	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). ⁽⁴⁾	±9	±9	±9	±9	ps per tap
T _{IODELAY_CLK_MAX}	Maximum frequency of CLK input to IDELAY	500.00	420.00	300.00	300.00	MHz
T _{IODCCK_CE} / T _{IODCKC_CE}	CE pin Setup/Hold with respect to CK	0.45/ –0.09	0.53/ –0.09	0.65/ –0.09	0.84/ –0.14	ns
T _{IODCK_INC} / T _{IODCKC_INC}	INC pin Setup/Hold with respect to CK	0.23/ –0.02	0.27/ –0.01	0.31/ 0.00	0.27/ –0.04	ns
T _{IODCCK_RST} / T _{IODCKC_RST}	RST pin Setup/Hold with respect to CK	0.57/ –0.08	0.62/ –0.08	0.69/ –0.08	0.74/ –0.13	ns
T _{IODDO_T}	TSCONTROL delay to MUXE/MUXF switching and through IDELAY	Note 5	Note 5	Note 5	Note 5	ps
T _{IODDO_IDATAIN}	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	ps
T _{IODDO_ODATAIN}	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See TRACE report for actual values.

CLB Switching Characteristics

Table 54: CLB Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Combinatorial Delays						
T _{ILO}	An – Dn LUT address to A	0.06	0.07	0.07	0.09	ns, Max
	An – Dn LUT address to AMUX/CMUX	0.18	0.20	0.22	0.25	ns, Max
	An – Dn LUT address to BMUX_A	0.28	0.31	0.36	0.40	ns, Max

Table 54: CLB Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T _{ITO}	An – Dn inputs to A – D Q outputs	0.59	0.67	0.79	0.85	ns, Max
T _{AXA}	AX inputs to AMUX output	0.31	0.35	0.42	0.44	ns, Max
T _{AXB}	AX inputs to BMUX output	0.35	0.39	0.47	0.50	ns, Max
T _{AXC}	AX inputs to CMUX output	0.39	0.44	0.52	0.56	ns, Max
T _{AXD}	AX inputs to DMUX output	0.42	0.47	0.55	0.60	ns, Max
T _{BXB}	BX inputs to BMUX output	0.30	0.34	0.39	0.44	ns, Max
T _{BXD}	BX inputs to DMUX output	0.38	0.43	0.50	0.55	ns, Max
T _{CXC}	CX inputs to CMUX output	0.26	0.29	0.34	0.37	ns, Max
T _{CXD}	CX inputs to DMUX output	0.30	0.34	0.40	0.44	ns, Max
T _{DXD}	DX inputs to DMUX output	0.30	0.33	0.38	0.43	ns, Max
T _{OPCYA}	An input to COUT output	0.32	0.36	0.41	0.47	ns, Max
T _{OPCYB}	Bn input to COUT output	0.32	0.36	0.41	0.47	ns, Max
T _{OPCYC}	Cn input to COUT output	0.27	0.30	0.34	0.40	ns, Max
T _{OPCYD}	Dn input to COUT output	0.25	0.28	0.32	0.37	ns, Max
T _{AXCY}	AX input to COUT output	0.25	0.28	0.33	0.36	ns, Max
T _{BXCY}	BX input to COUT output	0.22	0.24	0.28	0.31	ns, Max
T _{CXCY}	CX input to COUT output	0.15	0.17	0.20	0.22	ns, Max
T _{DXCY}	DX input to COUT output	0.14	0.16	0.19	0.21	ns, Max
T _{BYP}	CIN input to COUT output	0.06	0.07	0.08	0.09	ns, Max
T _{CINA}	CIN input to AMUX output	0.21	0.24	0.28	0.30	ns, Max
T _{CINB}	CIN input to BMUX output	0.23	0.25	0.29	0.31	ns, Max
T _{CINC}	CIN input to CMUX output	0.23	0.26	0.30	0.33	ns, Max
T _{CIND}	CIN input to DMUX output	0.25	0.29	0.33	0.36	ns, Max
Sequential Delays						
T _{CKO}	Clock to AQ – DQ outputs	0.29	0.33	0.39	0.44	ns, Max
T _{SHCKO}	Clock to AMUX – DMUX outputs	0.36	0.40	0.47	0.53	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T _{DICK} /T _{CKDI}	A – D input to CLK on A – D Flip Flops	0.30/0.17	0.36/0.18	0.43/0.20	0.44/0.25	ns, Min
T _{CECK_CLB} / T _{CKCE_CLB}	CE input to CLK on A – D Flip Flops	0.20/0.00	0.25/0.00	0.32/0.00	0.32/0.01	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D Flip Flops	0.39/–0.07	0.44/–0.07	0.52/–0.07	0.58/–0.08	ns, Min
T _{CINCK} /T _{CKCIN}	CIN input to CLK on A – D Flip Flops	0.16/0.12	0.19/0.14	0.24/0.16	0.23/0.22	ns, Min
Set/Reset						
T _{SRMIN}	SR input minimum pulse width	0.90	0.90	0.97	0.80	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops	0.52	0.58	0.68	0.77	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops	0.41	0.48	0.59	0.61	ns, Max
F _{TOG}	Toggle frequency (for export control)	1412.00	1286.40	1098.00	1098.00	MHz

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

Block RAM and FIFO Switching Characteristics

Table 57: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Block RAM and FIFO Clock-to-Out Delays						
T _{RCKO_DO} and T _{RCKO_DO_REG} ⁽¹⁾	Clock CLK to DOUT output (without output register) ⁽²⁾⁽³⁾	1.60	1.79	2.08	2.36	ns, Max
	Clock CLK to DOUT output (with output register) ⁽⁴⁾⁽⁵⁾	0.60	0.66	0.75	0.83	ns, Max
T _{RCKO_DO_ECC} and T _{RCKO_DO_ECC_REG}	Clock CLK to DOUT output with ECC (without output register) ⁽²⁾⁽³⁾	2.62	2.89	3.30	3.73	ns, Max
	Clock CLK to DOUT output with ECC (with output register) ⁽⁴⁾⁽⁵⁾	0.71	0.77	0.86	0.94	ns, Max
T _{RCKO_CASC} and T _{RCKO_CASC_REG}	Clock CLK to DOUT output with Cascade (without output register) ⁽²⁾	2.49	2.77	3.18	3.61	ns, Max
	Clock CLK to DOUT output with Cascade (with output register) ⁽⁴⁾	1.29	1.41	1.58	1.79	ns, Max
T _{RCKO_FLAGS}	Clock CLK to FIFO flags outputs ⁽⁶⁾	0.74	0.81	0.91	0.98	ns, Max
T _{RCKO_POINTERS}	Clock CLK to FIFO pointers outputs ⁽⁷⁾	0.90	0.98	1.09	1.21	ns, Max
T _{RCKO_SDBIT_ECC} and T _{RCKO_SDBIT_ECC_REG}	Clock CLK to BITERR (with output register)	0.62	0.68	0.76	0.82	ns, Max
	Clock CLK to BITERR (without output register)	2.21	2.46	2.84	3.23	ns, Max
T _{RCKO_PARITY_ECC}	Clock CLK to ECCPARITY in ECC encode only mode	0.86	0.94	1.06	1.18	ns, Max
T _{RCKO_RDADDR_ECC} and T _{RCKO_RDADDR_ECC_REG}	Clock CLK to RDADDR output with ECC (without output register)	0.73	0.79	0.90	1.00	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.76	0.82	0.92	1.02	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{RCKC_ADDR} /T _{RCKC_ADDR}	ADDR inputs ⁽⁸⁾	0.47/ 0.27	0.53/ 0.29	0.62/ 0.32	0.66/ 0.34	ns, Min
T _{RDCK_DI} /T _{RCKD_DI}	DIN inputs ⁽⁹⁾	0.84/ 0.30	0.95/ 0.32	1.11/ 0.34	1.26/ 0.36	ns, Min
T _{RDCK_DI_ECC} /T _{RCKD_DI_ECC}	DIN inputs with block RAM ECC in standard mode ⁽⁹⁾	0.47/ 0.30	0.52/ 0.32	0.59/ 0.34	0.68/ 0.36	ns, Min
	DIN inputs with block RAM ECC encode only ⁽⁹⁾	0.68/ 0.30	0.75/ 0.32	0.85/ 0.34	0.97/ 0.36	ns, Min
	DIN inputs with FIFO ECC in standard mode ⁽⁹⁾	0.77/ 0.30	0.87/ 0.32	1.02/ 0.34	1.16/ 0.36	ns, Min
T _{RCKC_CLK} /T _{RCKC_CLK}	Inject single/double bit error in ECC mode	0.90/ 0.27	1.02/ 0.28	1.20/ 0.29	1.56/ 0.29	ns, Min
T _{RCKC_RDEN} /T _{RCKC_RDEN}	Block RAM Enable (EN) input	0.31/ 0.26	0.35/ 0.27	0.41/ 0.30	0.44/ 0.31	ns, Min
T _{RCKC_REGCE} /T _{RCKC_REGCE}	CE input of output register	0.18/ 0.25	0.19/ 0.27	0.22/ 0.31	0.24/ 0.33	ns, Min
T _{RCKC_RSTREG} /T _{RCKC_RSTREG}	Synchronous RSTREG input	0.22/ 0.23	0.24/ 0.24	0.28/ 0.26	0.31/ 0.27	ns, Min
T _{RCKC_RSTRAM} /T _{RCKC_RSTRAM}	Synchronous RSTRAM input	0.32/ 0.23	0.36/ 0.24	0.41/ 0.27	0.46/ 0.29	ns, Min

Table 57: Block RAM and FIFO Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{RCKK_WE}/T_{RCKC_WE}	Write Enable (WE) input (Block RAM only)	0.44/ 0.19	0.47/ 0.25	0.52/ 0.35	0.67/ 0.24	ns, Min
$T_{RCKK_WREN}/T_{RCKC_WREN}$	WREN FIFO inputs	0.47/ 0.26	0.50/ 0.27	0.55/ 0.30	0.68/ 0.31	ns, Min
$T_{RCKK_RDEN}/T_{RCKC_RDEN}$	RDEN FIFO inputs	0.46/ 0.26	0.50/ 0.27	0.55/ 0.30	0.67/ 0.31	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers ⁽¹⁰⁾	0.90	0.98	1.10	1.23	ns, Max
$T_{RCKK_RSTREG}/T_{RCKC_RSTREG}$	FIFO reset timing ⁽¹¹⁾	0.22/ 0.23	0.24/ 0.24	0.28/ 0.26	0.31/ 0.27	ns, Min
Maximum Frequency						
F_{MAX}	Block RAM in TDP and SDP modes (Write First and No Change modes)	600	540	450	340	MHz
	Block RAM (Read First mode)	525	475	400	275	MHz
	Block RAM (SDP mode) ⁽¹²⁾	525	475	400	275	MHz
$F_{MAX_CASCADE}$	Block RAM Cascade (Write First and No Change modes)	550	490	400	300	MHz
	Block RAM Cascade (Read First mode)	475	425	350	235	MHz
F_{MAX_FIFO}	FIFO in all modes	600	540	450	340	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	450	400	325	250	MHz

Notes:

1. TRACE will report all of these parameters as T_{RCKO_DO} .
2. T_{RCKO_DOR} includes T_{RCKO_DOW} , T_{RCKO_DOPR} , and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with $DO_REG = 0$.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with $DO_REG = 1$.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY} , T_{RCKO_AFULL} , T_{RCKO_EMPTY} , T_{RCKO_FULL} , T_{RCKO_RDERR} , T_{RCKO_WRERR} .
7. $T_{RCKO_POINTERS}$ includes both $T_{RCKO_RDCOUNT}$ and $T_{RCKO_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. The FIFO reset must be asserted for at least three positive clock edges.
12. When using ISE software v12.4 or later, if the RDADDR_COLLISION_HWCONFIG attribute is set to PERFORMANCE or the block RAM is in single-port operation, then the faster F_{MAX} for WRITE_FIRST/NO_CHANGE modes apply.

DSP48E1 Switching Characteristics

Table 58: DSP48E1 Switching Characteristics

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock							
$T_{\text{DSPDCK}_{\{A, \text{ACIN}; B, \text{BCIN}\}}_{\{\text{AREG}; \text{BREG}\}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}; B, \text{BCIN}\}}_{\{\text{AREG}; \text{BREG}\}}}$	{A, ACIN, B, BCIN} input to {A, B} register CLK	0.25/ 0.27	0.29/ 0.30	0.35/ 0.34	0.36/ 0.34	0.46/ 0.39	ns
$T_{\text{DSPDCK}_{\text{C_CREG}}/T_{\text{DSPCKD}_{\text{C_CREG}}}}$	C input to C register CLK	0.16/ 0.20	0.19/ 0.22	0.22/ 0.24	0.25/ 0.24	0.33/ 0.30	ns
$T_{\text{DSPDCK}_{\text{D_DREG}}/T_{\text{DSPCKD}_{\text{D_DREG}}}}$	D input to D register CLK	0.07/ 0.31	0.10/ 0.34	0.15/ 0.39	0.16/ 0.39	0.24/ 0.45	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock							
$T_{\text{DSPDCK}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{MREG_MULT}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{MREG_MULT}}}$	{A, ACIN, B, BCIN} input to M register CLK	2.36/ 0.04	2.70/ 0.04	3.21/ 0.04	3.21/ 0.04	3.66/ 0.02	ns
$T_{\text{DSPDCK}_{\{A, D\}}_{\text{ADREG}}/T_{\text{DSPCKD}_{\{A, D\}}_{\text{ADREG}}}$	{A, D} input to AD register CLK	1.24/ 0.10	1.42/ 0.12	1.69/ 0.13	1.69/ 0.13	1.91/ 0.16	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock							
$T_{\text{DSPDCK}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG_MULT}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG_MULT}}}$	{A, ACIN, B, BCIN} input to P register CLK using multiplier	3.83/ −0.13	4.37/ −0.13	5.20/ −0.13	5.20/ −0.13	5.94/ −0.24	ns
$T_{\text{DSPDCK}_{\text{D_PREG_MULT}}/T_{\text{DSPCKD}_{\text{D_PREG_MULT}}}}$	D input to P register CLK	3.62/ −0.47	4.13/ −0.47	4.90/ −0.47	4.90/ −0.47	5.61/ −0.77	ns
$T_{\text{DSPDCK}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG}}}$	{A, ACIN, B, BCIN} input to P register CLK not using multiplier	1.59/ −0.13	1.81/ −0.13	2.15/ −0.13	2.15/ −0.13	2.44/ −0.24	ns
$T_{\text{DSPDCK}_{\text{C_PREG}}/T_{\text{DSPCKD}_{\text{C_PREG}}}}$	C input to P register CLK	1.42/ −0.10	1.61/ −0.10	1.91/ −0.10	1.91/ −0.10	2.16/ −0.19	ns
$T_{\text{DSPDCK}_{\{\text{PCIN}, \text{CARRYCASCIN}, \text{MULTSIGNIN}\}}_{\text{PREG}}/T_{\text{DSPCKD}_{\{\text{PCIN}, \text{CARRYCASCIN}, \text{MULTSIGNIN}\}}_{\text{PREG}}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK	1.23/ −0.02	1.41/ −0.02	1.67/ −0.02	1.67/ −0.02	1.91/ −0.07	ns
Setup and Hold Times of the CE Pins							
$T_{\text{DSPDCK}_{\{\text{CEA}; \text{CEB}\}}_{\{\text{AREG}; \text{BREG}\}}/T_{\text{DSPCKD}_{\{\text{CEA}; \text{CEB}\}}_{\{\text{AREG}; \text{BREG}\}}}$	{CEA; CEB} input to {A; B} register CLK	0.14/ 0.19	0.17/ 0.22	0.22/ 0.25	0.22/ 0.25	0.30/ 0.28	ns
$T_{\text{DSPDCK}_{\text{CEC_CREG}}/T_{\text{DSPCKD}_{\text{CEC_CREG}}}}$	CEC input to C register CLK	0.15/ 0.18	0.18/ 0.20	0.24/ 0.23	0.24/ 0.23	0.31/ 0.26	ns
$T_{\text{DSPDCK}_{\text{CED_DREG}}/T_{\text{DSPCKD}_{\text{CED_DREG}}}}$	CED input to D register CLK	0.20/ 0.12	0.24/ 0.13	0.31/ 0.14	0.31/ 0.14	0.43/ 0.16	ns
$T_{\text{DSPDCK}_{\text{CEM_MREG}}/T_{\text{DSPCKD}_{\text{CEM_MREG}}}}$	CEM input to M register CLK	0.16/ 0.19	0.20/ 0.21	0.26/ 0.25	0.26/ 0.25	0.32/ 0.28	ns
$T_{\text{DSPDCK}_{\text{CEP_PREG}}/T_{\text{DSPCKD}_{\text{CEP_PREG}}}}$	CEP input to P register CLK	0.32/ 0.02	0.38/ 0.02	0.46/ 0.03	0.46/ 0.03	0.54/ 0.04	ns
Setup and Hold Times of the RST Pins							
$T_{\text{DSPDCK}_{\{\text{RSTA}; \text{RSTB}\}}_{\{\text{AREG}; \text{BREG}\}}/T_{\text{DSPCKD}_{\{\text{RSTA}; \text{RSTB}\}}_{\{\text{AREG}; \text{BREG}\}}}$	{RSTA, RSTB} input to {A, B} register CLK	0.27/ 0.17	0.31/ 0.19	0.38/ 0.22	0.38/ 0.22	0.41/ 0.25	ns
$T_{\text{DSPDCK}_{\text{RSTC_CREG}}/T_{\text{DSPCKD}_{\text{RSTC_CREG}}}}$	RSTC input to C register CLK	0.18/ 0.08	0.20/ 0.08	0.23/ 0.09	0.23/ 0.09	0.27/ 0.11	ns
$T_{\text{DSPDCK}_{\text{RSTD_DREG}}/T_{\text{DSPCKD}_{\text{RSTD_DREG}}}}$	RSTD input to D register CLK	0.28/ 0.15	0.32/ 0.16	0.38/ 0.19	0.38/ 0.19	0.45/ 0.21	ns
$T_{\text{DSPDCK}_{\text{RSTM_MREG}}/T_{\text{DSPCKD}_{\text{RSTM_MREG}}}}$	RSTM input to M register CLK	0.20/ 0.24	0.23/ 0.26	0.26/ 0.30	0.26/ 0.30	0.29/ 0.34	ns

Table 59: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T _{SMCKBY}	CCLK to BUSY out in readback at 2.5V	6	6	6	7	ns, Max
	CCLK to BUSY out in readback at 1.8V	6	6	6	7	ns, Max
F _{SMCK}	Maximum Frequency with respect to nominal CCLK	100	100	100	70	MHz, Max
F _{RBCK}	Maximum Readback Frequency with respect to nominal CCLK	100	100	100	60	MHz, Max
F _{MCCKTOL}	Frequency tolerance, master mode with respect to nominal CCLK	55	55	55	60	%
Boundary-Scan Port Timing Specifications						
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI Setup time before TCK/ Hold time after TCK	3.0/2.0	3.0/2.0	3.0/2.0	4.0/2.0	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output valid at 2.5V	6	6	6	7	ns, Max
	TCK falling edge to TDO output valid at 1.8V	6	6	6	7	ns, Max
F _{TCK}	Maximum configuration TCK clock frequency	66	66	66	33	MHz, Max
F _{TCKB_MIN}	Minimum boundary-scan TCK clock frequency when using IEEE Std 1149.6 (AC-JTAG). Minimum operating temperature for IEEE Std 1149.6 is 0°C.	15	15	15	15	MHz, Min
F _{TCKB}	Maximum boundary-scan TCK clock frequency	66	66	66	33	MHz, Max
BPI Master Flash Mode Programming Switching						
T _{BPICCO} ⁽²⁾	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 2.5V	6	6	6	7	ns
	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 1.8V	6	6	6	7	ns
T _{BPIDCC} /T _{BPICCD}	Setup/Hold on D[15:0] data input pins	4.0/0.0	4.0/0.0	4.0/0.0	5.0/0.0	ns
T _{INITADDR}	Minimum period of initial ADDR[25:0] address cycles	3	3	3	3	CCLK cycles
SPI Master Flash Mode Programming Switching						
T _{SPIDCC} /T _{SPIDCCD}	DIN Setup/Hold before/after the rising CCLK edge	3.0/0.0	3.0/0.0	3.0/0.0	3.5/0.0	ns
T _{SPICCM}	MOSI clock to out at 2.5V	6	6	6	7	ns
	MOSI clock to out at 1.8V	6	6	6	7	ns
T _{SPICFC}	FCS_B clock to out at 2.5V	6	6	6	7	ns
	FCS_B clock to out at 1.8V	6	6	6	7	ns
T _{FSINIT} /T _{FSINITH}	FS[2:0] to INIT_B rising edge Setup and Hold	2	2	2	2	μs
CCLK Output (Master Modes)						
T _{MCCKL}	Master CCLK clock Low time duty cycle	45/55	45/55	45/55	40/60	%, Min/Max
T _{MCCKH}	Master CCLK clock High time duty cycle	45/55	45/55	45/55	40/60	%, Min/Max
CCLK Input (Slave Modes)						
T _{SCCKL}	Slave CCLK clock minimum Low time	2.5	2.5	2.5	2.5	ns, Min
T _{SCCKH}	Slave CCLK clock minimum High time	2.5	2.5	2.5	2.5	ns, Min
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
F _{DCK}	Maximum frequency for DCLK	200	200	200	200	MHz
T _{MMCMCKD_DADDR} / T _{MMCMCKD_DADDR}	DADDR Setup/Hold	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns

Table 62: Regional Clock Switching Characteristics (BUFR) (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BRDO_O}	Propagation delay from CLR to O	0.69	0.74	0.80	1.12	ns
Maximum Frequency						
$F_{MAX}^{(1)}$	Regional clock tree (BUFR)	500	420	300	300	MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

Table 63: Horizontal Clock Buffer Switching Characteristics (BUFH)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	0.15	ns
T_{BHCK_CE}/T_{BHCK_CE}	CE pin Setup and Hold	0.04/ 0.04	0.04/ 0.04	0.05/ 0.05	0.04/ 0.04	ns
Maximum Frequency						
F_{MAX}	Horizontal clock buffer (BUFH)	800	750	700	667	MHz

MMCM Switching Characteristics

Table 64: MMCM Specification

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F_{INMAX}	Maximum Input Clock Frequency ⁽¹⁾	800	750	700	700	MHz
F_{INMIN}	Minimum Input Clock Frequency	10	10	10	10	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
$F_{INDUTY}^{(2)}$	Allowable Input Duty Cycle: 10—49 MHz	25/75				%
	Allowable Input Duty Cycle: 50—199 MHz	30/70				%
	Allowable Input Duty Cycle: 200—399 MHz	35/65				%
	Allowable Input Duty Cycle: 400—499 MHz	40/60				%
	Allowable Input Duty Cycle: >500 MHz	45/55				%
F_{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	0.01	0.01	MHz
F_{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	550	500	450	450	MHz
F_{VCOMIN}	Minimum MMCM VCO Frequency	600	600	600	600	MHz
F_{VCOMAX}	Maximum MMCM VCO Frequency	1600	1440	1200	1200	MHz
$F_{BANDWIDTH}$	Low MMCM Bandwidth at Typical ⁽³⁾	1.00	1.00	1.00	1.00	MHz
	High MMCM Bandwidth at Typical ⁽³⁾	4.00	4.00	4.00	4.00	MHz
$T_{STATPHAOFFSET}$	Static Phase Offset of the MMCM Outputs ⁽⁴⁾	0.12	0.12	0.12	0.12	ns
$T_{OUTJITTER}$	MMCM Output Jitter ⁽⁵⁾	Note 3				
$T_{OUTDUTY}$	MMCM Output Clock Duty Cycle Precision ⁽⁶⁾	0.15	0.20	0.20	0.20	ns
$T_{LOCKMAX}$	MMCM Maximum Lock Time	100	100	100	100	μs
F_{OUTMAX}	MMCM Maximum Output Frequency	800	750	700	700	MHz
F_{OUTMIN}	MMCM Minimum Output Frequency ⁽⁷⁾⁽⁸⁾	4.69	4.69	4.69	4.69	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				

Table 66: Global Clock Input to Output Delay With MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> MMCM.							
T _{ICKOFFMMCMGC}	Global Clock Input and OUTFF <i>with</i> MMCM	XC6VLX75T	2.34	2.50	2.77	2.85	ns
		XC6VLX130T	2.35	2.51	2.78	2.87	ns
		XC6VLX195T	2.36	2.52	2.79	2.88	ns
		XC6VLX240T	2.36	2.52	2.79	2.88	ns
		XC6VLX365T	2.37	2.53	2.79	2.89	ns
		XC6VLX550T	N/A	2.55	2.82	2.93	ns
		XC6VLX760	N/A	2.54	2.82	2.92	ns
		XC6VSX315T	2.35	2.51	2.79	2.87	ns
		XC6VSX475T	N/A	2.43	2.70	2.79	ns
		XC6VHX250T	2.36	2.53	2.80	N/A	ns
		XC6VHX255T	2.46	2.63	2.91	N/A	ns
		XC6VHX380T	2.39	2.59	2.83	N/A	ns
		XC6VHX565T	N/A	2.54	2.81	N/A	ns
		XQ6VLX130T	N/A	2.51	2.78	2.87	ns
		XQ6VLX240T	N/A	2.52	2.79	2.88	ns
		XQ6VLX550T	N/A	N/A	2.82	2.93	ns
		XQ6VSX315T	N/A	2.51	2.79	2.87	ns
		XQ6VSX475T	N/A	N/A	2.70	2.79	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 67: Clock-Capable Clock Input to Output Delay With MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Clock-capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> MMCM.							
T _{ICKOFMMCMCC}	Clock-capable Clock Input and OUTFF <i>with</i> MMCM	XC6VLX75T	2.22	2.38	2.63	2.72	ns
		XC6VLX130T	2.24	2.39	2.65	2.74	ns
		XC6VLX195T	2.24	2.40	2.65	2.75	ns
		XC6VLX240T	2.24	2.40	2.65	2.75	ns
		XC6VLX365T	2.25	2.42	2.65	2.76	ns
		XC6VLX550T	N/A	2.43	2.68	2.80	ns
		XC6VLX760	N/A	2.42	2.69	2.79	ns
		XC6VSX315T	2.23	2.38	2.65	2.73	ns
		XC6VSX475T	N/A	2.30	2.57	2.66	ns
		XC6VHX250T	2.25	2.41	2.67	N/A	ns
		XC6VHX255T	2.35	2.51	2.78	N/A	ns
		XC6VHX380T	2.27	2.43	2.69	N/A	ns
		XC6VHX565T	N/A	2.41	2.68	N/A	ns
		XQ6VLX130T	N/A	2.39	2.65	2.74	ns
		XQ6VLX240T	N/A	2.40	2.65	2.75	ns
		XQ6VLX550T	N/A	N/A	2.68	2.80	ns
		XQ6VSX315T	N/A	2.38	2.65	2.73	ns
		XQ6VSX475T	N/A	N/A	2.57	2.66	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

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