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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	128000
Total RAM Bits	9732096
Number of I/O	400
Number of Gates	-
Voltage - Supply	0.91V ~ 0.97V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	784-BBGA, FCBGA
Supplier Device Package	784-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vlx130t-l1ffg784i

Table 3: DC Characteristics Over Recommended Operating Conditions (1)(2)

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	10	μA
I_L	Input or output leakage current per pin (sample-tested)	–	–	10	μA
$C_{IN}^{(3)}$	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 2.5V$	20	–	80	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.8V$	8	–	40	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.5V$	5	–	30	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.2V$	1	–	20	μA
I_{RPD}	Pad pull-down (when selected) @ $V_{IN} = 2.5V$	3	–	80	μA
I_{BATT}	Battery supply current	–	–	150	nA
n	Temperature diode ideality factor	–	1.0002	–	n
r	Series resistance	–	5	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst case process at 25°C.
3. This measurement represents the die capacitance at the pad, not including the package.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on sequence and ramp rate of the power supply.

The recommended power-on sequence for Virtex-6 devices is V_{CCINT} , V_{CCAUX} , and V_{CCO} to meet the power-up current requirements listed in Table 5. V_{CCINT} can be powered up or down at any time, but power up current specifications can vary from Table 5. The device will have no physical damage or reliability concerns if V_{CCINT} , V_{CCAUX} , and V_{CCO} sequence cannot be followed.

If the recommended power-up sequence cannot be followed and the I/Os must remain 3-stated throughout configuration, then V_{CCAUX} must be powered prior to V_{CCO} or V_{CCAUX} and V_{CCO} must be powered by the same supply. Similarly, for power-down, the reverse V_{CCAUX} and V_{CCO} sequence is recommended if the I/Os are to remain 3-stated.

The GTH transceiver supplies must be powered using a MGTHAVCC, MGTHAVCCR, MGTHAVCCPLL, and MGTHAVTT sequence. There are no sequencing requirement for these supplies with respect to the other FPGA supply voltages. For more detail see Table 27: *GTH Transceiver Power Supply Sequencing*. There are no sequencing requirements for the GTX transceivers power supplies.

Table 5 shows the minimum current, in addition to I_{CCQ} , that are required by Virtex-6 devices for proper power-on and configuration. If the current minimums shown in Table 4 and Table 5 are met, the device powers on after all three supplies have passed through their power-on reset threshold voltages. The FPGA must be configured after applying V_{CCINT} , V_{CCAUX} , and V_{CCO} for the appropriate configuration banks. Once initialized and configured, use the XPE tools to estimate current drain on these supplies.

Table 5: Power-On Current for Virtex-6 Devices

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	Units
	Typ ⁽¹⁾	Typ ⁽¹⁾	Typ ⁽¹⁾	
XC6VLX75T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 10$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VLX130T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 10$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VLX195T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VLX240T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VLX365T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VLX550T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VLX760	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VSX315T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VSX475T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 50$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VHX250T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VHX255T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VHX380T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VHX565T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XQ6VLX130T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 100$	$I_{CCOQ} + 30$ mA per bank	mA
XQ6VLX240T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 100$	$I_{CCOQ} + 30$ mA per bank	mA
XQ6VLX550T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 100$	$I_{CCOQ} + 30$ mA per bank	mA
XQ6VSX315T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 100$	$I_{CCOQ} + 40$ mA per bank	mA
XQ6VSX475T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 100$	$I_{CCOQ} + 40$ mA per bank	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Use the XPower Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate maximum power-on currents.

HT DC Specifications (HT_25)

Table 8: HT DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage for XC devices	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	480	600	885	mV
	Differential Output Voltage for XQ devices		480	600	930	mV
ΔV_{OD}	Change in V_{OD} Magnitude		-15	—	15	mV
V_{OCM}	Output Common Mode Voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	440	600	760	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		-15	—	15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		-15	—	15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		-15	—	15	mV

LVDS DC Specifications (LVDS_25)

Table 9: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	—	—	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.825	—	—	V
V_{ODIFF}	Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage for XC devices	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
	Output Common-Mode Voltage for XQ devices		1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 10: Extended LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	—	—	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.715	—	—	V
V_{ODIFF}	Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High for XC devices	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	350	—	840	mV
	Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High for XQ devices		350	—	850	mV
V_{OCM}	Output Common-Mode Voltage for XC devices	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
	Output Common-Mode Voltage for XQ devices		1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	—	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ± 350 mV	0.3	1.2	2.2	V

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 13: Absolute Maximum Ratings for GTX Transceivers⁽¹⁾

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	−0.5	1.1	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	−0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	−0.5	1.32	V
V _{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	−0.5	1.32	V
V _{MGTREFCLK}	Reference clock absolute input voltage	−0.5	1.32	V

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 14: Recommended Operating Conditions for GTX Transceivers⁽¹⁾⁽²⁾

Symbol	Description	Speed Grade	PLL Frequency	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	-3, -2 ⁽³⁾	> 2.7 GHz	1.0	1.03	1.06	V
		-3, -2 ⁽³⁾	≤ 2.7 GHz	0.95	1.0	1.06	V
		-1	≤ 2.7 GHz	0.95	1.0	1.06	V
		-1L	≤ 2.7 GHz	0.95	1.0	1.05	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	All	—	1.14	1.2	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	All	—	1.14	1.2	1.26	V

Notes:

- Each voltage listed requires the filter circuit described in [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#).
- Voltages are specified for the temperature range of T_j = −40°C to +100°C for all XC devices and T_j = −55°C to +125°C for the XQ devices.
- If a GTX Quad contains transceivers operating with a mixture of PLL frequencies above and below 2.7 GHz, the MGTAVCC voltage supply must be in the range of 1.0V to 1.06V.

Table 15: GTX Transceiver Supply Current (per Lane) ⁽¹⁾⁽²⁾

Symbol	Description	Typ	Max	Units
I _{MGTAVTT}	MGTAVTT supply current for one GTX transceiver	55.9	Note 2	mA
I _{MGTAVCC}	MGTAVCC supply current for one GTX transceiver	56.1		mA
MGTR _{REF}	Precision reference resistor for internal calibration termination	100.0 ± 1% tolerance		Ω

Notes:

- Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
- Values for currents of other transceiver configurations and conditions can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

Table 16: GTX Transceiver Quiescent Supply Current (per Lane) ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Description	Typ ⁽⁴⁾	Max	Units
$I_{\text{MGTA VTTQ}}$	Quiescent MGTA VTT supply current for one GTX transceiver	0.9	Note 2	mA
$I_{\text{MGTA VCCQ}}$	Quiescent MGTA VCC supply current for one GTX transceiver	3.5		mA

Notes:

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.
3. GTX transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX transceivers.
4. Typical values are specified at nominal voltage, 25°C.

GTX Transceiver DC Input and Output Levels

Table 17 summarizes the DC output specifications of the GTX transceivers in Virtex-6 FPGAs. Consult [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#) for further details.

Table 17: GTX Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled ≤ 4.25 Gb/s	125	–	2000	mV
		External AC coupled > 4.25 Gb/s	175	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled MGTA VTT = 1.2V	–400	–	MGTA VTT	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTA VTT = 1.2V	–	2/3 MGTA VTT	–	mV
DV_{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	–	–	1000	mV
V_{CMOUTDC}	DC common mode output voltage.	Equation based	$\text{MGTA VTT} - DV_{\text{PPOUT}}/4$			mV
R_{IN}	Differential input resistance		80	100	130	Ω
R_{OUT}	Differential output resistance		80	100	120	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	8	ps
C_{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#) and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

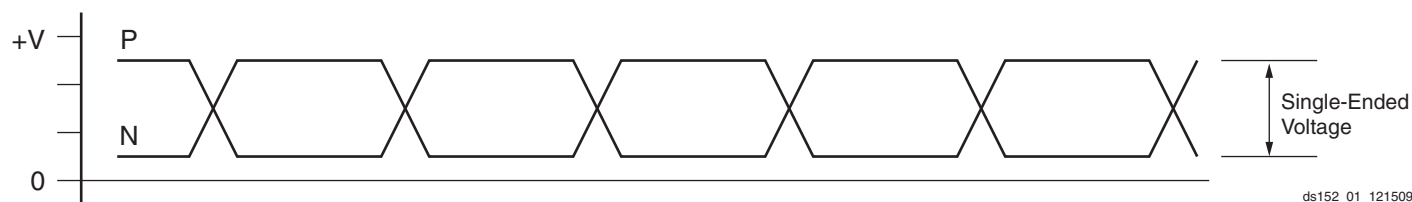


Figure 1: Single-Ended Peak-to-Ppeak Voltage

Table 23: GTX Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTXTX}	Serial data rate range		0.480	–	F _{GTXMAX}	Gb/s
T _{RTX}	TX Rise time	20%–80%	–	120	–	ps
T _{FTX}	TX Fall time	80%–20%	–	120	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	350	ps
V _{TXOOBVDPP}	Electrical idle amplitude		–	–	15	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		–	–	75	ns
TJ _{6.5}	Total Jitter ⁽²⁾⁽³⁾	6.5 Gb/s	–	–	0.33	UI
DJ _{6.5}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.17	UI
TJ _{5.0}	Total Jitter ⁽²⁾⁽³⁾	5.0 Gb/s	–	–	0.33	UI
DJ _{5.0}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.15	UI
TJ _{4.25}	Total Jitter ⁽²⁾⁽³⁾	4.25 Gb/s	–	–	0.33	UI
DJ _{4.25}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.14	UI
TJ _{3.75}	Total Jitter ⁽²⁾⁽³⁾	3.75 Gb/s	–	–	0.34	UI
DJ _{3.75}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.16	UI
TJ _{3.125}	Total Jitter ⁽²⁾⁽³⁾	3.125 Gb/s	–	–	0.2	UI
DJ _{3.125}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.1	UI
TJ _{3.125L}	Total Jitter ⁽²⁾⁽³⁾	3.125 Gb/s ⁽⁴⁾	–	–	0.35	UI
DJ _{3.125L}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.16	UI
TJ _{2.5}	Total Jitter ⁽²⁾⁽³⁾	2.5 Gb/s ⁽⁵⁾	–	–	0.20	UI
DJ _{2.5}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.08	UI
TJ _{1.25}	Total Jitter ⁽²⁾⁽³⁾	1.25 Gb/s ⁽⁶⁾	–	–	0.15	UI
DJ _{1.25}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.06	UI
TJ ₆₀₀	Total Jitter ⁽²⁾⁽³⁾	600 Mb/s	–	–	0.1	UI
DJ ₆₀₀	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.03	UI
TJ ₄₈₀	Total Jitter ⁽²⁾⁽³⁾	480 Mb/s	–	–	0.1	UI
DJ ₄₈₀	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
- Using PLL_DIVSEL_FB = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 1e⁻¹².
- PLL frequency at 1.5625 GHz and OUTDIV = 1.
- PLL frequency at 2.5 GHz and OUTDIV = 2.
- PLL frequency at 2.5 GHz and OUTDIV = 4.

Table 24: GTX Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
F _{GTXRX}	Serial data rate	RX oversampler not enabled	0.600	–	F _{GTXMAX}	Gb/s
		RX oversampler enabled	0.480	–	0.600	Gb/s
T _{RXELECIDLE}	Time for RXELECIdle to respond to loss or restoration of data		–	75	–	ns
RX _{OOBVDPP}	OOB detect threshold peak-to-peak		60	–	150	mV
RX _{SST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated @ 33 KHz	–5000	–	0	ppm
RX _{RL}	Run length (CID)	Internal AC capacitor bypassed	–	–	512	UI
RX _{PPMTOL}	Data/REFCLK PPM offset tolerance	CDR 2 nd -order loop disabled	–200	–	200	ppm
		CDR 2 nd -order loop enabled	–2000	–	2000	ppm
SJ Jitter Tolerance ⁽²⁾						
JT_SJ _{6.5}	Sinusoidal Jitter ⁽³⁾	6.5 Gb/s	0.44	–	–	UI
JT_SJ _{5.0}	Sinusoidal Jitter ⁽³⁾	5.0 Gb/s	0.44	–	–	UI
JT_SJ _{4.25}	Sinusoidal Jitter ⁽³⁾	4.25 Gb/s	0.44	–	–	UI
JT_SJ _{3.75}	Sinusoidal Jitter ⁽³⁾	3.75 Gb/s	0.44	–	–	UI
JT_SJ _{3.125}	Sinusoidal Jitter ⁽³⁾	3.125 Gb/s	0.45	–	–	UI
JT_SJ _{3.125L}	Sinusoidal Jitter ⁽³⁾	3.125 Gb/s ⁽⁴⁾	0.45	–	–	UI
JT_SJ _{2.5}	Sinusoidal Jitter ⁽³⁾	2.5 Gb/s ⁽⁵⁾	0.5	–	–	UI
JT_SJ _{1.25}	Sinusoidal Jitter ⁽³⁾	1.25 Gb/s ⁽⁶⁾	0.5	–	–	UI
JT_SJ ₆₀₀	Sinusoidal Jitter ⁽³⁾	600 Mb/s	0.4	–	–	UI
JT_SJ ₄₈₀	Sinusoidal Jitter ⁽³⁾	480 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye ⁽²⁾						
JT_TJSE _{3.125}	Total Jitter with Stressed Eye ⁽⁷⁾	3.125 Gb/s	0.70	–	–	UI
		5.0 Gb/s	0.70	–	–	UI
JT_SJSE _{3.125}	Sinusoidal Jitter with Stressed Eye ⁽⁷⁾	3.125 Gb/s	0.1	–	–	UI
		5.0 Gb/s	0.1	–	–	UI

Notes:

- Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 1e^{–12}.
- The frequency of the injected sinusoidal jitter is 80 MHz.
- PLL frequency at 1.5625 GHz and OUTDIV = 1.
- PLL frequency at 2.5 GHz and OUTDIV = 2.
- PLL frequency at 2.5 GHz and OUTDIV = 4.
- Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver DC Input and Output Levels

Table 30 summarizes the DC output specifications of the GTH transceivers in Virtex-6 FPGAs. Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further details.

Table 30: GTH Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
D_{VPPIN}	Differential peak-to-peak input voltage	External AC coupled	175	–	1200	mV
D_{VPPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	800	–	1200	mV
R_{IN}	Differential input resistance		80	100	120	Ω
R_{OUT}	Differential output resistance		80	100	120	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	–	ps
C_{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 31 summarizes the DC specifications of the clock input of the GTH transceiver. Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further details.

Table 31: GTH Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	≤ 600 MHz	500	–	1600	mV
		> 600 MHz	600	–	1600	mV
R_{IN}	Differential input resistance		80	100	120	Ω
C_{EXT}	Required external AC coupling capacitor		–	100	–	nF

Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.17 for -3, -2, and -1; and v1.10 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

[Table 42](#) correlates the current status of each Virtex-6 device on a per speed grade basis.

Table 42: Virtex-6 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6VLX75T			-3, -2, -1, -1L
XC6VLX130T			-3, -2, -1, -1L
XC6VLX195T			-3, -2, -1, -1L
XC6VLX240T			-3, -2, -1, -1L
XC6VLX365T			-3, -2, -1, -1L
XC6VLX550T			-2, -1, -1L
XC6VLX760			-2, -1, -1L
XC6VSX315T			-3, -2, -1, -1L
XC6VSX475T			-2, -1, -1L
XC6VHX250T			-3, -2, -1
XC6VHX255T			-3, -2, -1
XC6VHX380T			-3, -2, -1
XC6VHX565T			-2, -1
XQ6VLX130T			-2, -1, -1L
XQ6VLX240T			-2, -1, -1L
XQ6VLX550T			-1, -1L
XQ6VSX315T			-2, -1, -1L
XQ6VSX475T			-1, -1L

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 devices.

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDCI_DV2_25	0.51	0.57	0.66	0.70	1.71	1.83	2.01	2.00	1.71	1.83	2.01	2.00	ns
LVDCI_DV2_18	0.55	0.61	0.71	0.73	1.69	1.81	2.00	1.98	1.69	1.81	2.00	1.98	ns
LVDCI_DV2_15	0.64	0.73	0.85	0.85	1.68	1.77	1.91	1.98	1.68	1.77	1.91	1.98	ns
LVPECL_25	0.85	0.94	1.09	1.08	1.38	1.49	1.65	1.64	1.38	1.49	1.65	1.64	ns
HSTL_I_12	0.81	0.91	1.06	1.06	1.48	1.60	1.78	1.74	1.48	1.60	1.78	1.74	ns
HSTL_I_DCI	0.81	0.91	1.06	1.06	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
HSTL_II_DCI	0.81	0.91	1.06	1.06	1.37	1.49	1.68	1.66	1.37	1.49	1.68	1.66	ns
HSTL_II_T_DCI	0.81	0.91	1.06	1.06	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
HSTL_III_DCI	0.81	0.91	1.06	1.06	1.34	1.45	1.62	1.61	1.34	1.45	1.62	1.61	ns
HSTL_I_DCI_18	0.81	0.91	1.06	1.06	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
HSTL_II_DCI_18	0.81	0.91	1.06	1.06	1.36	1.46	1.62	1.59	1.36	1.46	1.62	1.59	ns
HSTL_II_T_DCI_18	0.81	0.91	1.06	1.06	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
HSTL_III_DCI_18	0.81	0.91	1.06	1.06	1.43	1.54	1.69	1.67	1.43	1.54	1.69	1.67	ns
DIFF_HSTL_I_18	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
DIFF_HSTL_I_DCI_18	0.85	0.94	1.09	1.08	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
DIFF_HSTL_I	0.85	0.94	1.09	1.08	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns
DIFF_HSTL_I_DCI	0.85	0.94	1.09	1.08	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
DIFF_HSTL_II_18	0.85	0.94	1.09	1.08	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
DIFF_HSTL_II_DCI_18	0.85	0.94	1.09	1.08	1.36	1.46	1.62	1.59	1.36	1.46	1.62	1.59	ns
DIFF_HSTL_II_T_DCI_18	0.85	0.94	1.09	1.08	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
DIFF_HSTL_II	0.85	0.94	1.09	1.08	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
DIFF_HSTL_II_DCI	0.85	0.94	1.09	1.08	1.37	1.49	1.68	1.66	1.37	1.49	1.68	1.66	ns
SSTL2_I_DCI	0.81	0.91	1.06	1.06	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
SSTL2_II_DCI	0.81	0.91	1.06	1.06	1.39	1.50	1.67	1.69	1.39	1.50	1.67	1.69	ns
SSTL2_II_T_DCI	0.81	0.91	1.06	1.06	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
SSTL18_I	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
SSTL18_II	0.81	0.91	1.06	1.06	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
SSTL18_I_DCI	0.81	0.91	1.06	1.06	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
SSTL18_II_DCI	0.81	0.91	1.06	1.06	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
SSTL18_II_T_DCI	0.81	0.91	1.06	1.06	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL2_I	0.85	0.94	1.09	1.08	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
DIFF_SSTL2_I_DCI	0.85	0.94	1.09	1.08	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
DIFF_SSTL2_II	0.85	0.94	1.09	1.08	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
DIFF_SSTL2_II_DCI	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.69	1.39	1.50	1.67	1.69	ns
DIFF_SSTL2_II_T_DCI	0.85	0.94	1.09	1.08	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
DIFF_SSTL18_II	0.94	1.09	1.08	1.50	2.27	1.66	1.50	2.27	1.66	ns
DIFF_SSTL18_II_DCI	0.94	1.09	1.08	1.47	2.20	1.62	1.47	2.20	1.62	ns
DIFF_SSTL18_II_T_DCI	0.94	1.09	1.08	1.51	2.30	1.65	1.51	2.30	1.65	ns
DIFF_SSTL15	0.91	1.06	1.06	1.54	2.25	1.69	1.54	2.25	1.69	ns
DIFF_SSTL15_DCI	0.91	1.06	1.06	1.52	2.25	1.66	1.52	2.25	1.66	ns
DIFF_SSTL15_T_DCI	0.91	1.06	1.06	1.52	2.25	1.66	1.52	2.25	1.66	ns

Table 46: IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{IOTPHZ}	T input to Pad high-impedance	0.86	0.92	0.99	0.99	ns

Table 48: Output Delay Measurement Methodology (Cont'd)

Description	I/O Standard Attribute	R _{REF} (Ω)	C _{REF} ⁽¹⁾ (pF)	V _{MEAS} (V)	V _{REF} (V)
HT (HyperTransport), 2.5V	LDT_25	100	0	0 ⁽²⁾	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	100	0	0 ⁽²⁾	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V _{REF}	0.75
HSTL, Class III, with DCI	HSTL_III_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V _{REF}	0.9
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termini.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V _{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V _{REF}	1.25

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 49: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Setup/Hold						
T _{ICE1CK} /T _{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.21/ 0.03	0.25/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T _{ISRCK} /T _{ICKSR}	SR pin Setup/Hold with respect to CLK	0.66/ −0.08	0.78/ −0.08	0.96/ −0.08	1.09/ −0.11	ns
T _{IDOCK} /T _{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.07/ 0.41	0.08/ 0.46	0.10/ 0.54	0.11/ 0.64	ns
T _{IDOCKD} /T _{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.10/ 0.32	0.12/ 0.36	0.14/ 0.42	0.16/ 0.50	ns
Combinatorial						
T _{IDI}	D pin to O pin propagation delay, no Delay	0.15	0.17	0.20	0.23	ns
T _{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.19	0.22	0.25	0.28	ns
Sequential Delays						
T _{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.48	0.54	0.64	0.73	ns
T _{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.52	0.58	0.68	0.78	ns
T _{ICKQ}	CLK to Q outputs	0.54	0.61	0.70	0.93	ns
T _{RQ_ILOGIC}	SR pin to OQ/TQ out	0.85	0.97	1.15	1.32	ns
T _{GSRQ_ILOGIC}	Global Set/Reset to Q outputs	7.60	7.60	10.51	10.51	ns
Set/Reset						
T _{RPW_ILOGIC}	Minimum Pulse Width, SR inputs	0.78	0.95	1.20	1.30	ns, Min

Table 50: OLOGIC Switching Characteristics

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup/Hold							
T _{ODCK} /T _{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.45/ −0.08	0.50/ −0.08	0.54/ −0.08	0.54/ −0.08	0.69/ −0.11	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.17/ −0.03	0.20/ −0.03	0.22/ −0.03	0.27/ −0.05	0.27/ −0.04	ns
T _{OSRCK} /T _{OCKSR}	SR pin Setup/Hold with respect to CLK	0.59/ −0.24	0.62/ −0.24	0.54/ −0.08	0.54/ −0.08	0.79/ −0.35	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.44/ −0.07	0.51/ −0.07	0.56/ −0.07	0.60/ −0.10	0.68/ −0.13	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.15/ −0.04	0.19/ −0.04	0.21/ −0.04	0.27/ −0.05	0.29/ −0.05	ns
Combinatorial							
T _{DOQ}	D1 to OQ out or T1 to TQ out	0.78	0.87	1.01	1.01	1.15	ns
Sequential Delays							
T _{OCKQ}	CLK to OQ/TQ out	0.54	0.61	0.71	0.71	0.80	ns
T _{RQ}	SR pin to OQ/TQ out	0.80	0.90	1.05	1.05	1.19	ns
T _{GSRQ}	Global Set/Reset to Q outputs	7.60	7.60	10.51	10.51	10.51	ns
Set/Reset							
T _{RPW}	Minimum Pulse Width, SR inputs	0.78	0.95	1.20	1.20	1.30	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 51: ISERDES Switching Characteristics

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup/Hold for Control Lines							
T _{ISCKK_BITSIP} / T _{ISCKC_BITSIP}	BITSLIP pin Setup/Hold with respect to CLKDIV	0.07/ 0.15	0.08/ 0.16	0.09/ 0.17	0.09/ 0.17	0.14/ 0.17	ns
T _{ISCKK_CE} / T _{ISCKC_CE} ⁽²⁾	CE pin Setup/Hold with respect to CLK (for CE1)	0.20/ 0.03	0.25/ 0.04	0.27/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T _{ISCKK_CE2} / T _{ISCKC_CE2} ⁽²⁾	CE pin Setup/Hold with respect to CLKDIV (for CE2)	0.01/ 0.27	0.01 0.29	0.01/ 0.31	0.01/ 0.31	−0.05/ 0.35	ns
Setup/Hold for Data Lines							
T _{ISDCK_D} / T _{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.07/ 0.08	0.08/ 0.09	0.09/ 0.11	0.09/ 0.11	0.11/ 0.19	ns
T _{ISDCK_DDLY} / T _{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY) ⁽¹⁾	0.10/ 0.05	0.12/ 0.06	0.14/ 0.07	0.14/ 0.07	0.16/ 0.15	ns
T _{ISDCK_D_DDR} / T _{ISCKD_D_DDR}	D pin Setup/Hold with respect to CLK at DDR mode	0.07/ 0.08	0.08/ 0.09	0.09/ 0.11	0.09/ 0.11	0.11/ 0.19	ns
T _{ISDCK_DDLY_DDR} / T _{ISCKD_DDLY_DDR}	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY) ⁽¹⁾	0.10/ 0.05	0.12/ 0.06	0.14/ 0.07	0.14/ 0.07	0.16/ 0.15	ns
Sequential Delays							
T _{ISCKO_Q}	CLKDIV to out at Q pin	0.57	0.66	0.75	0.80	0.88	ns
Propagation Delays							
T _{ISDO_DO}	D input to DO output pin	0.19	0.22	0.25	0.25	0.28	ns

Notes:

- Recorded at 0 tap value.
- T_{ISCK_CE2} and T_{ISCK_CE2} are reported as $T_{ISCK_CE} / T_{ISCK_CE}$ in TRACE report.

Output Serializer/Deserializer Switching Characteristics

Table 52: OSERDES Switching Characteristics

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup/Hold							
T _{OSDCK_D} /T _{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.23/ −0.10	0.28/ −0.10	0.31/ −0.10	0.35/ −0.10	0.36/ −0.15	ns
T _{OSDCK_T} /T _{OSCKD_T} ⁽¹⁾	T input Setup/Hold with respect to CLK	0.44/ −0.10	0.51/ −0.09	0.56/ −0.08	0.60/ −0.08	0.68/ −0.15	ns
T _{OSDCK_T2} /T _{OSCKD_T2} ⁽¹⁾	T input Setup/Hold with respect to CLKDIV	0.25/ −0.10	0.27/ −0.09	0.31/ −0.08	0.31/ −0.08	0.47/ −0.15	ns
T _{OSCCK_OCE} /T _{OSCKC_OCE}	OCE input Setup/Hold with respect to CLK	0.17/ −0.03	0.20/ −0.03	0.22/ −0.03	0.27/ −0.03	0.27/ −0.04	ns
T _{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.07	0.07	0.07	0.07	0.08	ns
T _{OSCCK_TCE} /T _{OSCKC_TCE}	TCE input Setup/Hold with respect to CLK	0.15/ −0.04	0.19/ −0.04	0.21/ −0.04	0.27/ −0.04	0.29/ −0.05	ns
Sequential Delays							
T _{OSCKO_OQ}	Clock to out from CLK to OQ	0.63	0.71	0.82	0.82	0.93	ns
T _{OSCKO_TQ}	Clock to out from CLK to TQ	0.63	0.71	0.82	0.82	0.93	ns
Combinatorial							
T _{OSDO_TTQ}	T input to TQ Out	0.76	0.84	0.97	0.97	1.11	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Table 54: CLB Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T _{ITO}	An – Dn inputs to A – D Q outputs	0.59	0.67	0.79	0.85	ns, Max
T _{AXA}	AX inputs to AMUX output	0.31	0.35	0.42	0.44	ns, Max
T _{AXB}	AX inputs to BMUX output	0.35	0.39	0.47	0.50	ns, Max
T _{AXC}	AX inputs to CMUX output	0.39	0.44	0.52	0.56	ns, Max
T _{AXD}	AX inputs to DMUX output	0.42	0.47	0.55	0.60	ns, Max
T _{BXB}	BX inputs to BMUX output	0.30	0.34	0.39	0.44	ns, Max
T _{BXD}	BX inputs to DMUX output	0.38	0.43	0.50	0.55	ns, Max
T _{CXC}	CX inputs to CMUX output	0.26	0.29	0.34	0.37	ns, Max
T _{CXD}	CX inputs to DMUX output	0.30	0.34	0.40	0.44	ns, Max
T _{DXD}	DX inputs to DMUX output	0.30	0.33	0.38	0.43	ns, Max
T _{OPCYA}	An input to COUT output	0.32	0.36	0.41	0.47	ns, Max
T _{OPCYB}	Bn input to COUT output	0.32	0.36	0.41	0.47	ns, Max
T _{OPCYC}	Cn input to COUT output	0.27	0.30	0.34	0.40	ns, Max
T _{OPCYD}	Dn input to COUT output	0.25	0.28	0.32	0.37	ns, Max
T _{AXCY}	AX input to COUT output	0.25	0.28	0.33	0.36	ns, Max
T _{BXCY}	BX input to COUT output	0.22	0.24	0.28	0.31	ns, Max
T _{CXCY}	CX input to COUT output	0.15	0.17	0.20	0.22	ns, Max
T _{DXCY}	DX input to COUT output	0.14	0.16	0.19	0.21	ns, Max
T _{BYP}	CIN input to COUT output	0.06	0.07	0.08	0.09	ns, Max
T _{CINA}	CIN input to AMUX output	0.21	0.24	0.28	0.30	ns, Max
T _{CINB}	CIN input to BMUX output	0.23	0.25	0.29	0.31	ns, Max
T _{CINC}	CIN input to CMUX output	0.23	0.26	0.30	0.33	ns, Max
T _{CIND}	CIN input to DMUX output	0.25	0.29	0.33	0.36	ns, Max
Sequential Delays						
T _{CKO}	Clock to AQ – DQ outputs	0.29	0.33	0.39	0.44	ns, Max
T _{SHCKO}	Clock to AMUX – DMUX outputs	0.36	0.40	0.47	0.53	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T _{DICK} /T _{CKDI}	A – D input to CLK on A – D Flip Flops	0.30/0.17	0.36/0.18	0.43/0.20	0.44/0.25	ns, Min
T _{CECK_CLB} / T _{CKCE_CLB}	CE input to CLK on A – D Flip Flops	0.20/0.00	0.25/0.00	0.32/0.00	0.32/0.01	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D Flip Flops	0.39/–0.07	0.44/–0.07	0.52/–0.07	0.58/–0.08	ns, Min
T _{CINCK} /T _{CKCIN}	CIN input to CLK on A – D Flip Flops	0.16/0.12	0.19/0.14	0.24/0.16	0.23/0.22	ns, Min
Set/Reset						
T _{SRMIN}	SR input minimum pulse width	0.90	0.90	0.97	0.80	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops	0.52	0.58	0.68	0.77	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops	0.41	0.48	0.59	0.61	ns, Max
F _{TOG}	Toggle frequency (for export control)	1412.00	1286.40	1098.00	1098.00	MHz

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

Table 57: Block RAM and FIFO Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{RCKK_WE}/T_{RCKC_WE}	Write Enable (WE) input (Block RAM only)	0.44/ 0.19	0.47/ 0.25	0.52/ 0.35	0.67/ 0.24	ns, Min
$T_{RCKK_WREN}/T_{RCKC_WREN}$	WREN FIFO inputs	0.47/ 0.26	0.50/ 0.27	0.55/ 0.30	0.68/ 0.31	ns, Min
$T_{RCKK_RDEN}/T_{RCKC_RDEN}$	RDEN FIFO inputs	0.46/ 0.26	0.50/ 0.27	0.55/ 0.30	0.67/ 0.31	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers ⁽¹⁰⁾	0.90	0.98	1.10	1.23	ns, Max
$T_{RCKK_RSTREG}/T_{RCKC_RSTREG}$	FIFO reset timing ⁽¹¹⁾	0.22/ 0.23	0.24/ 0.24	0.28/ 0.26	0.31/ 0.27	ns, Min
Maximum Frequency						
F_{MAX}	Block RAM in TDP and SDP modes (Write First and No Change modes)	600	540	450	340	MHz
	Block RAM (Read First mode)	525	475	400	275	MHz
	Block RAM (SDP mode) ⁽¹²⁾	525	475	400	275	MHz
$F_{MAX_CASCADE}$	Block RAM Cascade (Write First and No Change modes)	550	490	400	300	MHz
	Block RAM Cascade (Read First mode)	475	425	350	235	MHz
F_{MAX_FIFO}	FIFO in all modes	600	540	450	340	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	450	400	325	250	MHz

Notes:

- TRACE will report all of these parameters as T_{RCKO_DO} .
- T_{RCKO_DOR} includes T_{RCKO_DOW} , T_{RCKO_DOPR} , and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
- These parameters also apply to synchronous FIFO with $DO_REG = 0$.
- T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
- These parameters also apply to multirate (asynchronous) and synchronous FIFO with $DO_REG = 1$.
- T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY} , T_{RCKO_AFULL} , T_{RCKO_EMPTY} , T_{RCKO_FULL} , T_{RCKO_RDERR} , T_{RCKO_WRERR} .
- $T_{RCKO_POINTERS}$ includes both $T_{RCKO_RDCOUNT}$ and $T_{RCKO_WRCOUNT}$.
- The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
- T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
- T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
- The FIFO reset must be asserted for at least three positive clock edges.
- When using ISE software v12.4 or later, if the RDADDR_COLLISION_HWCONFIG attribute is set to PERFORMANCE or the block RAM is in single-port operation, then the faster F_{MAX} for WRITE_FIRST/NO_CHANGE modes apply.

DSP48E1 Switching Characteristics

Table 58: DSP48E1 Switching Characteristics

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock							
$T_{\text{DSPDCK}_{\{A, \text{ACIN}; B, \text{BCIN}\}}_{\{\text{AREG}; \text{BREG}\}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}; B, \text{BCIN}\}}_{\{\text{AREG}; \text{BREG}\}}}$	{A, ACIN, B, BCIN} input to {A, B} register CLK	0.25/ 0.27	0.29/ 0.30	0.35/ 0.34	0.36/ 0.34	0.46/ 0.39	ns
$T_{\text{DSPDCK}_{\text{C_CREG}}/T_{\text{DSPCKD}_{\text{C_CREG}}}}$	C input to C register CLK	0.16/ 0.20	0.19/ 0.22	0.22/ 0.24	0.25/ 0.24	0.33/ 0.30	ns
$T_{\text{DSPDCK}_{\text{D_DREG}}/T_{\text{DSPCKD}_{\text{D_DREG}}}}$	D input to D register CLK	0.07/ 0.31	0.10/ 0.34	0.15/ 0.39	0.16/ 0.39	0.24/ 0.45	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock							
$T_{\text{DSPDCK}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{MREG_MULT}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{MREG_MULT}}}$	{A, ACIN, B, BCIN} input to M register CLK	2.36/ 0.04	2.70/ 0.04	3.21/ 0.04	3.21/ 0.04	3.66/ 0.02	ns
$T_{\text{DSPDCK}_{\{A, D\}}_{\text{ADREG}}/T_{\text{DSPCKD}_{\{A, D\}}_{\text{ADREG}}}$	{A, D} input to AD register CLK	1.24/ 0.10	1.42/ 0.12	1.69/ 0.13	1.69/ 0.13	1.91/ 0.16	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock							
$T_{\text{DSPDCK}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG_MULT}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG_MULT}}}$	{A, ACIN, B, BCIN} input to P register CLK using multiplier	3.83/ −0.13	4.37/ −0.13	5.20/ −0.13	5.20/ −0.13	5.94/ −0.24	ns
$T_{\text{DSPDCK}_{\text{D_PREG_MULT}}/T_{\text{DSPCKD}_{\text{D_PREG_MULT}}}}$	D input to P register CLK	3.62/ −0.47	4.13/ −0.47	4.90/ −0.47	4.90/ −0.47	5.61/ −0.77	ns
$T_{\text{DSPDCK}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG}}}$	{A, ACIN, B, BCIN} input to P register CLK not using multiplier	1.59/ −0.13	1.81/ −0.13	2.15/ −0.13	2.15/ −0.13	2.44/ −0.24	ns
$T_{\text{DSPDCK}_{\text{C_PREG}}/T_{\text{DSPCKD}_{\text{C_PREG}}}}$	C input to P register CLK	1.42/ −0.10	1.61/ −0.10	1.91/ −0.10	1.91/ −0.10	2.16/ −0.19	ns
$T_{\text{DSPDCK}_{\{\text{PCIN}, \text{CARRYCASCIN}, \text{MULTSIGNIN}\}}_{\text{PREG}}/T_{\text{DSPCKD}_{\{\text{PCIN}, \text{CARRYCASCIN}, \text{MULTSIGNIN}\}}_{\text{PREG}}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK	1.23/ −0.02	1.41/ −0.02	1.67/ −0.02	1.67/ −0.02	1.91/ −0.07	ns
Setup and Hold Times of the CE Pins							
$T_{\text{DSPDCK}_{\{\text{CEA}; \text{CEB}\}}_{\{\text{AREG}; \text{BREG}\}}/T_{\text{DSPCKD}_{\{\text{CEA}; \text{CEB}\}}_{\{\text{AREG}; \text{BREG}\}}}$	{CEA; CEB} input to {A; B} register CLK	0.14/ 0.19	0.17/ 0.22	0.22/ 0.25	0.22/ 0.25	0.30/ 0.28	ns
$T_{\text{DSPDCK}_{\text{CEC_CREG}}/T_{\text{DSPCKD}_{\text{CEC_CREG}}}}$	CEC input to C register CLK	0.15/ 0.18	0.18/ 0.20	0.24/ 0.23	0.24/ 0.23	0.31/ 0.26	ns
$T_{\text{DSPDCK}_{\text{CED_DREG}}/T_{\text{DSPCKD}_{\text{CED_DREG}}}}$	CED input to D register CLK	0.20/ 0.12	0.24/ 0.13	0.31/ 0.14	0.31/ 0.14	0.43/ 0.16	ns
$T_{\text{DSPDCK}_{\text{CEM_MREG}}/T_{\text{DSPCKD}_{\text{CEM_MREG}}}}$	CEM input to M register CLK	0.16/ 0.19	0.20/ 0.21	0.26/ 0.25	0.26/ 0.25	0.32/ 0.28	ns
$T_{\text{DSPDCK}_{\text{CEP_PREG}}/T_{\text{DSPCKD}_{\text{CEP_PREG}}}}$	CEP input to P register CLK	0.32/ 0.02	0.38/ 0.02	0.46/ 0.03	0.46/ 0.03	0.54/ 0.04	ns
Setup and Hold Times of the RST Pins							
$T_{\text{DSPDCK}_{\{\text{RSTA}; \text{RSTB}\}}_{\{\text{AREG}; \text{BREG}\}}/T_{\text{DSPCKD}_{\{\text{RSTA}; \text{RSTB}\}}_{\{\text{AREG}; \text{BREG}\}}}$	{RSTA, RSTB} input to {A, B} register CLK	0.27/ 0.17	0.31/ 0.19	0.38/ 0.22	0.38/ 0.22	0.41/ 0.25	ns
$T_{\text{DSPDCK}_{\text{RSTC_CREG}}/T_{\text{DSPCKD}_{\text{RSTC_CREG}}}}$	RSTC input to C register CLK	0.18/ 0.08	0.20/ 0.08	0.23/ 0.09	0.23/ 0.09	0.27/ 0.11	ns
$T_{\text{DSPDCK}_{\text{RSTD_DREG}}/T_{\text{DSPCKD}_{\text{RSTD_DREG}}}}$	RSTD input to D register CLK	0.28/ 0.15	0.32/ 0.16	0.38/ 0.19	0.38/ 0.19	0.45/ 0.21	ns
$T_{\text{DSPDCK}_{\text{RSTM_MREG}}/T_{\text{DSPCKD}_{\text{RSTM_MREG}}}}$	RSTM input to M register CLK	0.20/ 0.24	0.23/ 0.26	0.26/ 0.30	0.26/ 0.30	0.29/ 0.34	ns

Table 58: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
$T_{DSPDO_PCIN, CARRYCASCIN, MULTSIGNIN_PCOUT, CARRYCASCOUT, MULTSIGNOUT}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.28	1.46	1.72	1.72	2.06	ns
Clock to Outs from Output Register Clock to Output Pins							
$T_{DSPCKO_P, CARRYOUT_PREG}$	CLK (PREG) to {P, CARRYOUT} output	0.38	0.43	0.50	0.50	0.57	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_PREG}$	CLK (PREG) to {CARRYCASCOUT, PCOUT, MULTSIGNOUT} output	0.50	0.56	0.66	0.66	0.76	ns
Clock to Outs from Pipeline Register Clock to Output Pins							
$T_{DSPCKO_P, CARRYOUT_MREG}$	CLK (MREG) to {P, CARRYOUT} output	1.72	1.96	2.30	2.30	2.69	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_MREG}$	CLK (MREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.81	2.06	2.43	2.43	2.88	ns
$T_{DSPCKO_P, CARRYOUT_ADREG_MULT}$	CLK (ADREG) to {P, CARRYOUT} output	2.79	3.16	3.72	3.72	4.32	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_ADREG_MULT}$	CLK (ADREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.87	3.26	3.84	3.84	4.51	ns
Clock to Outs from Input Register Clock to Output Pins							
$T_{DSPCKO_P, CARRYOUT_AREG, BREG_MULT}$	CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier	3.97	4.52	5.36	5.36	6.20	ns
$T_{DSPCKO_P, CARRYOUT_AREG, BREG}$	CLK (AREG, BREG) to {P, CARRYOUT} output not using multiplier	1.70	1.93	2.27	2.27	2.65	ns
$T_{DSPCKO_P, CARRYOUT_CREG}$	CLK (CREG) to {P, CARRYOUT} output	1.70	1.93	2.27	2.27	2.80	ns
$T_{DSPCKO_P, CARRYOUT_DREG_MULT}$	CLK (DREG) to {P, CARRYOUT} output	3.89	4.44	5.25	5.25	6.07	ns
Clock to Outs from Input Register Clock to Cascading Output Pins							
$T_{DSPCKO_ACOUT, BCOUT_AREG, BREG}$	CLK (AREG, BREG) to {P, CARRYOUT} output	0.66	0.76	0.89	0.89	1.01	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_AREG, BREG_MULT}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	4.05	4.63	5.49	5.49	6.39	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_AREG, BREG}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.79	2.03	2.40	2.40	2.84	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_DREG_MULT}$	CLK (DREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.98	4.54	5.38	5.38	6.26	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_CREG}$	CLK (CREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.78	2.03	2.40	2.40	2.99	ns

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 FPGA clock transmitter and receiver data-valid windows.

Table 71: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion ⁽¹⁾	All	0.12	0.12	0.12	0.12	ns
T_{CKSKEW}	Global Clock Tree Skew ⁽²⁾	XC6VLX75T	0.15	0.16	0.18	0.17	ns
		XC6VLX130T	0.25	0.26	0.29	0.28	ns
		XC6VLX195T	0.26	0.27	0.31	0.30	ns
		XC6VLX240T	0.26	0.27	0.31	0.30	ns
		XC6VLX365T	0.28	0.29	0.31	0.31	ns
		XC6VLX550T	N/A	0.50	0.54	0.54	ns
		XC6VLX760	N/A	0.51	0.56	0.56	ns
		XC6VSX315T	0.27	0.28	0.32	0.30	ns
		XC6VSX475T	N/A	0.39	0.44	0.42	ns
		XC6VHX250T	0.25	0.26	0.29	N/A	ns
		XC6VHX255T	0.35	0.37	0.41	N/A	ns
		XC6VHX380T	0.45	0.47	0.52	N/A	ns
		XC6VHX565T	N/A	0.46	0.51	N/A	ns
		XQ6VLX130T	N/A	0.26	0.29	0.28	ns
		XQ6VLX240T	N/A	0.27	0.31	0.30	ns
		XQ6VLX550T	N/A	N/A	0.54	0.54	ns
		XQ6VSX315T	N/A	0.28	0.32	0.30	ns
		XQ6VSX475T	N/A	N/A	0.44	0.42	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.08	0.08	0.08	0.08	ns
T_{BUFIO_SKEW}	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	0.02	ns
T_{BUFIO_SKEW2}	I/O clock tree skew across three clock regions	All	0.10	0.12	0.23	0.12	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	ns

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.