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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	15600
Number of Logic Elements/Cells	199680
Total RAM Bits	12681216
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1156-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vlx195t-1ffg1156c

Table 4: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed and Temperature Grade						Units
			-3 (C)	-2 (C, E, & I)	-1 (C & I)	-1 (I & M) ⁽²⁾	-1L (C)	-1L (I) ⁽¹⁾	
I _{CCOQ}	Quiescent V _{CCO} supply current	XC6VLX75T	1	1	1	N/A	1	1	mA
		XC6VLX130T	1	1	1	N/A	1	1	mA
		XC6VLX195T	1	1	1	N/A	1	1	mA
		XC6VLX240T	2	2	2	N/A	2	2	mA
		XC6VLX365T	2	2	2	N/A	2	2	mA
		XC6VLX550T ⁽³⁾	N/A	3	3	N/A	3	3	mA
		XC6VLX760 ⁽³⁾	N/A	3	3	N/A	3	3	mA
		XC6VSX315T	2	2	2	N/A	2	2	mA
		XC6VSX475T ⁽³⁾	N/A	2	2	N/A	2	2	mA
		XC6VHX250T	1	1	1	N/A	N/A	N/A	mA
		XC6VHX255T	1	1	1	N/A	N/A	N/A	mA
		XC6VHX380T ⁽⁴⁾	2	2	2	N/A	N/A	N/A	mA
		XC6VHX565T ⁽⁵⁾	N/A	2	2	N/A	N/A	N/A	mA
		XQ6VLX130T	N/A	1	N/A	1	N/A	1	mA
		XQ6VLX240T	N/A	2	N/A	2	N/A	2	mA
		XQ6VLX550T ⁽⁷⁾	N/A	N/A	N/A	3	N/A	3	mA
		XQ6VSX315T	N/A	2	N/A	2	N/A	2	mA
		XQ6VSX475T ⁽⁷⁾	N/A	N/A	N/A	2	N/A	2	mA

Table 4: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed and Temperature Grade						Units
			-3 (C)	-2 (C, E, & I)	-1 (C & I)	-1 (I & M) ⁽²⁾	-1L (C)	-1L (I) ⁽¹⁾	
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current	XC6VLX75T	45	45	45	N/A	45	45	mA
		XC6VLX130T	75	75	75	N/A	75	75	mA
		XC6VLX195T	113	113	113	N/A	113	113	mA
		XC6VLX240T	135	135	135	N/A	135	135	mA
		XC6VLX365T	191	191	191	N/A	191	191	mA
		XC6VLX550T ⁽³⁾	N/A	286	286	N/A	286	286	mA
		XC6VLX760 ⁽³⁾	N/A	387	387	N/A	387	387	mA
		XC6VSX315T	186	186	186	N/A	186	186	mA
		XC6VSX475T ⁽³⁾	N/A	279	279	N/A	279	279	mA
		XC6VHX250T	152	152	152	N/A	N/A	N/A	mA
		XC6VHX255T	152	152	152	N/A	N/A	N/A	mA
		XC6VHX380T ⁽⁴⁾	227	227	227	N/A	N/A	N/A	mA
		XC6VHX565T ⁽⁵⁾	N/A	315	315	N/A	N/A	N/A	mA
		XQ6VLX130T ⁽⁶⁾	N/A	75	N/A	75	N/A	75	mA
		XQ6VLX240T ⁽⁶⁾	N/A	135	N/A	135	N/A	135	mA
		XQ6VLX550T ⁽⁷⁾	N/A	N/A	N/A	286	N/A	286	mA
		XQ6VSX315T ⁽⁶⁾	N/A	186	N/A	186	N/A	186	mA
		XQ6VSX475T ⁽⁷⁾	N/A	N/A	N/A	279	N/A	279	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j). -1 and -2 industrial (I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. -1L industrial temperature range devices have the values specified in this column.
2. Use the XPE tool to calculate 125°C values for -1M temperature range devices.
3. The -2E extended temperature range (T_j = 0°C to +100°C) is only available in these devices. The -2I temperature range (T_j = -40°C to +100°C) is available for all other devices except the XC6VHX565T.
4. The XC6VHX380T is available with both -2E and -2I temperature ranges.
5. The XC6VHX565T is only available in the following temperature ranges: -1C, -1I, -2C, and -2E.
6. The XQ6VLX130T, XQ6VLX240T, and XQ6VSX315T are available in -2I, -1I, -1M, and -1LI temperature ranges.
7. The XQ6VLX550T and the XQ6VSX475T are only available in -1I and -1LI temperature ranges.
8. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
9. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPE or XPower Analyzer (XPA) tools.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on sequence and ramp rate of the power supply.

The recommended power-on sequence for Virtex-6 devices is V_{CCINT} , V_{CCAUX} , and V_{CCO} to meet the power-up current requirements listed in Table 5. V_{CCINT} can be powered up or down at any time, but power up current specifications can vary from Table 5. The device will have no physical damage or reliability concerns if V_{CCINT} , V_{CCAUX} , and V_{CCO} sequence cannot be followed.

If the recommended power-up sequence cannot be followed and the I/Os must remain 3-stated throughout configuration, then V_{CCAUX} must be powered prior to V_{CCO} or V_{CCAUX} and V_{CCO} must be powered by the same supply. Similarly, for power-down, the reverse V_{CCAUX} and V_{CCO} sequence is recommended if the I/Os are to remain 3-stated.

The GTH transceiver supplies must be powered using a MGTHAVCC, MGTHAVCCRX, MGTHAVCCPLL, and MGTHAVTT sequence. There are no sequencing requirement for these supplies with respect to the other FPGA supply voltages. For more detail see Table 27: *GTH Transceiver Power Supply Sequencing*. There are no sequencing requirements for the GTX transceivers power supplies.

Table 5 shows the minimum current, in addition to I_{CCQ} , that are required by Virtex-6 devices for proper power-on and configuration. If the current minimums shown in Table 4 and Table 5 are met, the device powers on after all three supplies have passed through their power-on reset threshold voltages. The FPGA must be configured after applying V_{CCINT} , V_{CCAUX} , and V_{CCO} for the appropriate configuration banks. Once initialized and configured, use the XPE tools to estimate current drain on these supplies.

Table 5: Power-On Current for Virtex-6 Devices

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	Units
	Typ ⁽¹⁾	Typ ⁽¹⁾	Typ ⁽¹⁾	
XC6VLX75T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 10$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VLX130T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 10$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VLX195T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VLX240T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VLX365T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VLX550T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VLX760	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VSX315T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VSX475T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 50$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VHX250T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VHX255T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VHX380T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VHX565T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XQ6VLX130T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 100$	$I_{CCOQ} + 30$ mA per bank	mA
XQ6VLX240T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 100$	$I_{CCOQ} + 30$ mA per bank	mA
XQ6VLX550T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 100$	$I_{CCOQ} + 30$ mA per bank	mA
XQ6VSX315T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 100$	$I_{CCOQ} + 40$ mA per bank	mA
XQ6VSX475T	See I_{CCINTQ} in Table 4	$I_{CCAUXQ} + 100$	$I_{CCOQ} + 40$ mA per bank	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Use the XPower Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate maximum power-on currents.

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. [Table 11](#) summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see [UG361: Virtex-6 FPGA SelectIO Resources User Guide](#).

Table 11: LVPECL DC Specifications

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage	$V_{CC} - 1.025$	1.545	$V_{CC} - 0.88$	V
V_{OL}	Output Low Voltage	$V_{CC} - 1.81$	0.795	$V_{CC} - 1.62$	V
V_{ICM}	Input Common-Mode Voltage	0.6	—	2.2	V
V_{IDIFF}	Differential Input Voltage ⁽¹⁾⁽²⁾	0.100	—	1.5	V

Notes:

1. Recommended input maximum voltage not to exceed $V_{CCAUX} + 0.2V$.
2. Recommended input minimum voltage not to go below $-0.5V$.

eFUSE Read Endurance

[Table 12](#) lists the maximum number of read cycle operations expected. For more information, see [UG360: Virtex-6 FPGA Configuration User Guide](#).

Table 12: eFUSE Read Endurance

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

Table 23: GTX Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTXTX}	Serial data rate range		0.480	–	F _{GTXMAX}	Gb/s
T _{RTX}	TX Rise time	20%–80%	–	120	–	ps
T _{FTX}	TX Fall time	80%–20%	–	120	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	350	ps
V _{TXOOBVDPP}	Electrical idle amplitude		–	–	15	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		–	–	75	ns
TJ _{6.5}	Total Jitter ⁽²⁾⁽³⁾	6.5 Gb/s	–	–	0.33	UI
DJ _{6.5}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.17	UI
TJ _{5.0}	Total Jitter ⁽²⁾⁽³⁾	5.0 Gb/s	–	–	0.33	UI
DJ _{5.0}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.15	UI
TJ _{4.25}	Total Jitter ⁽²⁾⁽³⁾	4.25 Gb/s	–	–	0.33	UI
DJ _{4.25}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.14	UI
TJ _{3.75}	Total Jitter ⁽²⁾⁽³⁾	3.75 Gb/s	–	–	0.34	UI
DJ _{3.75}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.16	UI
TJ _{3.125}	Total Jitter ⁽²⁾⁽³⁾	3.125 Gb/s	–	–	0.2	UI
DJ _{3.125}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.1	UI
TJ _{3.125L}	Total Jitter ⁽²⁾⁽³⁾	3.125 Gb/s ⁽⁴⁾	–	–	0.35	UI
DJ _{3.125L}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.16	UI
TJ _{2.5}	Total Jitter ⁽²⁾⁽³⁾	2.5 Gb/s ⁽⁵⁾	–	–	0.20	UI
DJ _{2.5}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.08	UI
TJ _{1.25}	Total Jitter ⁽²⁾⁽³⁾	1.25 Gb/s ⁽⁶⁾	–	–	0.15	UI
DJ _{1.25}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.06	UI
TJ ₆₀₀	Total Jitter ⁽²⁾⁽³⁾	600 Mb/s	–	–	0.1	UI
DJ ₆₀₀	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.03	UI
TJ ₄₈₀	Total Jitter ⁽²⁾⁽³⁾	480 Mb/s	–	–	0.1	UI
DJ ₄₈₀	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
- Using PLL_DIVSEL_FB = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 1e⁻¹².
- PLL frequency at 1.5625 GHz and OUTDIV = 1.
- PLL frequency at 2.5 GHz and OUTDIV = 2.
- PLL frequency at 2.5 GHz and OUTDIV = 4.

GTH Transceiver DC Input and Output Levels

Table 30 summarizes the DC output specifications of the GTH transceivers in Virtex-6 FPGAs. Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further details.

Table 30: GTH Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
D_{VPPIN}	Differential peak-to-peak input voltage	External AC coupled	175	–	1200	mV
D_{VPPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	800	–	1200	mV
R_{IN}	Differential input resistance		80	100	120	Ω
R_{OUT}	Differential output resistance		80	100	120	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	–	ps
C_{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 31 summarizes the DC specifications of the clock input of the GTH transceiver. Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further details.

Table 31: GTH Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	≤ 600 MHz	500	–	1600	mV
		> 600 MHz	600	–	1600	mV
R_{IN}	Differential input resistance		80	100	120	Ω
C_{EXT}	Required external AC coupling capacitor		–	100	–	nF

Table 37: GTH Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
R _{XRL}	Run length (CID)		8000	–	–	UI
R _{XPPMTOL}	Data/REFCLK PPM offset tolerance		–200	–	200	ppm
SJ Jitter Tolerance ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾						
JT_SJ _{11.18}	Sinusoidal Jitter	11.18 Gb/s	0.3	–	–	UI
JT_SJ _{10.32}	Sinusoidal Jitter	10.32 Gb/s	0.3	–	–	UI
JT_SJ _{9.95}	Sinusoidal Jitter	9.95 Gb/s	0.3	–	–	UI
JT_SJ _{2.667}	Sinusoidal Jitter	2.667 Gb/s	0.5	–	–	UI
JT_SJ _{2.48}	Sinusoidal Jitter	2.48 Gb/s	0.5	–	–	UI

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. High-frequency jitter tolerance including 6 db of channel loss at a high frequency of the data rate divided by two.

Ethernet MAC Switching Characteristics

Consult [UG368: Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide](#) for further information.

Table 38: Maximum Ethernet MAC Performance

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1	-1L	
F _{TEMACCLIENT}	Client interface maximum frequency	10 Mb/s – 8-bit width	2.5 ⁽¹⁾	2.5 ⁽¹⁾	2.5 ⁽¹⁾	2.5 ⁽¹⁾	MHz
		100 Mb/s – 8-bit width	25 ⁽²⁾	25 ⁽²⁾	25 ⁽²⁾	25 ⁽²⁾	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		1000 Mb/s – 16-bit width	62.5	62.5	62.5	62.5	MHz
		2000 Mb/s – 16-bit width	125	125	125	N/A	MHz
		2500 Mb/s – 16-bit width	156.25	156.25	156.25	N/A	MHz
F _{TEMACPHY}	Physical interface maximum frequency	10 Mb/s – 4-bit width	2.5	2.5	2.5	2.5	MHz
		100 Mb/s – 4-bit width	25	25	25	25	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		2000 Mb/s – 8-bit width	250	250	250	N/A	MHz
		2500 Mb/s – 8-bit width	312.5	312.5	312.5	N/A	MHz

Notes:

1. When not using clock enable, the F_{MAX} is lowered to 1.25 MHz.
2. When not using clock enable, the F_{MAX} is lowered to 12.5 MHz.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 39: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F _{PIPECLK}	Pipe clock maximum frequency	250	250	250	250	MHz
F _{USERCLK}	User clock maximum frequency	500	500	250	250	MHz
F _{DRPCLK}	DRP clock maximum frequency	250	250	250	250	MHz

System Monitor Analog-to-Digital Converter Specification

Table 40: Analog-to-Digital Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
AV _{DD} = 2.5V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 5.2 MHz, T _j = -55°C to 125°C M-Grade, Typical values at T _j = +35°C						
DC Accuracy: All external input channels. Both unipolar and bipolar modes.						
Resolution			10	—	—	Bits
Integral Nonlinearity	INL		—	—	±1	LSBs
Differential Nonlinearity	DNL	No missing codes (T _{MIN} to T _{MAX}) Guaranteed Monotonic	—	—	±0.9	LSBs
Unipolar Offset Error ⁽¹⁾		Uncalibrated	—	±2	±30	LSBs
Bipolar Offset Error ⁽¹⁾		Uncalibrated measured in bipolar mode	—	±2	±30	LSBs
Gain Error		Uncalibrated - External Reference	—	±0.2	±2	%
		Uncalibrated - Internal Reference	—	±2	—	%
Bipolar Gain Error ⁽¹⁾		Uncalibrated - External Reference	—	±0.2	±2	%
		Uncalibrated - Internal Reference	—	±2	—	%
Total Unadjusted Error (Uncalibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	—	±10	—	LSBs
		Deviation from ideal transfer function. Internal reference	—	±20	—	LSBs
Total Unadjusted Error (Calibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	—	±1	±2	LSBs
Calibrated Gain Temperature Coefficient		Variation of FS code with temperature	—	±0.01	—	LSB/°C
DC Common-Mode Reject	CMRR _{DC}	V _N = V _{CM} = 0.5V ± 0.5V, V _P - V _N = 100mV	—	70	—	dB
Conversion Rate ⁽²⁾						
Conversion Time - Continuous	t _{CONV}	Number of CLK cycles	26	—	32	
Conversion Time - Event	t _{CONV}	Number of CLK cycles	—	—	21	
T/H Acquisition Time	t _{ACQ}	Number of CLK cycles	4	—	—	
DRP Clock Frequency	DCLK	DRP clock frequency	8	—	80	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	—	5.2	MHz
CLK Duty cycle			40	—	60	%

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDCI_DV2_25	0.51	0.57	0.66	0.70	1.71	1.83	2.01	2.00	1.71	1.83	2.01	2.00	ns
LVDCI_DV2_18	0.55	0.61	0.71	0.73	1.69	1.81	2.00	1.98	1.69	1.81	2.00	1.98	ns
LVDCI_DV2_15	0.64	0.73	0.85	0.85	1.68	1.77	1.91	1.98	1.68	1.77	1.91	1.98	ns
LVPECL_25	0.85	0.94	1.09	1.08	1.38	1.49	1.65	1.64	1.38	1.49	1.65	1.64	ns
HSTL_I_12	0.81	0.91	1.06	1.06	1.48	1.60	1.78	1.74	1.48	1.60	1.78	1.74	ns
HSTL_I_DCI	0.81	0.91	1.06	1.06	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
HSTL_II_DCI	0.81	0.91	1.06	1.06	1.37	1.49	1.68	1.66	1.37	1.49	1.68	1.66	ns
HSTL_II_T_DCI	0.81	0.91	1.06	1.06	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
HSTL_III_DCI	0.81	0.91	1.06	1.06	1.34	1.45	1.62	1.61	1.34	1.45	1.62	1.61	ns
HSTL_I_DCI_18	0.81	0.91	1.06	1.06	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
HSTL_II_DCI_18	0.81	0.91	1.06	1.06	1.36	1.46	1.62	1.59	1.36	1.46	1.62	1.59	ns
HSTL_II_T_DCI_18	0.81	0.91	1.06	1.06	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
HSTL_III_DCI_18	0.81	0.91	1.06	1.06	1.43	1.54	1.69	1.67	1.43	1.54	1.69	1.67	ns
DIFF_HSTL_I_18	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
DIFF_HSTL_I_DCI_18	0.85	0.94	1.09	1.08	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
DIFF_HSTL_I	0.85	0.94	1.09	1.08	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns
DIFF_HSTL_I_DCI	0.85	0.94	1.09	1.08	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
DIFF_HSTL_II_18	0.85	0.94	1.09	1.08	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
DIFF_HSTL_II_DCI_18	0.85	0.94	1.09	1.08	1.36	1.46	1.62	1.59	1.36	1.46	1.62	1.59	ns
DIFF_HSTL_II_T_DCI_18	0.85	0.94	1.09	1.08	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
DIFF_HSTL_II	0.85	0.94	1.09	1.08	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
DIFF_HSTL_II_DCI	0.85	0.94	1.09	1.08	1.37	1.49	1.68	1.66	1.37	1.49	1.68	1.66	ns
SSTL2_I_DCI	0.81	0.91	1.06	1.06	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
SSTL2_II_DCI	0.81	0.91	1.06	1.06	1.39	1.50	1.67	1.69	1.39	1.50	1.67	1.69	ns
SSTL2_II_T_DCI	0.81	0.91	1.06	1.06	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
SSTL18_I	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
SSTL18_II	0.81	0.91	1.06	1.06	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
SSTL18_I_DCI	0.81	0.91	1.06	1.06	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
SSTL18_II_DCI	0.81	0.91	1.06	1.06	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
SSTL18_II_T_DCI	0.81	0.91	1.06	1.06	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL2_I	0.85	0.94	1.09	1.08	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
DIFF_SSTL2_I_DCI	0.85	0.94	1.09	1.08	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
DIFF_SSTL2_II	0.85	0.94	1.09	1.08	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
DIFF_SSTL2_II_DCI	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.69	1.39	1.50	1.67	1.69	ns
DIFF_SSTL2_II_T_DCI	0.85	0.94	1.09	1.08	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVC MOS25, Fast, 16 mA	0.57	0.66	0.70	1.92	2.15	2.08	1.92	2.15	2.08	ns
LVC MOS25, Fast, 24 mA	0.57	0.66	0.70	1.79	2.15	1.96	1.79	2.15	1.96	ns
LVC MOS18, Slow, 2 mA	0.61	0.71	0.73	4.47	4.87	4.30	4.47	4.87	4.30	ns
LVC MOS18, Slow, 4 mA	0.61	0.71	0.73	2.96	3.21	2.94	2.96	3.21	2.94	ns
LVC MOS18, Slow, 6 mA	0.61	0.71	0.73	2.43	2.64	2.47	2.43	2.64	2.47	ns
LVC MOS18, Slow, 8 mA	0.61	0.71	0.73	2.11	2.41	2.24	2.11	2.41	2.24	ns
LVC MOS18, Slow, 12 mA	0.61	0.71	0.73	1.99	2.30	2.10	1.99	2.30	2.10	ns
LVC MOS18, Slow, 16 mA	0.61	0.71	0.73	1.95	2.30	2.04	1.95	2.30	2.04	ns
LVC MOS18, Fast, 2 mA	0.61	0.71	0.73	4.23	4.57	4.08	4.23	4.57	4.08	ns
LVC MOS18, Fast, 4 mA	0.61	0.71	0.73	2.76	2.97	2.74	2.76	2.97	2.74	ns
LVC MOS18, Fast, 6 mA	0.61	0.71	0.73	2.28	2.46	2.32	2.28	2.46	2.32	ns
LVC MOS18, Fast, 8 mA	0.61	0.71	0.73	1.99	2.34	2.14	1.99	2.34	2.14	ns
LVC MOS18, Fast, 12 mA	0.61	0.71	0.73	1.80	2.19	1.88	1.80	2.19	1.88	ns
LVC MOS18, Fast, 16 mA	0.61	0.71	0.73	1.74	2.18	1.88	1.74	2.18	1.88	ns
LVC MOS15, Slow, 2 mA	0.73	0.85	0.85	3.77	4.29	3.91	3.77	4.29	3.91	ns
LVC MOS15, Slow, 4 mA	0.73	0.85	0.85	2.79	3.10	2.93	2.79	3.10	2.93	ns
LVC MOS15, Slow, 6 mA	0.73	0.85	0.85	2.32	2.68	2.50	2.32	2.68	2.50	ns
LVC MOS15, Slow, 8 mA	0.73	0.85	0.85	1.98	2.29	2.24	1.98	2.29	2.24	ns
LVC MOS15, Slow, 12 mA	0.73	0.85	0.85	1.91	2.23	2.07	1.91	2.23	2.07	ns
LVC MOS15, Slow, 16 mA	0.73	0.85	0.85	1.83	2.23	1.98	1.83	2.23	1.98	ns
LVC MOS15, Fast, 2 mA	0.73	0.85	0.85	3.77	4.28	3.91	3.77	4.28	3.91	ns
LVC MOS15, Fast, 4 mA	0.73	0.85	0.85	2.53	2.78	2.66	2.53	2.78	2.66	ns
LVC MOS15, Fast, 6 mA	0.73	0.85	0.85	2.05	2.42	2.16	2.05	2.42	2.16	ns
LVC MOS15, Fast, 8 mA	0.73	0.85	0.85	1.90	2.20	2.04	1.90	2.20	2.04	ns
LVC MOS15, Fast, 12 mA	0.73	0.85	0.85	1.77	2.11	1.90	1.77	2.11	1.90	ns
LVC MOS15, Fast, 16 mA	0.73	0.85	0.85	1.76	2.11	1.92	1.76	2.11	1.92	ns
LVC MOS12, Slow, 2 mA	0.81	0.93	0.95	3.39	3.75	3.54	3.39	3.75	3.54	ns
LVC MOS12, Slow, 4 mA	0.81	0.93	0.95	2.63	2.93	2.79	2.63	2.93	2.79	ns
LVC MOS12, Slow, 6 mA	0.81	0.93	0.95	2.11	2.67	2.26	2.11	2.67	2.26	ns
LVC MOS12, Slow, 8 mA	0.81	0.93	0.95	2.02	2.25	2.17	2.02	2.25	2.17	ns
LVC MOS12, Fast, 2 mA	0.81	0.93	0.95	2.98	3.39	3.11	2.98	3.39	3.11	ns
LVC MOS12, Fast, 4 mA	0.81	0.93	0.95	2.16	2.70	2.31	2.16	2.70	2.31	ns
LVC MOS12, Fast, 6 mA	0.81	0.93	0.95	1.89	2.34	2.05	1.89	2.34	2.05	ns
LVC MOS12, Fast, 8 mA	0.81	0.93	0.95	1.82	2.10	1.98	1.82	2.10	1.98	ns
LVDCI_25	0.57	0.70	0.70	2.14	2.82	2.26	2.14	2.82	2.26	ns
LVDCI_18	0.61	0.71	0.73	2.23	2.78	2.38	2.23	2.78	2.38	ns
LVDCI_15	0.73	0.85	0.85	2.01	2.75	2.18	2.01	2.75	2.18	ns
LVDCI_DV2_25	0.57	0.70	0.70	1.83	2.37	2.00	1.83	2.37	2.00	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPi}			T _{IOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
DIFF_SSTL18_II	0.94	1.09	1.08	1.50	2.27	1.66	1.50	2.27	1.66	ns
DIFF_SSTL18_II_DCI	0.94	1.09	1.08	1.47	2.20	1.62	1.47	2.20	1.62	ns
DIFF_SSTL18_II_T_DCI	0.94	1.09	1.08	1.51	2.30	1.65	1.51	2.30	1.65	ns
DIFF_SSTL15	0.91	1.06	1.06	1.54	2.25	1.69	1.54	2.25	1.69	ns
DIFF_SSTL15_DCI	0.91	1.06	1.06	1.52	2.25	1.66	1.52	2.25	1.66	ns
DIFF_SSTL15_T_DCI	0.91	1.06	1.06	1.52	2.25	1.66	1.52	2.25	1.66	ns

Table 46: IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T _{IOTPHZ}	T input to Pad high-impedance	0.86	0.92	0.99	0.99	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 47 shows the test setup parameters used for measuring input delay.

Table 47: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)(2)}$	$V_H^{(1)(2)}$	$V_{MEAS}^{(1)(4)(5)}$	$V_{REF}^{(1)(3)(5)}$
LVC MOS, 2.5V	LVC MOS25	0	2.5	1.25	—
LVC MOS, 1.8V	LVC MOS18	0	1.8	0.9	—
LVC MOS, 1.5V	LVC MOS15	0	1.5	0.75	—
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL, Class III	HSTL_III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	$V_{REF} - 1.00$	$V_{REF} + 1.00$	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	$1.2 - 0.125$	$1.2 + 0.125$	$0^{(6)}$	—
LVDS EXT (LVDS Extended Mode), 2.5V	LVDS EXT_25	$1.2 - 0.125$	$1.2 + 0.125$	$0^{(6)}$	—
HT (HyperTransport), 2.5V	LDT_25	$0.6 - 0.125$	$0.6 + 0.125$	$0^{(6)}$	—

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVC MOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H .
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 6.
6. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 6 and Figure 7.

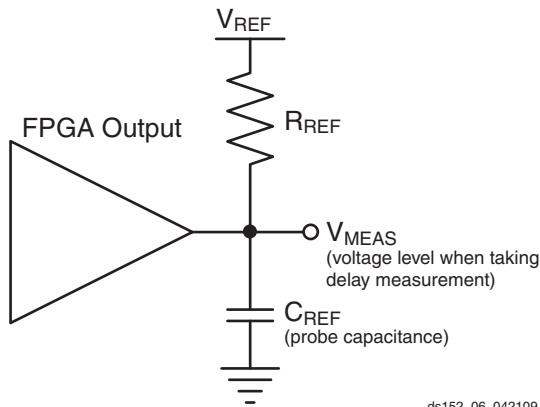
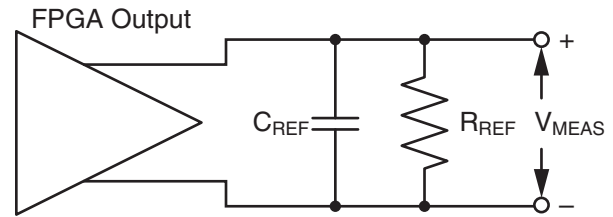


Figure 6: Single Ended Test Setup



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Figure 7: Differential Test Setup

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 48.
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 48: Output Delay Measurement Methodology

Description	I/O Standard Attribute	R_{REF} (Ω)	$C_{REF}^{(1)}$ (pF)	V_{MEAS} (V)	V_{REF} (V)
LVC MOS, 2.5V	LVC MOS25	1M	0	1.25	0
LVC MOS, 1.8V	LVC MOS18	1M	0	0.9	0
LVC MOS, 1.5V	LVC MOS15	1M	0	0.75	0
LVC MOS, 1.2V	LVC MOS12	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	100	0	0 ⁽²⁾	1.2
LVDS EXT (LVDS Extended Mode), 2.5V	LVDS_25	100	0	0 ⁽²⁾	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0 ⁽²⁾	0

Table 54: CLB Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T _{ITO}	An – Dn inputs to A – D Q outputs	0.59	0.67	0.79	0.85	ns, Max
T _{AXA}	AX inputs to AMUX output	0.31	0.35	0.42	0.44	ns, Max
T _{AXB}	AX inputs to BMUX output	0.35	0.39	0.47	0.50	ns, Max
T _{AXC}	AX inputs to CMUX output	0.39	0.44	0.52	0.56	ns, Max
T _{AXD}	AX inputs to DMUX output	0.42	0.47	0.55	0.60	ns, Max
T _{BXB}	BX inputs to BMUX output	0.30	0.34	0.39	0.44	ns, Max
T _{BXD}	BX inputs to DMUX output	0.38	0.43	0.50	0.55	ns, Max
T _{CXC}	CX inputs to CMUX output	0.26	0.29	0.34	0.37	ns, Max
T _{CXD}	CX inputs to DMUX output	0.30	0.34	0.40	0.44	ns, Max
T _{DXD}	DX inputs to DMUX output	0.30	0.33	0.38	0.43	ns, Max
T _{OPCYA}	An input to COUT output	0.32	0.36	0.41	0.47	ns, Max
T _{OPCYB}	Bn input to COUT output	0.32	0.36	0.41	0.47	ns, Max
T _{OPCYC}	Cn input to COUT output	0.27	0.30	0.34	0.40	ns, Max
T _{OPCYD}	Dn input to COUT output	0.25	0.28	0.32	0.37	ns, Max
T _{AXCY}	AX input to COUT output	0.25	0.28	0.33	0.36	ns, Max
T _{BXCY}	BX input to COUT output	0.22	0.24	0.28	0.31	ns, Max
T _{CXCY}	CX input to COUT output	0.15	0.17	0.20	0.22	ns, Max
T _{DXCY}	DX input to COUT output	0.14	0.16	0.19	0.21	ns, Max
T _{BYP}	CIN input to COUT output	0.06	0.07	0.08	0.09	ns, Max
T _{CINA}	CIN input to AMUX output	0.21	0.24	0.28	0.30	ns, Max
T _{CINB}	CIN input to BMUX output	0.23	0.25	0.29	0.31	ns, Max
T _{CINC}	CIN input to CMUX output	0.23	0.26	0.30	0.33	ns, Max
T _{CIND}	CIN input to DMUX output	0.25	0.29	0.33	0.36	ns, Max
Sequential Delays						
T _{CKO}	Clock to AQ – DQ outputs	0.29	0.33	0.39	0.44	ns, Max
T _{SHCKO}	Clock to AMUX – DMUX outputs	0.36	0.40	0.47	0.53	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T _{DICK} /T _{CKDI}	A – D input to CLK on A – D Flip Flops	0.30/0.17	0.36/0.18	0.43/0.20	0.44/0.25	ns, Min
T _{CECK_CLB} / T _{CKCE_CLB}	CE input to CLK on A – D Flip Flops	0.20/0.00	0.25/0.00	0.32/0.00	0.32/0.01	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D Flip Flops	0.39/–0.07	0.44/–0.07	0.52/–0.07	0.58/–0.08	ns, Min
T _{CINCK} /T _{CKCIN}	CIN input to CLK on A – D Flip Flops	0.16/0.12	0.19/0.14	0.24/0.16	0.23/0.22	ns, Min
Set/Reset						
T _{SRMIN}	SR input minimum pulse width	0.90	0.90	0.97	0.80	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops	0.52	0.58	0.68	0.77	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops	0.41	0.48	0.59	0.61	ns, Max
F _{TOG}	Toggle frequency (for export control)	1412.00	1286.40	1098.00	1098.00	MHz

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

Table 59: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T _{SMCKBY}	CCLK to BUSY out in readback at 2.5V	6	6	6	7	ns, Max
	CCLK to BUSY out in readback at 1.8V	6	6	6	7	ns, Max
F _{SMCK}	Maximum Frequency with respect to nominal CCLK	100	100	100	70	MHz, Max
F _{RBCK}	Maximum Readback Frequency with respect to nominal CCLK	100	100	100	60	MHz, Max
F _{MCCKTOL}	Frequency tolerance, master mode with respect to nominal CCLK	55	55	55	60	%
Boundary-Scan Port Timing Specifications						
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI Setup time before TCK/ Hold time after TCK	3.0/2.0	3.0/2.0	3.0/2.0	4.0/2.0	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output valid at 2.5V	6	6	6	7	ns, Max
	TCK falling edge to TDO output valid at 1.8V	6	6	6	7	ns, Max
F _{TCK}	Maximum configuration TCK clock frequency	66	66	66	33	MHz, Max
F _{TCKB_MIN}	Minimum boundary-scan TCK clock frequency when using IEEE Std 1149.6 (AC-JTAG). Minimum operating temperature for IEEE Std 1149.6 is 0°C.	15	15	15	15	MHz, Min
F _{TCKB}	Maximum boundary-scan TCK clock frequency	66	66	66	33	MHz, Max
BPI Master Flash Mode Programming Switching						
T _{BPICCO} ⁽²⁾	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 2.5V	6	6	6	7	ns
	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 1.8V	6	6	6	7	ns
T _{BPIDCC} /T _{BPICCD}	Setup/Hold on D[15:0] data input pins	4.0/0.0	4.0/0.0	4.0/0.0	5.0/0.0	ns
T _{INITADDR}	Minimum period of initial ADDR[25:0] address cycles	3	3	3	3	CCLK cycles
SPI Master Flash Mode Programming Switching						
T _{SPIDCC} /T _{SPIDCCD}	DIN Setup/Hold before/after the rising CCLK edge	3.0/0.0	3.0/0.0	3.0/0.0	3.5/0.0	ns
T _{SPICCM}	MOSI clock to out at 2.5V	6	6	6	7	ns
	MOSI clock to out at 1.8V	6	6	6	7	ns
T _{SPICFC}	FCS_B clock to out at 2.5V	6	6	6	7	ns
	FCS_B clock to out at 1.8V	6	6	6	7	ns
T _{FSINIT} /T _{FSINITH}	FS[2:0] to INIT_B rising edge Setup and Hold	2	2	2	2	μs
CCLK Output (Master Modes)						
T _{MCCKL}	Master CCLK clock Low time duty cycle	45/55	45/55	45/55	40/60	%, Min/Max
T _{MCCKH}	Master CCLK clock High time duty cycle	45/55	45/55	45/55	40/60	%, Min/Max
CCLK Input (Slave Modes)						
T _{SCCKL}	Slave CCLK clock minimum Low time	2.5	2.5	2.5	2.5	ns, Min
T _{SCCKH}	Slave CCLK clock minimum High time	2.5	2.5	2.5	2.5	ns, Min
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
F _{DCK}	Maximum frequency for DCLK	200	200	200	200	MHz
T _{MMCMCDCK_DADDR} / T _{MMCMCKD_DADDR}	DADDR Setup/Hold	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns

Table 62: Regional Clock Switching Characteristics (BUFR) (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BRDO_O}	Propagation delay from CLR to O	0.69	0.74	0.80	1.12	ns
Maximum Frequency						
$F_{MAX}^{(1)}$	Regional clock tree (BUFR)	500	420	300	300	MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

Table 63: Horizontal Clock Buffer Switching Characteristics (BUFH)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	0.15	ns
T_{BHCK_CE}/T_{BHCK_CE}	CE pin Setup and Hold	0.04/ 0.04	0.04/ 0.04	0.05/ 0.05	0.04/ 0.04	ns
Maximum Frequency						
F_{MAX}	Horizontal clock buffer (BUFH)	800	750	700	667	MHz

MMCM Switching Characteristics

Table 64: MMCM Specification

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F_{INMAX}	Maximum Input Clock Frequency ⁽¹⁾	800	750	700	700	MHz
F_{INMIN}	Minimum Input Clock Frequency	10	10	10	10	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
$F_{INDUTY}^{(2)}$	Allowable Input Duty Cycle: 10—49 MHz	25/75				%
	Allowable Input Duty Cycle: 50—199 MHz	30/70				%
	Allowable Input Duty Cycle: 200—399 MHz	35/65				%
	Allowable Input Duty Cycle: 400—499 MHz	40/60				%
	Allowable Input Duty Cycle: >500 MHz	45/55				%
F_{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	0.01	0.01	MHz
F_{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	550	500	450	450	MHz
F_{VCOMIN}	Minimum MMCM VCO Frequency	600	600	600	600	MHz
F_{VCOMAX}	Maximum MMCM VCO Frequency	1600	1440	1200	1200	MHz
$F_{BANDWIDTH}$	Low MMCM Bandwidth at Typical ⁽³⁾	1.00	1.00	1.00	1.00	MHz
	High MMCM Bandwidth at Typical ⁽³⁾	4.00	4.00	4.00	4.00	MHz
$T_{STATPHAOFFSET}$	Static Phase Offset of the MMCM Outputs ⁽⁴⁾	0.12	0.12	0.12	0.12	ns
$T_{OUTJITTER}$	MMCM Output Jitter ⁽⁵⁾	Note 3				
$T_{OUTDUTY}$	MMCM Output Clock Duty Cycle Precision ⁽⁶⁾	0.15	0.20	0.20	0.20	ns
$T_{LOCKMAX}$	MMCM Maximum Lock Time	100	100	100	100	μs
F_{OUTMAX}	MMCM Maximum Output Frequency	800	750	700	700	MHz
F_{OUTMIN}	MMCM Minimum Output Frequency ⁽⁷⁾⁽⁸⁾	4.69	4.69	4.69	4.69	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				

Table 64: MMCM Specification (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
RST _{MINPULSE}	Minimum Reset Pulse Width	1.5	1.5	1.5	1.5	ns
F _{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized ⁽⁹⁾	550	500	450	450	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300	300	300	300	MHz
F _{PFDMIN}	Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	135	135	135	135	MHz
	Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	10	10	10	10	MHz
T _{FBDELAY}	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				
T _{MMCMCK_PSEN} / T _{MMCMCKD_PSEN}	Setup and Hold of Phase Shift Enable	1.04 0.00	1.04 0.00	1.04 0.00	1.04 0.00	ns
T _{MMCMCK_PINCDEC} / T _{MMCMCKD_PINCDEC}	Setup and Hold of Phase Shift Increment/Decrement	1.04 0.00	1.04 0.00	1.04 0.00	1.04 0.00	ns
T _{MMCMCKO_PSDONE}	Phase Shift Clock-to-Out of PSDONE	0.32	0.34	0.38	0.38	ns

Notes:

1. When DIVCLK_DIVIDE = 3 or 4, F_{INMAX} is 315 MHz.
2. This duty cycle specification does not apply to the GTH_QUAD (GTH) to MMCM connection. The GTH transceivers drive the MMCMs at the following maximum frequencies: 323 MHz for -1 speed grade devices, 350 MHz for -2 speed grade devices, or 350 MHz for -3 speed grade devices.
3. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. The static offset is measured between any MMCM outputs with identical phase.
5. Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
6. Includes global clock buffer.
7. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
8. When CASCADE4_OUT = TRUE, F_{OUTMIN} is 0.036 MHz.
9. In ISE software 12.3 (or earlier versions supporting the Virtex-6 family), the phase frequency detector Optimized bandwidth setting is equivalent to the High bandwidth setting. Starting with ISE software 12.4, the Optimized bandwidth setting is automatically adjusted to Low when the software can determine that the phase frequency detector input is less than 135 MHz.

Virtex-6 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 68. Values are expressed in nanoseconds unless otherwise noted.

Table 68: Global Clock Input Setup and Hold Without MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. ⁽¹⁾							
T _{PSFD} / T _{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF ⁽²⁾ without MMCM	XC6VLX75T	1.33/ 0.03	1.44/ 0.03	1.75/ 0.03	2.18/ −0.22	ns
		XC6VLX130T	1.31/ −0.08	1.54/ −0.08	1.88/ −0.08	2.31/ −0.12	ns
		XC6VLX195T	1.36/ −0.11	1.60/ −0.11	1.97/ −0.11	2.40/ −0.25	ns
		XC6VLX240T	1.36/ −0.11	1.60/ −0.11	1.97/ −0.11	2.40/ −0.25	ns
		XC6VLX365T	1.79/ −0.28	1.87/ −0.28	2.17/ −0.28	2.48/ −0.24	ns
		XC6VLX550T	N/A	2.22/ −0.12	2.36/ −0.12	2.77/ −0.26	ns
		XC6VLX760	N/A	2.19/ −0.24	2.35/ −0.24	2.71/ −0.21	ns
		XC6VSX315T	1.75/ −0.09	1.85/ −0.09	2.06/ −0.09	2.47/ −0.24	ns
		XC6VSX475T	N/A	2.14/ −0.14	2.31/ −0.14	2.71/ −0.30	ns
		XC6VHX250T	1.93/ −0.22	2.04/ −0.22	2.25/ −0.22	N/A	ns
		XC6VHX255T	1.81/ −0.33	2.11/ −0.33	2.56/ −0.33	N/A	ns
		XC6VHX380T	1.93/ −0.11	2.04/ −0.11	2.25/ −0.11	N/A	ns
		XC6VHX565T	N/A	2.20/ −0.12	2.39/ −0.12	N/A	ns
		XQ6VLX130T	N/A	1.54/ −0.08	1.88/ −0.08	2.31/ −0.12	ns
		XQ6VLX240T	N/A	1.60/ −0.11	1.97/ −0.11	2.40/ −0.25	ns
		XQ6VLX550T	N/A	N/A	2.36/ −0.12	2.77/ −0.26	ns
		XQ6VSX315T	N/A	1.85/ −0.09	2.06/ −0.09	2.47/ −0.24	ns
		XQ6VSX475T	N/A	N/A	2.31/ −0.14	2.71/ −0.30	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch
- A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 FPGA clock transmitter and receiver data-valid windows.

Table 71: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion ⁽¹⁾	All	0.12	0.12	0.12	0.12	ns
T_{CKSKEW}	Global Clock Tree Skew ⁽²⁾	XC6VLX75T	0.15	0.16	0.18	0.17	ns
		XC6VLX130T	0.25	0.26	0.29	0.28	ns
		XC6VLX195T	0.26	0.27	0.31	0.30	ns
		XC6VLX240T	0.26	0.27	0.31	0.30	ns
		XC6VLX365T	0.28	0.29	0.31	0.31	ns
		XC6VLX550T	N/A	0.50	0.54	0.54	ns
		XC6VLX760	N/A	0.51	0.56	0.56	ns
		XC6VSX315T	0.27	0.28	0.32	0.30	ns
		XC6VSX475T	N/A	0.39	0.44	0.42	ns
		XC6VHX250T	0.25	0.26	0.29	N/A	ns
		XC6VHX255T	0.35	0.37	0.41	N/A	ns
		XC6VHX380T	0.45	0.47	0.52	N/A	ns
		XC6VHX565T	N/A	0.46	0.51	N/A	ns
		XQ6VLX130T	N/A	0.26	0.29	0.28	ns
		XQ6VLX240T	N/A	0.27	0.31	0.30	ns
		XQ6VLX550T	N/A	N/A	0.54	0.54	ns
		XQ6VSX315T	N/A	0.28	0.32	0.30	ns
		XQ6VSX475T	N/A	N/A	0.44	0.42	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.08	0.08	0.08	0.08	ns
T_{BUFIO_SKEW}	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	0.02	ns
T_{BUFIO_SKEW2}	I/O clock tree skew across three clock regions	All	0.10	0.12	0.23	0.12	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	ns

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Date	Version	Description of Revisions
01/18/10	2.1	Changed absolute maximum ratings for both V_{IN} and V_{TS} in Table 1 . Added data to Table 3 . Added data to Table 5 . Updated SSTL15 in Table 7 . Updated V_{OCM} and V_{OD} values in Table 8 . Added eFUSE endurance Table 12 . Added values to $V_{MGTREFCLK}$ and V_{IN} in Table 13 , page 11 . Added values and updated tables in the GTX Transceiver Specifications and GTH Transceiver Specifications sections. Added Table 27 and Figure 4 . Revised parameters and values in Table 39 . Updated Table 40 , page 23 . Added data to Table 41 . Updated speed specification to v1.04 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX240T for -1 and -2 speed grades. Speed specification changes and numerous updates also made to Table 44 , and Table 49 through Table 71 . Added data to Table 73 and Table 74 .
02/09/10	2.2	Revised description of C_{IN} in Table 3 . Clarified values in Table 5 . Fixed SDR LVDS unit error in Table 41 .
04/12/10	2.3	Added note 3 and update value of n in Table 3 . Clarified simultaneous power-down in Power-On Power Supply Requirements . Updated external reference junction temperatures in Table 40 , Analog-to-Digital Specifications . Updated speed specification to v1.05 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX130T for -1 and -2 speed grades. Fixed note 4 in Table 48 . Increased the -2 specification for $F_{IDELAYCTRL_REF}$ and clarified units for $T_{IDELAYPAT_JIT}$ in Table 53 . Added note 1 to Table 62 .
05/11/10	2.4	Updated F_{RXREC} in Table 22 . Revised $F_{IDELAYCTRL_REF}$ in Table 53 . Removed $T_{RCKO_PARITY_ECC}$: Clock CLK to ECCPARITY in standard ECC mode row in Table 57 . Added XC6VLX130T values to Table 72 .
05/26/10	2.5	Added XC6VLX195T data to Table 5 . Updated values in Table 22 including adding note 2 and note 3. Updated speed specification to v1.06 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX195T for -1 and -2 speed grades. Added XC6VLX195T values to Table 72 .
07/16/10	2.6	Changed Table 42 and Table 43 to production status on the -3 speed grade XC6VLX130T, XC6VLX195T, and XC6VLX240T devices. Added XC6VHX250T data to Table 4 and Table 72 . Added Note 6 to Table 64 .
07/23/10	2.7	Changed Table 42 and Table 43 to production status on the XC6VLX75T, XC6VLX365T, XC6VLX550T, XC6VLX760, XC6VSX315T, and XC6VSX475T devices using ISE 12.2 software with speed specification v1.08. Updated $V_{CMOUTDC}$ equation to $MGTAVTT - D_{VPPOUT}/4$ in Table 17 . Updated some -3, -2, -1 specifications in Table 65 through Table 72 . Added and updated -1L specifications to Table 41 and for most switching characteristics tables.
07/30/10	2.8	Changed Table 42 and Table 43 to production status on the -1L speed grade for the XC6VLX130T, XC6VLX195T, XC6VLX240T, XC6VLX365T, and XC6VLX550T devices using ISE 12.2 software with current speed specifications. Also updated the speed specifications for XC6VLX75T, XC6VLX550T, and XC6VSX315T. Updated V_{CCINT} specifications for -1L speed grade industrial temperature range devices in Table 2 .
09/20/10	2.9	In Table 32 , changed $F_{GPLLMAX}$ specification in -3 column from 5.951 to 5.591. In Table 40 , changed F_{MAX} for the DCLK from 250 MHz to 80 MHz.
10/18/10	2.10	The specification change in version 2.9, Table 40 is described in XCN10032 , <i>Virtex-6 FPGA: GTX Transceiver User Guide, Family Data Sheet (SYSMON DCLK), and JTAG ID Changes</i> . In this version (2.10), -1L(I) data is added to Table 4 and clarified in Note 2. Changed Table 42 and Table 43 to production status on the -1L speed grade XC6VLX75T, XC6VLX760, XC6VSX315T, and XC6VSX475T devices using ISE 12.3 software with current speed specifications. Revised the XC6VLX760 -1L speed specification for $T_{PHMMCMGC}$ in Table 69 and $T_{PHMMCMCC}$ in Table 70 .
01/17/11	2.11	Changed in Table 42 and Table 43 to production status on the XC6VHX250T devices using ISE 12.4 software with current speed specifications. Added industrial temperature range (T_I) recommended specifications to Table 2 ; including specific ranges for the -2I XC6VSX475T, XC6VLX550T, XC6VLX760, and XC6VHX565T devices. Added note 3 to Table 36 and maximum total jitter values. Added note 4 to Table 37 and maximum sinusoidal jitter values. Added note 2 to Table 43 . Revised F_{MAX} descriptions in Table 57 and added note 12. Added note 8 to F_{PFDMIN} in Table 64 . The following revisions are due to specification changes as described in XCN11009 , <i>Virtex-6 FPGA: Data Sheet, User Guides, and JTAG ID Updates</i> . In Table 59: Configuration Switching Characteristics , page 49 , revised -1L specifications for T_{POR} , F_{MCKK} , $F_{MCKKTOL}$, T_{SMCCKK} , T_{SMCKKW} , F_{RBCKK} , F_{TCK} , F_{TCKB} , T_{MCKKL} , and T_{MCKKH} . In Table 64: MMCM Specification , added bandwidth settings to F_{PFDMIN} and added note 1.