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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	15600
Number of Logic Elements/Cells	199680
Total RAM Bits	12681216
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1156-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vlx195t-1ffg1156i

Table 4: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed and Temperature Grade						Units
			-3 (C)	-2 (C, E, & I)	-1 (C & I)	-1 (I & M) ⁽²⁾	-1L (C)	-1L (I) ⁽¹⁾	
I _{CCOQ}	Quiescent V _{CCO} supply current	XC6VLX75T	1	1	1	N/A	1	1	mA
		XC6VLX130T	1	1	1	N/A	1	1	mA
		XC6VLX195T	1	1	1	N/A	1	1	mA
		XC6VLX240T	2	2	2	N/A	2	2	mA
		XC6VLX365T	2	2	2	N/A	2	2	mA
		XC6VLX550T ⁽³⁾	N/A	3	3	N/A	3	3	mA
		XC6VLX760 ⁽³⁾	N/A	3	3	N/A	3	3	mA
		XC6VSX315T	2	2	2	N/A	2	2	mA
		XC6VSX475T ⁽³⁾	N/A	2	2	N/A	2	2	mA
		XC6VHX250T	1	1	1	N/A	N/A	N/A	mA
		XC6VHX255T	1	1	1	N/A	N/A	N/A	mA
		XC6VHX380T ⁽⁴⁾	2	2	2	N/A	N/A	N/A	mA
		XC6VHX565T ⁽⁵⁾	N/A	2	2	N/A	N/A	N/A	mA
		XQ6VLX130T	N/A	1	N/A	1	N/A	1	mA
		XQ6VLX240T	N/A	2	N/A	2	N/A	2	mA
		XQ6VLX550T ⁽⁷⁾	N/A	N/A	N/A	3	N/A	3	mA
		XQ6VSX315T	N/A	2	N/A	2	N/A	2	mA
		XQ6VSX475T ⁽⁷⁾	N/A	N/A	N/A	2	N/A	2	mA

Table 4: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed and Temperature Grade						Units
			-3 (C)	-2 (C, E, & I)	-1 (C & I)	-1 (I & M) ⁽²⁾	-1L (C)	-1L (I) ⁽¹⁾	
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current	XC6VLX75T	45	45	45	N/A	45	45	mA
		XC6VLX130T	75	75	75	N/A	75	75	mA
		XC6VLX195T	113	113	113	N/A	113	113	mA
		XC6VLX240T	135	135	135	N/A	135	135	mA
		XC6VLX365T	191	191	191	N/A	191	191	mA
		XC6VLX550T ⁽³⁾	N/A	286	286	N/A	286	286	mA
		XC6VLX760 ⁽³⁾	N/A	387	387	N/A	387	387	mA
		XC6VSX315T	186	186	186	N/A	186	186	mA
		XC6VSX475T ⁽³⁾	N/A	279	279	N/A	279	279	mA
		XC6VHX250T	152	152	152	N/A	N/A	N/A	mA
		XC6VHX255T	152	152	152	N/A	N/A	N/A	mA
		XC6VHX380T ⁽⁴⁾	227	227	227	N/A	N/A	N/A	mA
		XC6VHX565T ⁽⁵⁾	N/A	315	315	N/A	N/A	N/A	mA
		XQ6VLX130T ⁽⁶⁾	N/A	75	N/A	75	N/A	75	mA
		XQ6VLX240T ⁽⁶⁾	N/A	135	N/A	135	N/A	135	mA
		XQ6VLX550T ⁽⁷⁾	N/A	N/A	N/A	286	N/A	286	mA
		XQ6VSX315T ⁽⁶⁾	N/A	186	N/A	186	N/A	186	mA
		XQ6VSX475T ⁽⁷⁾	N/A	N/A	N/A	279	N/A	279	mA

Notes:

- Typical values are specified at nominal voltage, 85°C junction temperatures (T_j). -1 and -2 industrial (I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. -1L industrial temperature range devices have the values specified in this column.
- Use the XPE tool to calculate 125°C values for -1M temperature range devices.
- The -2E extended temperature range (T_j = 0°C to +100°C) is only available in these devices. The -2I temperature range (T_j = -40°C to +100°C) is available for all other devices except the XC6VHX565T.
- The XC6VHX380T is available with both -2E and -2I temperature ranges.
- The XC6VHX565T is only available in the following temperature ranges: -1C, -1I, -2C, and -2E.
- The XQ6VLX130T, XQ6VLX240T, and XQ6VSX315T are available in -2I, -1I, -1M, and -1LI temperature ranges.
- The XQ6VLX550T and the XQ6VSX475T are only available in -1I and -1LI temperature ranges.
- Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
- If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPE or XPower Analyzer (XPA) tools.

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. [Table 11](#) summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see [UG361: Virtex-6 FPGA SelectIO Resources User Guide](#).

Table 11: LVPECL DC Specifications

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage	$V_{CC} - 1.025$	1.545	$V_{CC} - 0.88$	V
V_{OL}	Output Low Voltage	$V_{CC} - 1.81$	0.795	$V_{CC} - 1.62$	V
V_{ICM}	Input Common-Mode Voltage	0.6	—	2.2	V
V_{IDIFF}	Differential Input Voltage ⁽¹⁾⁽²⁾	0.100	—	1.5	V

Notes:

1. Recommended input maximum voltage not to exceed $V_{CCAUX} + 0.2V$.
2. Recommended input minimum voltage not to go below $-0.5V$.

eFUSE Read Endurance

[Table 12](#) lists the maximum number of read cycle operations expected. For more information, see [UG360: Virtex-6 FPGA Configuration User Guide](#).

Table 12: eFUSE Read Endurance

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 13: Absolute Maximum Ratings for GTX Transceivers⁽¹⁾

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	−0.5	1.1	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	−0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	−0.5	1.32	V
V _{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	−0.5	1.32	V
V _{MGTREFCLK}	Reference clock absolute input voltage	−0.5	1.32	V

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 14: Recommended Operating Conditions for GTX Transceivers⁽¹⁾⁽²⁾

Symbol	Description	Speed Grade	PLL Frequency	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	-3, -2 ⁽³⁾	> 2.7 GHz	1.0	1.03	1.06	V
		-3, -2 ⁽³⁾	≤ 2.7 GHz	0.95	1.0	1.06	V
		-1	≤ 2.7 GHz	0.95	1.0	1.06	V
		-1L	≤ 2.7 GHz	0.95	1.0	1.05	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	All	—	1.14	1.2	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	All	—	1.14	1.2	1.26	V

Notes:

- Each voltage listed requires the filter circuit described in [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#).
- Voltages are specified for the temperature range of T_j = −40°C to +100°C for all XC devices and T_j = −55°C to +125°C for the XQ devices.
- If a GTX Quad contains transceivers operating with a mixture of PLL frequencies above and below 2.7 GHz, the MGTAVCC voltage supply must be in the range of 1.0V to 1.06V.

Table 15: GTX Transceiver Supply Current (per Lane) ⁽¹⁾⁽²⁾

Symbol	Description	Typ	Max	Units
I _{MGTAVTT}	MGTAVTT supply current for one GTX transceiver	55.9	Note 2	mA
I _{MGTAVCC}	MGTAVCC supply current for one GTX transceiver	56.1		mA
MGTR _{REF}	Precision reference resistor for internal calibration termination	100.0 ± 1% tolerance		Ω

Notes:

- Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
- Values for currents of other transceiver configurations and conditions can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

Table 16: GTX Transceiver Quiescent Supply Current (per Lane) ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Description	Typ ⁽⁴⁾	Max	Units
$I_{\text{MGTA VTTQ}}$	Quiescent MGTA VTT supply current for one GTX transceiver	0.9	Note 2	mA
$I_{\text{MGTA VCCQ}}$	Quiescent MGTA VCC supply current for one GTX transceiver	3.5		mA

Notes:

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.
3. GTX transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX transceivers.
4. Typical values are specified at nominal voltage, 25°C.

GTX Transceiver DC Input and Output Levels

Table 17 summarizes the DC output specifications of the GTX transceivers in Virtex-6 FPGAs. Consult [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#) for further details.

Table 17: GTX Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled ≤ 4.25 Gb/s	125	–	2000	mV
		External AC coupled > 4.25 Gb/s	175	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled MGTA VTT = 1.2V	–400	–	MGTA VTT	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTA VTT = 1.2V	–	2/3 MGTA VTT	–	mV
DV_{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	–	–	1000	mV
V_{CMOUTDC}	DC common mode output voltage.	Equation based	$\text{MGTA VTT} - DV_{\text{PPOUT}}/4$			mV
R_{IN}	Differential input resistance		80	100	130	Ω
R_{OUT}	Differential output resistance		80	100	120	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	8	ps
C_{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#) and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

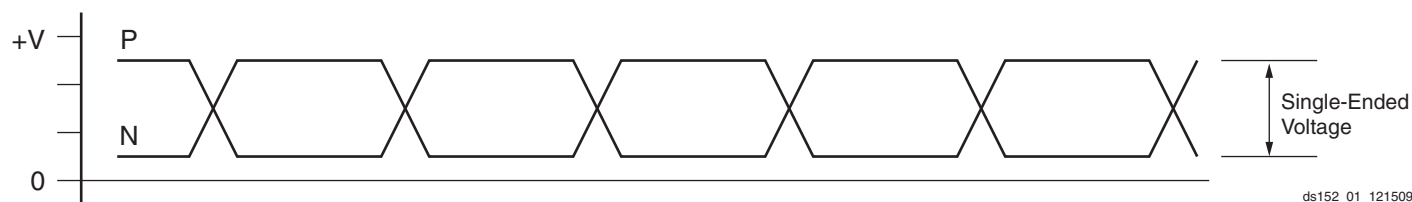


Figure 1: Single-Ended Peak-to-Ppeak Voltage

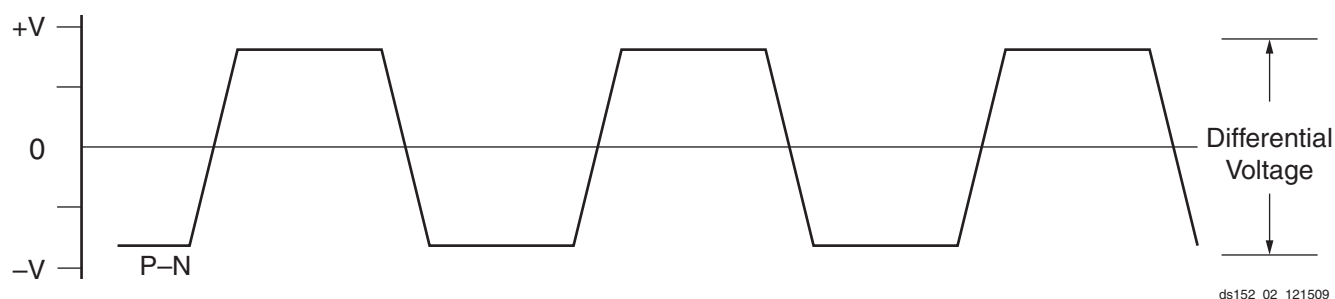


Figure 2: Differential Peak-to-Peak Voltage

Table 18 summarizes the DC specifications of the clock input of the GTX transceiver. Consult [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#) for further details.

Table 18: GTX Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	210	800	2000	mV
R_{IN}	Differential input resistance	90	100	130	Ω
C_{EXT}	Required external AC coupling capacitor	—	100	—	nF

GTX Transceiver Switching Characteristics

Consult [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#) for further information.

Table 19: GTX Transceiver Performance

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F_{GTXMAX}	Maximum GTX transceiver data rate	6.6	6.6	5.0	5.0	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	3.3 ⁽¹⁾	3.3 ⁽¹⁾	2.7	2.7	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.2	1.2	1.2	1.2	GHz

Notes:

- See Table 14 for MGTAVCC requirements when PLL frequency is greater than 2.7 GHz.

Table 20: GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	150	150	125	100	MHz

Table 35: GTH Transceiver User Clock Switching Characteristics ⁽¹⁾

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F _{TXOUT}	TXUSERCLKOUT maximum frequency		350	350	323	MHz
F _{RXOUT}	RXUSERCLKOUT maximum frequency		350	350	323	MHz
F _{TXIN}	TXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz
F _{RXIN}	RXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz

Notes:

1. Clocking must be implemented as described in [UG371](#): Virtex-6 FPGA GTH Transceivers User Guide.

Table 36: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
T _{RTX}	TX Rise time	20%–80%	–	50 ⁽³⁾	–	ps
T _{FTX}	TX Fall time	80%–20%	–	50 ⁽³⁾	–	ps
T _{LLSKEW}	TX lane-to-lane skew	within one GTH Quad	–	–	300	ps
Transmitter Output Jitter⁽¹⁾⁽²⁾						
TJ _{11.18}	Total Jitter	11.181 Gb/s	–	–	0.280	UI
DJ _{11.18}	Deterministic Jitter		–	–	0.170	UI
TJ _{10.3125}	Total Jitter	10.3125 Gb/s	–	–	0.280	UI
DJ _{10.3125}	Deterministic Jitter		–	–	0.170	UI
TJ _{9.953}	Total Jitter	9.953 Gb/s	–	–	0.280	UI
DJ _{9.953}	Deterministic Jitter		–	–	0.170	UI
TJ _{2.667}	Total Jitter	2.667 Gb/s	–	–	0.110	UI
DJ _{2.667}	Deterministic Jitter		–	–	0.060	UI
TJ _{2.488}	Total Jitter	2.488 Gb/s	–	–	0.110	UI
DJ _{2.488}	Deterministic Jitter		–	–	0.060	UI

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit-error ratio of 1e⁻¹².
3. Rise and fall times are specified at the transmitter package balls.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 39: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F _{PIPECLK}	Pipe clock maximum frequency	250	250	250	250	MHz
F _{USERCLK}	User clock maximum frequency	500	500	250	250	MHz
F _{DRPCLK}	DRP clock maximum frequency	250	250	250	250	MHz

System Monitor Analog-to-Digital Converter Specification

Table 40: Analog-to-Digital Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
AV _{DD} = 2.5V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 5.2 MHz, T _j = -55°C to 125°C M-Grade, Typical values at T _j = +35°C						
DC Accuracy: All external input channels. Both unipolar and bipolar modes.						
Resolution			10	–	–	Bits
Integral Nonlinearity	INL		–	–	±1	LSBs
Differential Nonlinearity	DNL	No missing codes (T _{MIN} to T _{MAX}) Guaranteed Monotonic	–	–	±0.9	LSBs
Unipolar Offset Error ⁽¹⁾		Uncalibrated	–	±2	±30	LSBs
Bipolar Offset Error ⁽¹⁾		Uncalibrated measured in bipolar mode	–	±2	±30	LSBs
Gain Error		Uncalibrated - External Reference	–	±0.2	±2	%
		Uncalibrated - Internal Reference	–	±2	–	%
Bipolar Gain Error ⁽¹⁾		Uncalibrated - External Reference	–	±0.2	±2	%
		Uncalibrated - Internal Reference	–	±2	–	%
Total Unadjusted Error (Uncalibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	–	±10	–	LSBs
		Deviation from ideal transfer function. Internal reference	–	±20	–	LSBs
Total Unadjusted Error (Calibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	–	±1	±2	LSBs
Calibrated Gain Temperature Coefficient		Variation of FS code with temperature	–	±0.01	–	LSB/°C
DC Common-Mode Reject	CMRR _{DC}	V _N = V _{CM} = 0.5V ± 0.5V, V _P – V _N = 100mV	–	70	–	dB
Conversion Rate⁽²⁾						
Conversion Time - Continuous	t _{CONV}	Number of CLK cycles	26	–	32	
Conversion Time - Event	t _{CONV}	Number of CLK cycles	–	–	21	
T/H Acquisition Time	t _{ACQ}	Number of CLK cycles	4	–	–	
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	80	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
CLK Duty cycle			40	–	60	%

Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.17 for -3, -2, and -1; and v1.10 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 42 correlates the current status of each Virtex-6 device on a per speed grade basis.

Table 42: Virtex-6 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6VLX75T			-3, -2, -1, -1L
XC6VLX130T			-3, -2, -1, -1L
XC6VLX195T			-3, -2, -1, -1L
XC6VLX240T			-3, -2, -1, -1L
XC6VLX365T			-3, -2, -1, -1L
XC6VLX550T			-2, -1, -1L
XC6VLX760			-2, -1, -1L
XC6VSX315T			-3, -2, -1, -1L
XC6VSX475T			-2, -1, -1L
XC6VHX250T			-3, -2, -1
XC6VHX255T			-3, -2, -1
XC6VHX380T			-3, -2, -1
XC6VHX565T			-2, -1
XQ6VLX130T			-2, -1, -1L
XQ6VLX240T			-2, -1, -1L
XQ6VLX550T			-1, -1L
XQ6VSX315T			-2, -1, -1L
XQ6VSX475T			-1, -1L

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 devices.

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVDCI_DV2_18	0.61	0.72	0.73	1.81	2.36	1.98	1.81	2.36	1.98	ns
LVDCI_DV2_15	0.73	0.85	0.85	1.77	2.30	1.98	1.77	2.30	1.98	ns
LVPECL_25	0.94	1.09	1.08	1.49	2.68	1.64	1.49	2.68	1.64	ns
HSTL_I_12	0.91	1.06	1.06	1.60	2.48	1.74	1.60	2.48	1.74	ns
HSTL_I_DCI	0.91	1.06	1.06	1.50	2.43	1.64	1.50	2.43	1.64	ns
HSTL_II_DCI	0.91	1.06	1.06	1.49	2.39	1.66	1.49	2.39	1.66	ns
HSTL_II_T_DCI	0.91	1.06	1.06	1.50	2.43	1.64	1.50	2.43	1.64	ns
HSTL_III_DCI	0.91	1.06	1.06	1.45	2.48	1.61	1.45	2.48	1.61	ns
HSTL_I_DCI_18	0.91	1.06	1.06	1.53	2.44	1.66	1.53	2.44	1.66	ns
HSTL_II_DCI_18	0.91	1.06	1.06	1.46	2.41	1.59	1.46	2.41	1.59	ns
HSTL_II_T_DCI_18	0.91	1.06	1.06	1.53	2.43	1.66	1.53	2.43	1.66	ns
HSTL_III_DCI_18	0.91	1.06	1.06	1.54	2.50	1.67	1.54	2.50	1.67	ns
DIFF_HSTL_I_18	0.94	1.09	1.08	1.58	2.30	1.72	1.58	2.30	1.72	ns
DIFF_HSTL_I_DCI_18	0.94	1.09	1.08	1.53	2.21	1.66	1.53	2.21	1.66	ns
DIFF_HSTL_I	0.94	1.09	1.08	1.56	2.28	1.71	1.56	2.28	1.71	ns
DIFF_HSTL_I_DCI	0.94	1.09	1.08	1.50	2.28	1.64	1.50	2.28	1.64	ns
DIFF_HSTL_II_18	0.94	1.09	1.08	1.62	2.33	1.78	1.62	2.33	1.78	ns
DIFF_HSTL_II_DCI_18	0.94	1.09	1.08	1.46	2.18	1.59	1.46	2.18	1.59	ns
DIFF_HSTL_II_T_DCI_18	0.94	1.09	1.08	1.53	2.22	1.66	1.53	2.22	1.66	ns
DIFF_HSTL_II	0.94	1.09	1.08	1.56	2.29	1.72	1.56	2.29	1.72	ns
DIFF_HSTL_II_DCI	0.94	1.09	1.08	1.49	2.26	1.66	1.49	2.26	1.66	ns
SSTL2_I_DCI	0.91	1.06	1.06	1.53	2.51	1.68	1.53	2.51	1.68	ns
SSTL2_II_DCI	0.91	1.06	1.06	1.50	2.50	1.69	1.50	2.50	1.69	ns
SSTL2_II_T_DCI	0.91	1.06	1.06	1.53	2.52	1.68	1.53	2.52	1.68	ns
SSTL18_I	0.91	1.06	1.06	1.58	2.48	1.73	1.58	2.48	1.73	ns
SSTL18_II	0.91	1.06	1.06	1.50	2.46	1.66	1.50	2.46	1.66	ns
SSTL18_I_DCI	0.91	1.06	1.06	1.51	2.49	1.65	1.51	2.49	1.65	ns
SSTL18_II_DCI	0.91	1.06	1.06	1.47	2.41	1.62	1.47	2.41	1.62	ns
SSTL18_II_T_DCI	0.91	1.06	1.06	1.51	2.49	1.65	1.51	2.49	1.65	ns
SSTL15_T_DCI	0.91	1.06	1.06	1.52	2.48	1.66	1.52	2.48	1.66	ns
SSTL15_DCI	0.91	1.06	1.06	1.52	2.48	1.66	1.52	2.48	1.66	ns
DIFF_SSTL2_I	0.94	1.09	1.08	1.60	2.34	1.74	1.60	2.34	1.74	ns
DIFF_SSTL2_I_DCI	0.94	1.09	1.08	1.53	2.25	1.68	1.53	2.25	1.68	ns
DIFF_SSTL2_II	0.94	1.09	1.08	1.54	2.29	1.71	1.54	2.29	1.71	ns
DIFF_SSTL2_II_DCI	0.94	1.09	1.08	1.50	2.23	1.69	1.50	2.23	1.69	ns
DIFF_SSTL2_II_T_DCI	0.94	1.09	1.08	1.53	2.26	1.68	1.53	2.26	1.68	ns
DIFF_SSTL18_I	0.94	1.09	1.08	1.58	2.22	1.73	1.58	2.22	1.73	ns
DIFF_SSTL18_I_DCI	0.94	1.09	1.08	1.51	2.30	1.65	1.51	2.30	1.65	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
DIFF_SSTL18_II	0.94	1.09	1.08	1.50	2.27	1.66	1.50	2.27	1.66	ns
DIFF_SSTL18_II_DCI	0.94	1.09	1.08	1.47	2.20	1.62	1.47	2.20	1.62	ns
DIFF_SSTL18_II_T_DCI	0.94	1.09	1.08	1.51	2.30	1.65	1.51	2.30	1.65	ns
DIFF_SSTL15	0.91	1.06	1.06	1.54	2.25	1.69	1.54	2.25	1.69	ns
DIFF_SSTL15_DCI	0.91	1.06	1.06	1.52	2.25	1.66	1.52	2.25	1.66	ns
DIFF_SSTL15_T_DCI	0.91	1.06	1.06	1.52	2.25	1.66	1.52	2.25	1.66	ns

Table 46: IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{IOTPHZ}	T input to Pad high-impedance	0.86	0.92	0.99	0.99	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 47 shows the test setup parameters used for measuring input delay.

Table 47: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)(2)}$	$V_H^{(1)(2)}$	$V_{MEAS}^{(1)(4)(5)}$	$V_{REF}^{(1)(3)(5)}$
LVC MOS, 2.5V	LVC MOS25	0	2.5	1.25	—
LVC MOS, 1.8V	LVC MOS18	0	1.8	0.9	—
LVC MOS, 1.5V	LVC MOS15	0	1.5	0.75	—
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL, Class III	HSTL_III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	$V_{REF} - 1.00$	$V_{REF} + 1.00$	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	$1.2 - 0.125$	$1.2 + 0.125$	$0^{(6)}$	—
LVDS EXT (LVDS Extended Mode), 2.5V	LVDS EXT_25	$1.2 - 0.125$	$1.2 + 0.125$	$0^{(6)}$	—
HT (HyperTransport), 2.5V	LDT_25	$0.6 - 0.125$	$0.6 + 0.125$	$0^{(6)}$	—

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVC MOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H .
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 6.
6. The value given is the differential input voltage.

Table 48: Output Delay Measurement Methodology (Cont'd)

Description	I/O Standard Attribute	R _{REF} (Ω)	C _{REF} ⁽¹⁾ (pF)	V _{MEAS} (V)	V _{REF} (V)
HT (HyperTransport), 2.5V	LDT_25	100	0	0 ⁽²⁾	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	100	0	0 ⁽²⁾	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V _{REF}	0.75
HSTL, Class III, with DCI	HSTL_III_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V _{REF}	0.9
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termination Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V _{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V _{REF}	1.25

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 49: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Setup/Hold						
T _{ICE1CK} /T _{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.21/ 0.03	0.25/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T _{ISRCK} /T _{ICKSR}	SR pin Setup/Hold with respect to CLK	0.66/ −0.08	0.78/ −0.08	0.96/ −0.08	1.09/ −0.11	ns
T _{IDOCK} /T _{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.07/ 0.41	0.08/ 0.46	0.10/ 0.54	0.11/ 0.64	ns
T _{IDOCKD} /T _{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.10/ 0.32	0.12/ 0.36	0.14/ 0.42	0.16/ 0.50	ns
Combinatorial						
T _{IDI}	D pin to O pin propagation delay, no Delay	0.15	0.17	0.20	0.23	ns
T _{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.19	0.22	0.25	0.28	ns
Sequential Delays						
T _{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.48	0.54	0.64	0.73	ns
T _{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.52	0.58	0.68	0.78	ns
T _{ICKQ}	CLK to Q outputs	0.54	0.61	0.70	0.93	ns
T _{RQ_ILOGIC}	SR pin to OQ/TQ out	0.85	0.97	1.15	1.32	ns
T _{GSRQ_ILOGIC}	Global Set/Reset to Q outputs	7.60	7.60	10.51	10.51	ns
Set/Reset						
T _{RPW_ILOGIC}	Minimum Pulse Width, SR inputs	0.78	0.95	1.20	1.30	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 51: ISERDES Switching Characteristics

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup/Hold for Control Lines							
T _{ISCKK_BITSIP} / T _{ISCKC_BITSIP}	BITSLIP pin Setup/Hold with respect to CLKDIV	0.07/ 0.15	0.08/ 0.16	0.09/ 0.17	0.09/ 0.17	0.14/ 0.17	ns
T _{ISCKK_CE} / T _{ISCKC_CE} ⁽²⁾	CE pin Setup/Hold with respect to CLK (for CE1)	0.20/ 0.03	0.25/ 0.04	0.27/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T _{ISCKK_CE2} / T _{ISCKC_CE2} ⁽²⁾	CE pin Setup/Hold with respect to CLKDIV (for CE2)	0.01/ 0.27	0.01 0.29	0.01/ 0.31	0.01/ 0.31	−0.05/ 0.35	ns
Setup/Hold for Data Lines							
T _{ISDCK_D} / T _{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.07/ 0.08	0.08/ 0.09	0.09/ 0.11	0.09/ 0.11	0.11/ 0.19	ns
T _{ISDCK_DDLY} / T _{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY) ⁽¹⁾	0.10/ 0.05	0.12/ 0.06	0.14/ 0.07	0.14/ 0.07	0.16/ 0.15	ns
T _{ISDCK_D_DDR} / T _{ISCKD_D_DDR}	D pin Setup/Hold with respect to CLK at DDR mode	0.07/ 0.08	0.08/ 0.09	0.09/ 0.11	0.09/ 0.11	0.11/ 0.19	ns
T _{ISDCK_DDLY_DDR} / T _{ISCKD_DDLY_DDR}	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY) ⁽¹⁾	0.10/ 0.05	0.12/ 0.06	0.14/ 0.07	0.14/ 0.07	0.16/ 0.15	ns
Sequential Delays							
T _{ISCKO_Q}	CLKDIV to out at Q pin	0.57	0.66	0.75	0.80	0.88	ns
Propagation Delays							
T _{ISDO_DO}	D input to DO output pin	0.19	0.22	0.25	0.25	0.28	ns

Notes:

- Recorded at 0 tap value.
- T_{ISCK_CE2} and T_{ISCK_CE2} are reported as $T_{ISCK_CE} / T_{ISCK_CE}$ in TRACE report.

Input/Output Delay Switching Characteristics

Table 53: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
IDELAYCTRL						
T _{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3.00	3.00	3.00	3.25	μs
F _{IDELAYCTRL_REF}	REFCLK frequency = 200.0 ⁽¹⁾	200	200	200	200	MHz
	REFCLK frequency = 300.0 ⁽¹⁾	300	300	–	–	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
T _{IDELAYCTRL_RPW}	Minimum Reset pulse width	50.00	50.00	50.00	52.50	ns
IODELAY						
T _{IDELAYRESOLUTION}	IODELAY Chain Delay Resolution	1/(32 x 2 x F _{REF})				ps
T _{IDELAYPAT_JIT}	Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾	0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). ⁽³⁾	±5	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). ⁽⁴⁾	±9	±9	±9	±9	ps per tap
T _{IODELAY_CLK_MAX}	Maximum frequency of CLK input to IDELAY	500.00	420.00	300.00	300.00	MHz
T _{IODCCK_CE} / T _{IODCKC_CE}	CE pin Setup/Hold with respect to CK	0.45/ –0.09	0.53/ –0.09	0.65/ –0.09	0.84/ –0.14	ns
T _{IODCK_INC} / T _{IODCKC_INC}	INC pin Setup/Hold with respect to CK	0.23/ –0.02	0.27/ –0.01	0.31/ 0.00	0.27/ –0.04	ns
T _{IODCCK_RST} / T _{IODCKC_RST}	RST pin Setup/Hold with respect to CK	0.57/ –0.08	0.62/ –0.08	0.69/ –0.08	0.74/ –0.13	ns
T _{IODDO_T}	TSCONTROL delay to MUXE/MUXF switching and through IDELAY	Note 5	Note 5	Note 5	Note 5	ps
T _{IODDO_IDATAIN}	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	ps
T _{IODDO_ODATAIN}	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See TRACE report for actual values.

CLB Switching Characteristics

Table 54: CLB Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Combinatorial Delays						
T _{ILO}	An – Dn LUT address to A	0.06	0.07	0.07	0.09	ns, Max
	An – Dn LUT address to AMUX/CMUX	0.18	0.20	0.22	0.25	ns, Max
	An – Dn LUT address to BMUX_A	0.28	0.31	0.36	0.40	ns, Max

Table 58: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
$T_{\text{DSPDCK_RSTP_PREG}} / T_{\text{DSPCKD_RSTP_PREG}}$	RSTP input to P register CLK	0.26/ 0.04	0.30/ 0.04	0.35/ 0.05	0.35/ 0.05	0.43/ 0.06	ns
Combinatorial Delays from Input Pins to Output Pins							
$T_{\text{DSPDO_}\{A, B\}_ \{P, \text{CARRYOUT}\}_ \text{MULT}}$	{A, B} input to {P, CARRYOUT} output using multiplier	3.76	4.29	5.08	5.08	5.87	ns
$T_{\text{DSPDO_D_}\{P, \text{CARRYOUT}\}_ \text{MULT}}$	D input to {P, CARRYOUT} output using multiplier	3.57	4.07	4.82	4.82	5.57	ns
$T_{\text{DSPDO_}\{A, B\}_ \{P, \text{CARRYOUT}\}}$	{A, B} input to {P, CARRYOUT} output not using multiplier	1.55	1.76	2.07	2.07	2.41	ns
$T_{\text{DSPDO_}\{C, \text{CARRYIN}\}_ \{P, \text{CARRYOUT}\}}$	{C, CARRYIN} input to {P, CARRYOUT} output	1.38	1.56	1.83	1.83	2.13	ns
Combinatorial Delays from Input Pins to Cascading Output Pins							
$T_{\text{DSPDO_}\{A, B\}_ \{ACOUT, BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.49	0.56	0.65	0.65	0.73	ns
$T_{\text{DSPDO_}\{A, B\}_ \{PCOUT, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}_ \text{MULT}}$	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.87	4.42	5.24	5.24	6.09	ns
$T_{\text{DSPDO_D_}\{PCOUT, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}_ \text{MULT}}$	D input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.66	4.17	4.94	4.94	5.76	ns
$T_{\text{DSPDO_}\{A, B\}_ \{PCOUT, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}$	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.64	1.86	2.19	2.19	2.60	ns
$T_{\text{DSPDO_}\{C, \text{CARRYIN}\}_ \{PCOUT, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}$	{C, CARRYIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.46	1.66	1.95	1.95	2.32	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins							
$T_{\text{DSPDO_}\{ACIN, BCIN\}_ \{P, \text{CARRYOUT}\}_ \text{MULT}}$	{ACIN, BCIN} input to {P, CARRYOUT} output using multiplier	3.67	4.19	4.97	4.97	5.75	ns
$T_{\text{DSPDO_}\{ACIN, BCIN\}_ \{P, \text{CARRYOUT}\}}$	{ACIN, BCIN} input to {P, CARRYOUT} output not using multiplier	1.43	1.63	1.92	1.92	2.25	ns
$T_{\text{DSPDO_}\{ACIN, BCIN\}_ \{ACOUT, BCOUT\}}$	{ACIN, BCIN} input to {ACOUT, BCOUT} output	0.36	0.42	0.49	0.49	0.56	ns
$T_{\text{DSPDO_}\{ACIN, BCIN\}_ \{PCOUT, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}_ \text{MULT}}$	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.76	4.29	5.10	5.10	5.94	ns
$T_{\text{DSPDO_}\{ACIN, BCIN\}_ \{PCOUT, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}$	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.52	1.73	2.05	2.05	2.44	ns
$T_{\text{DSPDO_}\{PCIN, \text{CARRYCASCIN}, \text{MULTSIGNIN}\}_ \{P, \text{CARRYOUT}\}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {P, CARRYOUT} output	1.19	1.35	1.60	1.60	1.87	ns

Table 58: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
$T_{DSPDO_PCIN, CARRYCASCIN, MULTSIGNIN_PCOUT, CARRYCASCOUT, MULTSIGNOUT}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.28	1.46	1.72	1.72	2.06	ns
Clock to Outs from Output Register Clock to Output Pins							
$T_{DSPCKO_P, CARRYOUT_PREG}$	CLK (PREG) to {P, CARRYOUT} output	0.38	0.43	0.50	0.50	0.57	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_PREG}$	CLK (PREG) to {CARRYCASCOUT, PCOUT, MULTSIGNOUT} output	0.50	0.56	0.66	0.66	0.76	ns
Clock to Outs from Pipeline Register Clock to Output Pins							
$T_{DSPCKO_P, CARRYOUT_MREG}$	CLK (MREG) to {P, CARRYOUT} output	1.72	1.96	2.30	2.30	2.69	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_MREG}$	CLK (MREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.81	2.06	2.43	2.43	2.88	ns
$T_{DSPCKO_P, CARRYOUT_ADREG_MULT}$	CLK (ADREG) to {P, CARRYOUT} output	2.79	3.16	3.72	3.72	4.32	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_ADREG_MULT}$	CLK (ADREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.87	3.26	3.84	3.84	4.51	ns
Clock to Outs from Input Register Clock to Output Pins							
$T_{DSPCKO_P, CARRYOUT_AREG, BREG_MULT}$	CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier	3.97	4.52	5.36	5.36	6.20	ns
$T_{DSPCKO_P, CARRYOUT_AREG, BREG}$	CLK (AREG, BREG) to {P, CARRYOUT} output not using multiplier	1.70	1.93	2.27	2.27	2.65	ns
$T_{DSPCKO_P, CARRYOUT_CREG}$	CLK (CREG) to {P, CARRYOUT} output	1.70	1.93	2.27	2.27	2.80	ns
$T_{DSPCKO_P, CARRYOUT_DREG_MULT}$	CLK (DREG) to {P, CARRYOUT} output	3.89	4.44	5.25	5.25	6.07	ns
Clock to Outs from Input Register Clock to Cascading Output Pins							
$T_{DSPCKO_ACOUT, BCOUT_AREG, BREG}$	CLK (AREG, BREG) to {P, CARRYOUT} output	0.66	0.76	0.89	0.89	1.01	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_AREG, BREG_MULT}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	4.05	4.63	5.49	5.49	6.39	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_AREG, BREG}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.79	2.03	2.40	2.40	2.84	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_DREG_MULT}$	CLK (DREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.98	4.54	5.38	5.38	6.26	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_CREG}$	CLK (CREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.78	2.03	2.40	2.40	2.99	ns

Table 59: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{\text{MMCMDCK_DI}}/$ $T_{\text{MMCCKD_DI}}$	DI Setup/Hold	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{\text{MMCMDCK_DEN}}/$ $T_{\text{MMCCKD_DEN}}$	DEN Setup/Hold time	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{\text{MMCMDCK_DWE}}/$ $T_{\text{MMCCKD_DWE}}$	DWE Setup/Hold time	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{\text{MMCCKO_DO}}$	CLK to out of DO ⁽³⁾	2.60	3.02	3.64	3.68	ns
$T_{\text{MMCCKO_DRDY}}$	CLK to out of DRDY	0.32	0.34	0.38	0.38	ns

Notes:

1. To support longer delays in configuration, use the design solutions described in [UG360: Virtex-6 FPGA Configuration User Guide](#).
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
3. DO will hold until next DRP operation.

Clock Buffers and Networks

Table 60: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	Devices	Speed Grade				Units
			-3	-2	-1	-1L	
$T_{\text{BCCCK_CE}}/T_{\text{BCCKC_CE}}^{(1)}$	CE pins Setup/Hold	All	0.11/ 0.00	0.13/ 0.00	0.16/ 0.00	0.13/ 0.00	ns
$T_{\text{BCCCK_S}}/T_{\text{BCCKC_S}}^{(1)}$	S pins Setup/Hold	All	0.11/ 0.00	0.13/ 0.00	0.16/ 0.00	0.13/ 0.00	ns
$T_{\text{BCKO_O}}^{(2)}$	BUFGCTRL delay from I0/I1 to O	All	0.07	0.08	0.10	0.10	ns
Maximum Frequency							
F_{MAX}	Global clock tree (BUFG)	All except LX760	800	750	700	667	MHz
		LX760	N/A	700	700	667	MHz

Notes:

1. $T_{\text{BCCCK_CE}}$ and $T_{\text{BCCKC_CE}}$ must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. $T_{\text{BCKO_O}}$ (BUFG delay from I0 to O) values are the same as $T_{\text{BCKO_O}}$ values.

Table 61: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{\text{BIOCKO_O}}$	Clock to out delay from I to O	0.14	0.16	0.18	0.21	ns
Maximum Frequency						
F_{MAX}	I/O clock tree (BUFIO)	800	800	710	710	MHz

Table 62: Regional Clock Switching Characteristics (BUFR)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{\text{BRCKO_O}}$	Clock to out delay from I to O	0.56	0.62	0.73	0.82	ns
$T_{\text{BRCKO_O_BYP}}$	Clock to out delay from I to O with Divide Bypass attribute set	0.28	0.31	0.36	0.41	ns

Table 67: Clock-Capable Clock Input to Output Delay With MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Clock-capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> MMCM.							
T _{ICKOFMMCMCC}	Clock-capable Clock Input and OUTFF <i>with</i> MMCM	XC6VLX75T	2.22	2.38	2.63	2.72	ns
		XC6VLX130T	2.24	2.39	2.65	2.74	ns
		XC6VLX195T	2.24	2.40	2.65	2.75	ns
		XC6VLX240T	2.24	2.40	2.65	2.75	ns
		XC6VLX365T	2.25	2.42	2.65	2.76	ns
		XC6VLX550T	N/A	2.43	2.68	2.80	ns
		XC6VLX760	N/A	2.42	2.69	2.79	ns
		XC6VSX315T	2.23	2.38	2.65	2.73	ns
		XC6VSX475T	N/A	2.30	2.57	2.66	ns
		XC6VHX250T	2.25	2.41	2.67	N/A	ns
		XC6VHX255T	2.35	2.51	2.78	N/A	ns
		XC6VHX380T	2.27	2.43	2.69	N/A	ns
		XC6VHX565T	N/A	2.41	2.68	N/A	ns
		XQ6VLX130T	N/A	2.39	2.65	2.74	ns
		XQ6VLX240T	N/A	2.40	2.65	2.75	ns
		XQ6VLX550T	N/A	N/A	2.68	2.80	ns
		XQ6VSX315T	N/A	2.38	2.65	2.73	ns
		XQ6VSX475T	N/A	N/A	2.57	2.66	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 72: Package Skew

Symbol	Description	Device	Package	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	XC6VLX75T	FF484	95	ps
			FF784	146	ps
		XC6VLX130T	FF484	95	ps
			FF784	146	ps
			FF1156	165	ps
		XC6VLX195T	FF784	145	ps
			FF1156	182	ps
		XC6VLX240T	FF784	146	ps
			FF1156	182	ps
			FF1759	187	ps
		XC6VLX365T	FF1156	189	ps
			FF1759	184	ps
		XC6VLX550T	FF1759	196	ps
			FF1760	249	ps
		XC6VLX760	FF1760	236	ps
		XC6VSX315T	FF1156	168	ps
			FF1759	190	ps
		XC6VSX475T	FF1156	168	ps
			FF1759	204	ps
		XC6VHX250T	FF1154	166	ps
		XC6VHX255T	FF1155	168	ps
			FF1923	228	ps
		XC6VHX380T	FF1154	159	ps
			FF1155	172	ps
			FF1923	227	ps
			FF1924	220	ps
		XC6VHX565T	FF1923	232	ps
			FF1924	197	ps
		XQ6VLX130T	RF784	146	ps
			RF1156	165	ps
			FFG1156	165	ps
		XQ6VLX240T	RF784	146	ps
			RF1156	182	ps
			FFG1156	182	ps
			RF1759	187	ps
		XQ6VLX550T	RF1759	196	ps
		XQ6VSX315T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	190	ps
		XQ6VSX475T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	204	ps

Notes:

- These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
- Package trace length information is available for these device/package combinations. This information can be used to deskew the package.