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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	15600
Number of Logic Elements/Cells	199680
Total RAM Bits	12681216
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1156-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vlx195t-l1ffg1156c

Table 2: **Recommended Operating Conditions**

Symbol	Description	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND for all devices except -1L devices.	0.95	1.05	V
	For -1L commercial temperature range devices: internal supply voltage relative to GND, T_j = 0°C to +85°C	0.87	0.93	V
	For -1L industrial temperature range devices: internal supply voltage relative to GND, T_j = –40°C to +100°C	0.91	0.97	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	2.375	2.625	V
V_{CCO}(1)(2)(3)	Supply voltage relative to GND	1.14	2.625	V
V_{IN}	2.5V supply voltage relative to GND	GND – 0.20	2.625	V
	2.5V and below supply voltage relative to GND	GND – 0.20	V_{CCO} + 0.2	V
I_{IN}(5)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	10	mA
V_{BATT}(6)	Battery voltage relative to GND	1.0	2.5	V
V_{FS}(7)	External voltage supply for eFUSE programming	2.375	2.625	V
T_j	Junction temperature operating range for commercial (C) temperature devices	0	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	100	°C
	Junction temperature operating range for military (M) temperature devices	–55	125	°C

Notes:

1. Configuration data is retained even if V_{CCO} drops to 0V.
2. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, and 2.5V.
3. The configuration supply voltage V_{CC_CONFIG} is also known as V_{CCO_0}.
4. All voltages are relative to ground.
5. A total of 100 mA per bank should not be exceeded.
6. V_{BATT} is required only when using bitstream encryption. If battery is not used, connect V_{BATT} to either ground or V_{CCAUX}.
7. During eFUSE programming, V_{FS} must be within the recommended operating range and T_j = +15°C to +85°C. Otherwise, V_{FS} can be connected to GND.

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 13: **Absolute Maximum Ratings for GTX Transceivers(1)**

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	–0.5	1.1	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	–0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 14: **Recommended Operating Conditions for GTX Transceivers(1)(2)**

Symbol	Description	Speed Grade	PLL Frequency	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	-3, -2(3)	> 2.7 GHz	1.0	1.03	1.06	V
		-3, -2(3)	≤ 2.7 GHz	0.95	1.0	1.06	V
		-1	≤ 2.7 GHz	0.95	1.0	1.06	V
		-1L	≤ 2.7 GHz	0.95	1.0	1.05	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	All	–	1.14	1.2	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	All	–	1.14	1.2	1.26	V

Notes:

1. Each voltage listed requires the filter circuit described in UG366: *Virtex-6 FPGA GTX Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +100°C for all XC devices and T_j = –55°C to +125°C for the XQ devices
3. If a GTX Quad contains transceivers operating with a mixture of PLL frequencies above and below 2.7 GHz, the MGTAVCC voltage supply must be in the range of 1.0V to 1.06V.

Table 15: **GTX Transceiver Supply Current (per Lane) (1)(2)**

Symbol	Description	Typ	Max	Units
$I_{MGTAVTT}$	MGTAVTT supply current for one GTX transceiver	55.9	Note 2	mA
$I_{MGTAVCC}$	MGTAVCC supply current for one GTX transceiver	56.1		mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	100.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
2. Values for currents of other transceiver configurations and conditions can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

Table 16: **GTX Transceiver Quiescent Supply Current (per Lane) (1)(2)(3)**

Symbol	Description	Typ(4)	Max	Units
$I_{MGTAVTTQ}$	Quiescent MGTAVTT supply current for one GTX transceiver	0.9	Note 2	mA
$I_{MGTAVCCQ}$	Quiescent MGTAVCC supply current for one GTX transceiver	3.5		mA

Notes:

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.
3. GTX transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX transceivers.
4. Typical values are specified at nominal voltage, 25°C.

GTX Transceiver DC Input and Output Levels

Table 17 summarizes the DC output specifications of the GTX transceivers in Virtex-6 FPGAs. Consult UG366: *Virtex-6 FPGA GTX Transceivers User Guide* for further details.

Table 17: **GTX Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled ≤ 4.25 Gb/s	125	–	2000	mV
		External AC coupled > 4.25 Gb/s	175	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled MGTAVTT = 1.2V	–400	–	MGTAVTT	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTT = 1.2V	–	2/3 MGTAVTT	–	mV
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage.	Equation based	MGTAVTT – DV_{PPOUT}/4			mV
R_{IN}	Differential input resistance		80	100	130	Ω
R_{OUT}	Differential output resistance		80	100	120	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	8	ps
C_{EXT}	Recommended external AC coupling capacitor(2)		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG366: *Virtex-6 FPGA GTX Transceivers User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

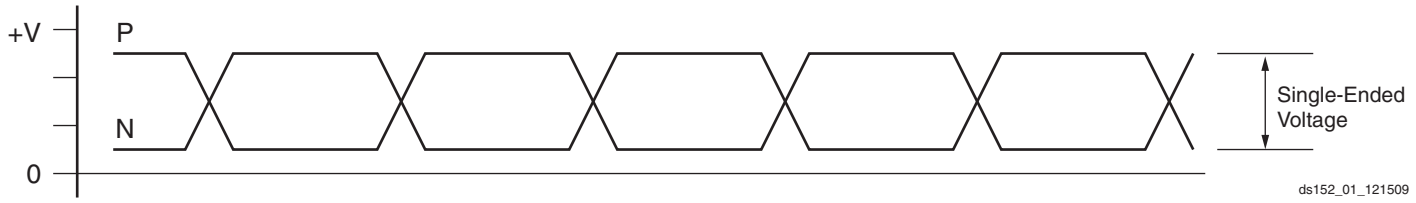

Figure 1: **Single-Ended Peak-to-Peak Voltage**

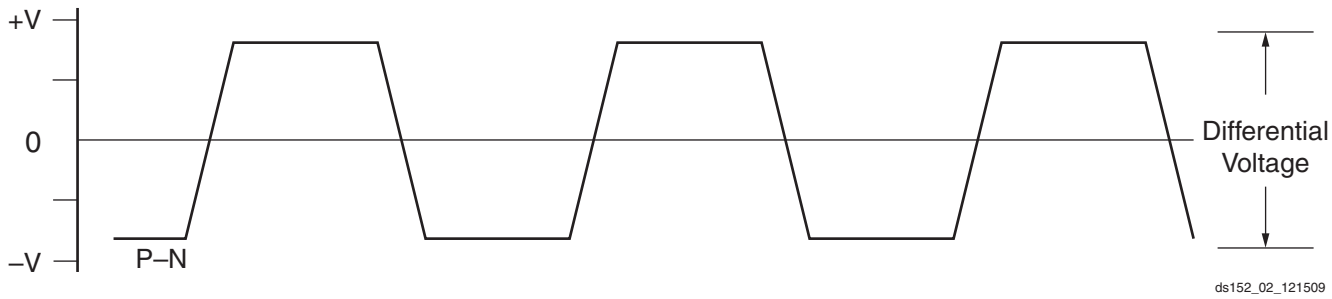

Figure 2: **Differential Peak-to-Peak Voltage**

Table 18 summarizes the DC specifications of the clock input of the GTX transceiver. Consult UG366: *Virtex-6 FPGA GTX Transceivers User Guide* for further details.

Table 18: **GTX Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	210	800	2000	mV
R_{IN}	Differential input resistance	90	100	130	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTX Transceiver Switching Characteristics

Consult UG366: *Virtex-6 FPGA GTX Transceivers User Guide* for further information.

Table 19: **GTX Transceiver Performance**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F_{GTXMAX}	Maximum GTX transceiver data rate	6.6	6.6	5.0	5.0	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	3.3(1)	3.3(1)	2.7	2.7	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.2	1.2	1.2	1.2	GHz

Notes:

1. See Table 14 for MGTAVCC requirements when PLL frequency is greater than 2.7 GHz.

Table 20: **GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	150	150	125	100	MHz

Table 21: **GTX Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		62.5	–	650	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	200	µs

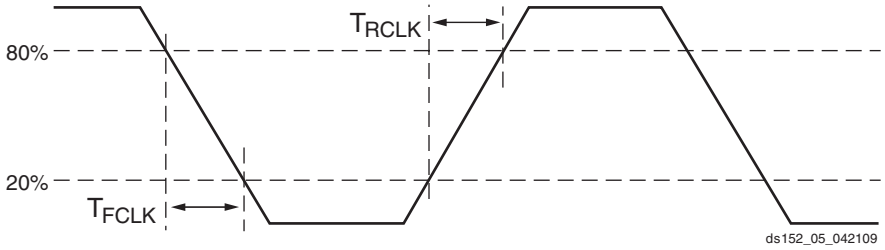

Figure 3: **Reference Clock Timing Parameters**

Table 22: **GTX Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1	-1L	
F_{TXOUT}	TXOUTCLK maximum frequency	Internal 20-bit data path	330	330	250	250	MHz
		Internal 16-bit data path	412.5	412.5	312.5	250	MHz
F_{RXREC}	RXRECCLK maximum frequency	Internal 20-bit data path	330	330	250	250	MHz
		Internal 16-bit data path	412.5	412.5	312.5	250	MHz
T_{RX}	RXUSRCLK maximum frequency		412.5(2)	412.5(2)	312.5	250	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	376	376	312.5	250	MHz
		2 byte interface	406.25	406.25	312.5	250	MHz
		4 byte interface	206.25	206.25	156.25	125	MHz
T_{TX}	TXUSRCLK maximum frequency		412.5(3)	412.5(3)	312.5	250	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	376	376	312.5	250	MHz
		2 byte interface	406.25	406.25	312.5	250	MHz
		4 byte interface	206.25	206.25	156.25	125	MHz

Notes:

1. Clocking must be implemented as described in UG366: *Virtex-6 FPGA GTX Transceivers User Guide*.
2. 406.25 MHz when the RX elastic buffer is bypassed.
3. 406.25 MHz when the TX buffer is bypassed.

Figure 4 shows the timing parameters in Table 27.

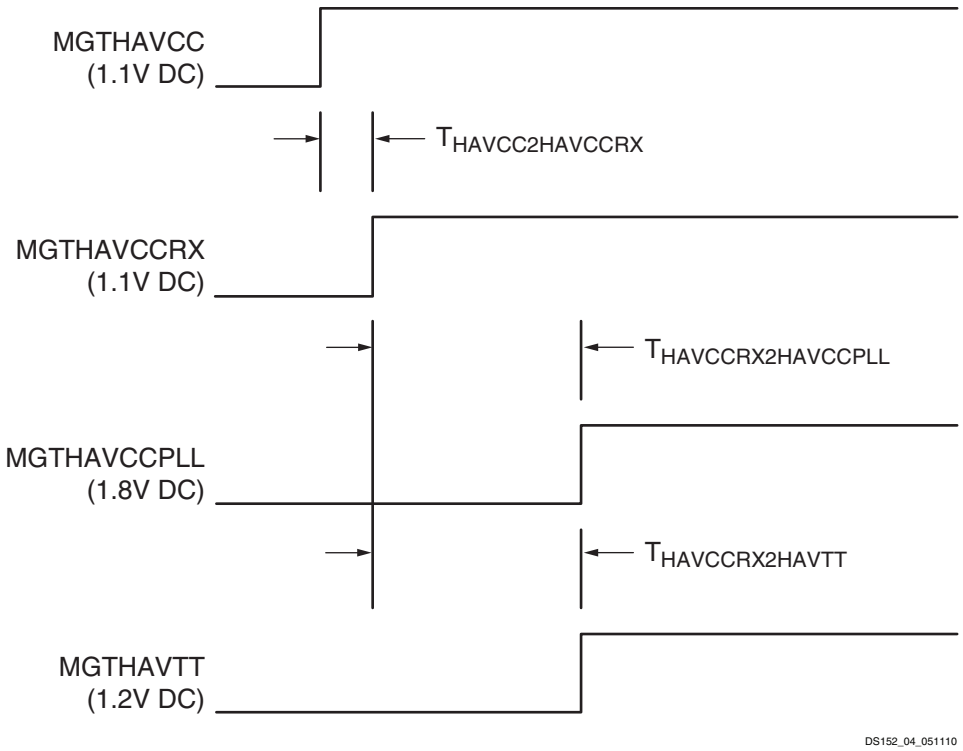

Figure 4: **GTH Transceiver Power Supply Power-On Sequencing**

Table 28: **GTH Transceiver Supply Current**

Symbol	Description	Typ(1)	Max	Units
$I_{MGTHAVCC}$	MGTHAVCC supply current for one GTH Quad (4 lanes)	571	Note 2	mA
$I_{MGTHAVCCRX}$	MGTHAVCCRX supply current for a GTH Quad (4 lanes)	254	Note 2	mA
$I_{MGTHAVTT}$	MGTHAVTT supply current for one GTH Quad (4 lanes)	93	Note 2	mA
$I_{MGTHAVCCPLL}$	MGTHAVCCPLL supply current for one GTH Quad (4 lanes)	219	Note 2	mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	1000.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 10.3125 Gb/s line rate.
2. Values for currents other than the values specified in this table can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

Table 29: **GTH Transceiver Quiescent Supply Current(1)(2)**

Symbol	Description	Typ(3)	Max	Units
$I_{MGTHAVCCQ}$	Quiescent MGTHAVCC Supply Current for one GTH Quad (4 lanes)	65	Note 4	mA
$I_{MGTHAVCCRXQ}$	Quiescent MGTHAVCCRX Supply Current for one GTH Quad (4 lanes)	17	Note 4	mA
$I_{MGTHAVTTQ}$	Quiescent MGTHAVTT Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA
$I_{MGTHAVCCPLLQ}$	Quiescent MGTHAVCCPLL Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA

Notes:

1. Device powered and unconfigured.
2. GTH transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTH transceivers.
3. Typical values are specified at nominal voltage, 25°C.
4. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.

Table 35: **GTH Transceiver User Clock Switching Characteristics (1)**

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F_{TXOUT}	TXUSERCLKOUT maximum frequency		350	350	323	MHz
F_{RXOUT}	RXUSERCLKOUT maximum frequency		350	350	323	MHz
F_{TXIN}	TXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz
F_{RXIN}	RXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz

Notes:

1. Clocking must be implemented as described in UG371:*Virtex-6 FPGA GTH Transceivers User Guide*.

Table 36: **GTH Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
T_{RTX}	TX Rise time	20%–80%	–	50(3)	–	ps
T_{FTX}	TX Fall time	80%–20%	–	50(3)	–	ps
T_{LLSKEW}	TX lane-to-lane skew	within one GTH Quad	–	–	300	ps
Transmitter Output Jitter(1)(2)						
$TJ_{11.18}$	Total Jitter	11.181 Gb/s	–	–	0.280	UI
$DJ_{11.18}$	Deterministic Jitter		–	–	0.170	UI
$TJ_{10.3125}$	Total Jitter	10.3125 Gb/s	–	–	0.280	UI
$DJ_{10.3125}$	Deterministic Jitter		–	–	0.170	UI
$TJ_{9.953}$	Total Jitter	9.953 Gb/s	–	–	0.280	UI
$DJ_{9.953}$	Deterministic Jitter		–	–	0.170	UI
$TJ_{2.667}$	Total Jitter	2.667 Gb/s	–	–	0.110	UI
$DJ_{2.667}$	Deterministic Jitter		–	–	0.060	UI
$TJ_{2.488}$	Total Jitter	2.488 Gb/s	–	–	0.110	UI
$DJ_{2.488}$	Deterministic Jitter		–	–	0.060	UI

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit-error ratio of $1e^{-12}$.
3. Rise and fall times are specified at the transmitter package balls.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

Table 39: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$F_{PIPECLK}$	Pipe clock maximum frequency	250	250	250	250	MHz
$F_{USERCLK}$	User clock maximum frequency	500	500	250	250	MHz
F_{DRPCLK}	DRP clock maximum frequency	250	250	250	250	MHz

System Monitor Analog-to-Digital Converter Specification

Table 40: **Analog-to-Digital Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
AV_{DD} = 2.5V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_j = –55°C to 125°C M-Grade, Typical values at T_j=+35°C						
DC Accuracy: All external input channels. Both unipolar and bipolar modes.						
Resolution			10	–	–	Bits
Integral Nonlinearity	INL		–	–	±1	LSBs
Differential Nonlinearity	DNL	No missing codes (T_{MIN} to T_{MAX}) Guaranteed Monotonic	–	–	±0.9	LSBs
Unipolar Offset Error (1)		Uncalibrated	–	±2	±30	LSBs
Bipolar Offset Error (1)		Uncalibrated measured in bipolar mode	–	±2	±30	LSBs
Gain Error		Uncalibrated - External Reference	–	±0.2	±2	%
		Uncalibrated - Internal Reference	–	±2	–	%
Bipolar Gain Error (1)		Uncalibrated - External Reference	–	±0.2	±2	%
		Uncalibrated - Internal Reference	–	±2	–	%
Total Unadjusted Error (Uncalibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	–	±10	–	LSBs
		Deviation from ideal transfer function. Internal reference	–	±20	–	LSBs
Total Unadjusted Error (Calibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	–	±1	±2	LSBs
Calibrated Gain Temperature Coefficient		Variation of FS code with temperature	–	±0.01	–	LSB/°C
DC Common-Mode Reject	$CMRR_{DC}$	$V_N = V_{CM}$ = 0.5V ± 0.5V, $V_P – V_N$ = 100mV	–	70	–	dB
Conversion Rate(2)						
Conversion Time - Continuous	t_{CONV}	Number of CLK cycles	26	–	32	
Conversion Time - Event	t_{CONV}	Number of CLK cycles	–	–	21	
T/H Acquisition Time	t_{ACQ}	Number of CLK cycles	4	–	–	
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	80	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
CLK Duty cycle			40	–	60	%

Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.17 for -3, -2, and -1; and v1.10 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 42 correlates the current status of each Virtex-6 device on a per speed grade basis.

Table 42: **Virtex-6 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6VLX75T			-3, -2, -1, -1L
XC6VLX130T			-3, -2, -1, -1L
XC6VLX195T			-3, -2, -1, -1L
XC6VLX240T			-3, -2, -1, -1L
XC6VLX365T			-3, -2, -1, -1L
XC6VLX550T			-2, -1, -1L
XC6VLX760			-2, -1, -1L
XC6VSX315T			-3, -2, -1, -1L
XC6VSX475T			-2, -1, -1L
XC6VHX250T			-3, -2, -1
XC6VHX255T			-3, -2, -1
XC6VHX380T			-3, -2, -1
XC6VHX565T			-2, -1
XQ6VLX130T			-2, -1, -1L
XQ6VLX240T			-2, -1, -1L
XQ6VLX550T			-1, -1L
XQ6VSX315T			-2, -1, -1L
XQ6VSX475T			-1, -1L

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 devices.

Table 44: **IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
DIFF_SSTL18_I	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
DIFF_SSTL18_I_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL18_II	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
DIFF_SSTL18_II_DCI	0.85	0.94	1.09	1.08	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
DIFF_SSTL18_II_T_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
DIFF_SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns

Table 45: **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices**

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVDS_25	0.94	1.09	1.08	1.54	2.16	1.62	1.54	2.16	1.62	ns
LVDSEXT_25	0.94	1.09	1.08	1.65	2.20	1.73	1.65	2.20	1.73	ns
HT_25	0.94	1.09	1.08	1.62	2.20	1.69	1.62	2.20	1.69	ns
BLVDS_25	0.94	1.09	1.08	1.50	3.18	1.65	1.50	3.18	1.65	ns
RSDS_25 (point to point)	0.94	1.09	1.08	1.54	2.22	1.62	1.54	2.22	1.62	ns
HSTL_I	0.91	1.06	1.06	1.56	2.44	1.71	1.56	2.44	1.71	ns
HSTL_II	0.91	1.06	1.06	1.56	2.21	1.72	1.56	2.21	1.72	ns
HSTL_III	0.91	1.06	1.06	1.54	2.50	1.69	1.54	2.50	1.69	ns
HSTL_I_18	0.91	1.06	1.06	1.58	2.43	1.72	1.58	2.43	1.72	ns
HSTL_II_18	0.91	1.06	1.06	1.62	2.30	1.78	1.62	2.30	1.78	ns
HSTL_III_18	0.91	1.06	1.06	1.54	2.49	1.69	1.54	2.49	1.69	ns
SSTL2_I	0.91	1.06	1.06	1.60	2.50	1.74	1.60	2.50	1.74	ns
SSTL2_II	0.91	1.06	1.06	1.54	2.49	1.71	1.54	2.49	1.71	ns
SSTL15	0.91	1.06	1.06	1.54	2.07	1.69	1.54	2.07	1.69	ns
LVCMOS25, Slow, 2 mA	0.57	0.66	0.70	5.46	6.01	5.63	5.46	6.01	5.63	ns
LVCMOS25, Slow, 4 mA	0.57	0.66	0.70	3.49	3.79	3.65	3.49	3.79	3.65	ns
LVCMOS25, Slow, 6 mA	0.57	0.66	0.70	2.81	3.08	2.95	2.81	3.08	2.95	ns
LVCMOS25, Slow, 8 mA	0.57	0.66	0.70	2.41	2.72	2.59	2.41	2.72	2.59	ns
LVCMOS25, Slow, 12 mA	0.57	0.66	0.70	1.95	2.23	2.10	1.95	2.23	2.10	ns
LVCMOS25, Slow, 16 mA	0.57	0.66	0.70	2.05	2.29	2.21	2.05	2.29	2.21	ns
LVCMOS25, Slow, 24 mA	0.57	0.66	0.70	1.82	2.24	1.98	1.82	2.24	1.98	ns
LVCMOS25, Fast, 2 mA	0.57	0.66	0.70	5.49	6.04	5.62	5.49	6.04	5.62	ns
LVCMOS25, Fast, 4 mA	0.57	0.66	0.70	3.50	3.82	3.65	3.50	3.82	3.65	ns
LVCMOS25, Fast, 6 mA	0.57	0.66	0.70	2.73	2.99	2.88	2.73	2.99	2.88	ns
LVCMOS25, Fast, 8 mA	0.57	0.66	0.70	2.33	2.65	2.53	2.33	2.65	2.53	ns
LVCMOS25, Fast, 12 mA	0.57	0.66	0.70	1.88	2.08	2.03	1.88	2.08	2.03	ns

Table 45: **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
DIFF_SSTL18_II	0.94	1.09	1.08	1.50	2.27	1.66	1.50	2.27	1.66	ns
DIFF_SSTL18_II_DCI	0.94	1.09	1.08	1.47	2.20	1.62	1.47	2.20	1.62	ns
DIFF_SSTL18_II_T_DCI	0.94	1.09	1.08	1.51	2.30	1.65	1.51	2.30	1.65	ns
DIFF_SSTL15	0.91	1.06	1.06	1.54	2.25	1.69	1.54	2.25	1.69	ns
DIFF_SSTL15_DCI	0.91	1.06	1.06	1.52	2.25	1.66	1.52	2.25	1.66	ns
DIFF_SSTL15_T_DCI	0.91	1.06	1.06	1.52	2.25	1.66	1.52	2.25	1.66	ns

Table 46: **IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{IOTPHZ}	T input to Pad high-impedance	0.86	0.92	0.99	0.99	ns

Input Serializer/Deserializer Switching Characteristics

Table 51: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup/Hold for Control Lines							
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.07/ 0.15	0.08/ 0.16	0.09/ 0.17	0.09/ 0.17	0.14/ 0.17	ns
T_{ISCCK_CE} / T_{ISCKC_CE}(2)	CE pin Setup/Hold with respect to CLK (for CE1)	0.20/ 0.03	0.25/ 0.04	0.27/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T_{ISCCK_CE2} / T_{ISCKC_CE2}(2)	CE pin Setup/Hold with respect to CLKDIV (for CE2)	0.01/ 0.27	0.01 0.29	0.01/ 0.31	0.01/ 0.31	–0.05/ 0.35	ns
Setup/Hold for Data Lines							
T_{ISDCK_D} /T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.07/ 0.08	0.08/ 0.09	0.09/ 0.11	0.09/ 0.11	0.11/ 0.19	ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)(1)	0.10/ 0.05	0.12/ 0.06	0.14/ 0.07	0.14/ 0.07	0.16/ 0.15	ns
$T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	0.07/ 0.08	0.08/ 0.09	0.09/ 0.11	0.09/ 0.11	0.11/ 0.19	ns
$T_{ISDCK\_DDLY\_DDR}$ $T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY)(1)	0.10/ 0.05	0.12/ 0.06	0.14/ 0.07	0.14/ 0.07	0.16/ 0.15	ns
Sequential Delays							
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.57	0.66	0.75	0.80	0.88	ns
Propagation Delays							
T_{ISDO_DO}	D input to DO output pin	0.19	0.22	0.25	0.25	0.28	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as T_{ISCCK_CE}/T_{ISCKC_CE} in TRACE report.

Block RAM and FIFO Switching Characteristics

Table 57: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Block RAM and FIFO Clock-to-Out Delays						
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$[1]	Clock CLK to DOUT output (without output register)[2][3]	1.60	1.79	2.08	2.36	ns, Max
	Clock CLK to DOUT output (with output register)[4][5]	0.60	0.66	0.75	0.83	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register)[2][3]	2.62	2.89	3.30	3.73	ns, Max
	Clock CLK to DOUT output with ECC (with output register)[4][5]	0.71	0.77	0.86	0.94	ns, Max
T_{RCKO_CASC} and $T_{RCKO\_CASC\_REG}$	Clock CLK to DOUT output with Cascade (without output register)[2]	2.49	2.77	3.18	3.61	ns, Max
	Clock CLK to DOUT output with Cascade (with output register)[4]	1.29	1.41	1.58	1.79	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs[6]	0.74	0.81	0.91	0.98	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs[7]	0.90	0.98	1.09	1.21	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (with output register)	0.62	0.68	0.76	0.82	ns, Max
	Clock CLK to BITERR (without output register)	2.21	2.46	2.84	3.23	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	0.86	0.94	1.06	1.18	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.73	0.79	0.90	1.00	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.76	0.82	0.92	1.02	ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs[8]	0.47/ 0.27	0.53/ 0.29	0.62/ 0.32	0.66/ 0.34	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs[9]	0.84/ 0.30	0.95/ 0.32	1.11/ 0.34	1.26/ 0.36	ns, Min
$T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode[9]	0.47/ 0.30	0.52/ 0.32	0.59/ 0.34	0.68/ 0.36	ns, Min
	DIN inputs with block RAM ECC encode only[9]	0.68/ 0.30	0.75/ 0.32	0.85/ 0.34	0.97/ 0.36	ns, Min
	DIN inputs with FIFO ECC in standard mode[9]	0.77/ 0.30	0.87/ 0.32	1.02/ 0.34	1.16/ 0.36	ns, Min
$T_{RCCK\_CLK}/T_{RCKC\_CLK}$	Inject single/double bit error in ECC mode	0.90/ 0.27	1.02/ 0.28	1.20/ 0.29	1.56/ 0.29	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	Block RAM Enable (EN) input	0.31/ 0.26	0.35/ 0.27	0.41/ 0.30	0.44/ 0.31	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.18/ 0.25	0.19/ 0.27	0.22/ 0.31	0.24/ 0.33	ns, Min
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	Synchronous RSTREG input	0.22/ 0.23	0.24/ 0.24	0.28/ 0.26	0.31/ 0.27	ns, Min
$T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$	Synchronous RSTRAM input	0.32/ 0.23	0.36/ 0.24	0.41/ 0.27	0.46/ 0.29	ns, Min

Table 57: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{RCCK_WE}/T_{RCKC_WE}	Write Enable (WE) input (Block RAM only)	0.44/ 0.19	0.47/ 0.25	0.52/ 0.35	0.67/ 0.24	ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN FIFO inputs	0.47/ 0.26	0.50/ 0.27	0.55/ 0.30	0.68/ 0.31	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	RDEN FIFO inputs	0.46/ 0.26	0.50/ 0.27	0.55/ 0.30	0.67/ 0.31	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers(10)	0.90	0.98	1.10	1.23	ns, Max
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	FIFO reset timing(11)	0.22/ 0.23	0.24/ 0.24	0.28/ 0.26	0.31/ 0.27	ns, Min
Maximum Frequency						
F_{MAX}	Block RAM in TDP and SDP modes (Write First and No Change modes)	600	540	450	340	MHz
	Block RAM (Read First mode)	525	475	400	275	MHz
	Block RAM (SDP mode)(12)	525	475	400	275	MHz
$F_{MAX\_CASCADE}$	Block RAM Cascade (Write First and No Change modes)	550	490	400	300	MHz
	Block RAM Cascade (Read First mode)	475	425	350	235	MHz
F_{MAX_FIFO}	FIFO in all modes	600	540	450	340	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	450	400	325	250	MHz

Notes:

1. TRACE will report all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. The FIFO reset must be asserted for at least three positive clock edges.
12. When using ISE software v12.4 or later, if the RDADDR_COLLISION_HWCONFIG attribute is set to PERFORMANCE or the block RAM is in single-port operation, then the faster F_{MAX} for WRITE_FIRST/NO_CHANGE modes apply.

Virtex-6 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 65. Values are expressed in nanoseconds unless otherwise noted.

Table 65: **Global Clock Input to Output Delay Without MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* MMCM.							
T_{ICKOF}	Global Clock input and OUTFF *without* MMCM	XC6VLX75T	4.91	5.32	5.88	6.02	ns
		XC6VLX130T	4.89	5.33	6.00	6.13	ns
		XC6VLX195T	5.02	5.46	6.13	6.27	ns
		XC6VLX240T	5.02	5.46	6.13	6.27	ns
		XC6VLX365T	5.30	5.75	6.43	6.37	ns
		XC6VLX550T	N/A	6.02	6.72	6.60	ns
		XC6VLX760	N/A	6.26	6.97	6.87	ns
		XC6VSX315T	5.40	5.85	6.54	6.49	ns
		XC6VSX475T	N/A	6.01	6.71	6.61	ns
		XC6VHX250T	5.18	5.63	6.30	N/A	ns
		XC6VHX255T	5.20	5.66	6.34	N/A	ns
		XC6VHX380T	5.38	5.84	6.53	N/A	ns
		XC6VHX565T	N/A	6.03	6.71	N/A	ns
		XQ6VLX130T	N/A	5.33	6.00	6.13	ns
		XQ6VLX240T	N/A	5.46	6.13	6.27	ns
		XQ6VLX550T	N/A	N/A	6.72	6.60	ns
		XQ6VSX315T	N/A	5.85	6.54	6.49	ns
		XQ6VSX475T	N/A	N/A	6.71	6.61	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 66: **Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM.							
$T_{ICKOFMMCMGC}$	Global Clock Input and OUTFF *with* MMCM	XC6VLX75T	2.34	2.50	2.77	2.85	ns
		XC6VLX130T	2.35	2.51	2.78	2.87	ns
		XC6VLX195T	2.36	2.52	2.79	2.88	ns
		XC6VLX240T	2.36	2.52	2.79	2.88	ns
		XC6VLX365T	2.37	2.53	2.79	2.89	ns
		XC6VLX550T	N/A	2.55	2.82	2.93	ns
		XC6VLX760	N/A	2.54	2.82	2.92	ns
		XC6VSX315T	2.35	2.51	2.79	2.87	ns
		XC6VSX475T	N/A	2.43	2.70	2.79	ns
		XC6VHX250T	2.36	2.53	2.80	N/A	ns
		XC6VHX255T	2.46	2.63	2.91	N/A	ns
		XC6VHX380T	2.39	2.59	2.83	N/A	ns
		XC6VHX565T	N/A	2.54	2.81	N/A	ns
		XQ6VLX130T	N/A	2.51	2.78	2.87	ns
		XQ6VLX240T	N/A	2.52	2.79	2.88	ns
		XQ6VLX550T	N/A	N/A	2.82	2.93	ns
		XQ6VSX315T	N/A	2.51	2.79	2.87	ns
		XQ6VSX475T	N/A	N/A	2.70	2.79	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 67: **Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Clock-capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM.							
$T_{ICKOFMMCMCC}$	Clock-capable Clock Input and OUTFF *with* MMCM	XC6VLX75T	2.22	2.38	2.63	2.72	ns
		XC6VLX130T	2.24	2.39	2.65	2.74	ns
		XC6VLX195T	2.24	2.40	2.65	2.75	ns
		XC6VLX240T	2.24	2.40	2.65	2.75	ns
		XC6VLX365T	2.25	2.42	2.65	2.76	ns
		XC6VLX550T	N/A	2.43	2.68	2.80	ns
		XC6VLX760	N/A	2.42	2.69	2.79	ns
		XC6VSX315T	2.23	2.38	2.65	2.73	ns
		XC6VSX475T	N/A	2.30	2.57	2.66	ns
		XC6VHX250T	2.25	2.41	2.67	N/A	ns
		XC6VHX255T	2.35	2.51	2.78	N/A	ns
		XC6VHX380T	2.27	2.43	2.69	N/A	ns
		XC6VHX565T	N/A	2.41	2.68	N/A	ns
		XQ6VLX130T	N/A	2.39	2.65	2.74	ns
		XQ6VLX240T	N/A	2.40	2.65	2.75	ns
		XQ6VLX550T	N/A	N/A	2.68	2.80	ns
		XQ6VSX315T	N/A	2.38	2.65	2.73	ns
		XQ6VSX475T	N/A	N/A	2.57	2.66	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 69: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
$T_{PSMMCMGC}$/ $T_{PHMMCMGC}$	No Delay Global Clock Input and IFF(2) with MMCM	XC6VLX75T	1.45/ –0.18	1.57/ –0.18	1.72/ –0.18	1.78/ –0.08	ns
		XC6VLX130T	1.53/ –0.18	1.65/ –0.18	1.81/ –0.18	1.87/ –0.07	ns
		XC6VLX195T	1.54/ –0.17	1.66/ –0.17	1.82/ –0.17	1.87/ –0.08	ns
		XC6VLX240T	1.54/ –0.17	1.66/ –0.17	1.82/ –0.17	1.87/ –0.08	ns
		XC6VLX365T	1.55/ –0.18	1.67/ –0.18	1.83/ –0.18	1.87/ –0.07	ns
		XC6VLX550T	N/A	1.84/ –0.17	2.02/ –0.17	2.06/ –0.06	ns
		XC6VLX760	N/A	2.26/ –0.13	2.49/ –0.13	2.06/ –0.03	ns
		XC6VSX315T	1.56/ –0.18	1.68/ –0.18	1.84/ –0.18	1.89/ –0.08	ns
		XC6VSX475T	N/A	1.85/ –0.23	2.03/ –0.23	2.07/ –0.13	ns
		XC6VHX250T	1.52/ –0.17	1.64/ –0.17	1.80/ –0.17	N/A	ns
		XC6VHX255T	1.52/ –0.12	1.64/ –0.12	1.85/ –0.12	N/A	ns
		XC6VHX380T	1.68/ –0.16	1.81/ –0.16	1.99/ –0.16	N/A	ns
		XC6VHX565T	N/A	1.81/ –0.01	1.99/ –0.01	N/A	ns
		XQ6VLX130T	N/A	1.65/ –0.18	1.81/ –0.18	1.87/ –0.07	ns
		XQ6VLX240T	N/A	1.66/ –0.17	1.82/ –0.17	1.87/ –0.08	ns
		XQ6VLX550T	N/A	N/A	2.02/ –0.17	2.06/ –0.06	ns
		XQ6VSX315T	N/A	1.68/ –0.18	1.84/ –0.18	1.89/ –0.08	ns
		XQ6VSX475T	N/A	N/A	2.03/ –0.23	2.07/ –0.13	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 FPGA clock transmitter and receiver data-valid windows.

Table 71: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion(1)	All	0.12	0.12	0.12	0.12	ns
T_{CKSKEW}	Global Clock Tree Skew(2)	XC6VLX75T	0.15	0.16	0.18	0.17	ns
		XC6VLX130T	0.25	0.26	0.29	0.28	ns
		XC6VLX195T	0.26	0.27	0.31	0.30	ns
		XC6VLX240T	0.26	0.27	0.31	0.30	ns
		XC6VLX365T	0.28	0.29	0.31	0.31	ns
		XC6VLX550T	N/A	0.50	0.54	0.54	ns
		XC6VLX760	N/A	0.51	0.56	0.56	ns
		XC6VSX315T	0.27	0.28	0.32	0.30	ns
		XC6VSX475T	N/A	0.39	0.44	0.42	ns
		XC6VHX250T	0.25	0.26	0.29	N/A	ns
		XC6VHX255T	0.35	0.37	0.41	N/A	ns
		XC6VHX380T	0.45	0.47	0.52	N/A	ns
		XC6VHX565T	N/A	0.46	0.51	N/A	ns
		XQ6VLX130T	N/A	0.26	0.29	0.28	ns
		XQ6VLX240T	N/A	0.27	0.31	0.30	ns
		XQ6VLX550T	N/A	N/A	0.54	0.54	ns
		XQ6VSX315T	N/A	0.28	0.32	0.30	ns
		XQ6VSX475T	N/A	N/A	0.44	0.42	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.08	0.08	0.08	0.08	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	0.02	ns
$T_{BUFIOSKEW2}$	I/O clock tree skew across three clock regions	All	0.10	0.12	0.23	0.12	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 72: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC6VLX75T	FF484	95	ps
			FF784	146	ps
		XC6VLX130T	FF484	95	ps
			FF784	146	ps
			FF1156	165	ps
		XC6VLX195T	FF784	145	ps
			FF1156	182	ps
		XC6VLX240T	FF784	146	ps
			FF1156	182	ps
			FF1759	187	ps
		XC6VLX365T	FF1156	189	ps
			FF1759	184	ps
		XC6VLX550T	FF1759	196	ps
			FF1760	249	ps
		XC6VLX760	FF1760	236	ps
		XC6VSX315T	FF1156	168	ps
			FF1759	190	ps
		XC6VSX475T	FF1156	168	ps
			FF1759	204	ps
		XC6VHX250T	FF1154	166	ps
		XC6VHX255T	FF1155	168	ps
			FF1923	228	ps
		XC6VHX380T	FF1154	159	ps
			FF1155	172	ps
			FF1923	227	ps
			FF1924	220	ps
		XC6VHX565T	FF1923	232	ps
			FF1924	197	ps
		XQ6VLX130T	RF784	146	ps
			RF1156	165	ps
			FFG1156	165	ps
		XQ6VLX240T	RF784	146	ps
			RF1156	182	ps
			FFG1156	182	ps
			RF1759	187	ps
		XQ6VLX550T	RF1759	196	ps
		XQ6VSX315T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	190	ps
		XQ6VSX475T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	204	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.