# AMD Xilinx - XC6VLX240T-1FFG1156I Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 18840 |
| Number of Logic Elements/Cells | 241152 |
| Total RAM Bits | 15335424 |
| Number of I/O | 600 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.05V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1156-BBGA, FCBGA |
| Supplier Device Package | 1156-FCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc6vlx240t-1ffg1156i |

*Table 3:* **DC Characteristics Over Recommended Operating Conditions** (1)(2)

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{DRINT}$ | Data retention $V_{CCINT}$ voltage (below which configuration data might be lost) | 0.75 | – | – | V |
| $V_{DRI}$ | Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost) | 2.0 | – | – | V |
| $I_{REF}$ | $V_{REF}$ leakage current per pin | – | – | 10 | µA |
| $I_L$ | Input or output leakage current per pin (sample-tested) | – | – | 10 | µA |
| $C_{IN}$(3) | Die input capacitance at the pad | – | – | 8 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 2.5V | 20 | – | 80 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.8V | 8 | – | 40 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.5V | 5 | – | 30 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.2V | 1 | – | 20 | µA |
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{IN}$ = 2.5V | 3 | – | 80 | µA |
| $I_{BATT}$ | Battery supply current | – | – | 150 | nA |
| n | Temperature diode ideality factor | – | 1.0002 | – | n |
| r | Series resistance | – | 5 | – | Ω |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst case process at 25°C.
3. This measurement represents the die capacitance at the pad, not including the package.

*Table 4:* **Typical Quiescent Supply Current *(Cont'd)***

| Symbol | Description | Device | Speed and Temperature Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | -3 (C) | -2 (C, E, & I) | -1 (C & I) | -1 (I & M)(2) | -1L (C) | -1L (I)(1) | |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current | XC6VLX75T | 1 | 1 | 1 | N/A | 1 | 1 | mA |
| | | XC6VLX130T | 1 | 1 | 1 | N/A | 1 | 1 | mA |
| | | XC6VLX195T | 1 | 1 | 1 | N/A | 1 | 1 | mA |
| | | XC6VLX240T | 2 | 2 | 2 | N/A | 2 | 2 | mA |
| | | XC6VLX365T | 2 | 2 | 2 | N/A | 2 | 2 | mA |
| | | XC6VLX550T(3) | N/A | 3 | 3 | N/A | 3 | 3 | mA |
| | | XC6VLX760(3) | N/A | 3 | 3 | N/A | 3 | 3 | mA |
| | | XC6VSX315T | 2 | 2 | 2 | N/A | 2 | 2 | mA |
| | | XC6VSX475T(3) | N/A | 2 | 2 | N/A | 2 | 2 | mA |
| | | XC6VHX250T | 1 | 1 | 1 | N/A | N/A | N/A | mA |
| | | XC6VHX255T | 1 | 1 | 1 | N/A | N/A | N/A | mA |
| | | XC6VHX380T(4) | 2 | 2 | 2 | N/A | N/A | N/A | mA |
| | | XC6VHX565T(5) | N/A | 2 | 2 | N/A | N/A | N/A | mA |
| | | XQ6VLX130T | N/A | 1 | N/A | 1 | N/A | 1 | mA |
| | | XQ6VLX240T | N/A | 2 | N/A | 2 | N/A | 2 | mA |
| | | XQ6VLX550T(7) | N/A | N/A | N/A | 3 | N/A | 3 | mA |
| | | XQ6VSX315T | N/A | 2 | N/A | 2 | N/A | 2 | mA |
| | | XQ6VSX475T(7) | N/A | N/A | N/A | 2 | N/A | 2 | mA |

*Table 6:* **Power Supply Ramp Time**

| Symbol | Description | Ramp Time | Units |
|---|---|---|---|
| $V_{CCINT}$ | Internal supply voltage relative to GND | 0.20 to 50.0 | ms |
| $V_{CCO}$ | Output drivers supply voltage relative to GND | 0.20 to 50.0 | ms |
| $V_{CCAUX}$ | Auxiliary supply voltage relative to GND | 0.20 to 50.0 | ms |

## SelectIO™ DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $I_{OL}$ and $I_{OH}$ are guaranteed over the recommended operating conditions at the $V_{OL}$ and $V_{OH}$ test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum $V_{CCO}$ with the respective $V_{OL}$ and $V_{OH}$ voltage levels shown. Other standards are sample tested.

*Table 7:* **SelectIO DC Input and Output Levels**

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| LVCMOS25, LVDCI25 | –0.3 | 0.7 | 1.7 | $V_{CCO}$ + 0.3 | 0.4 | $V_{CCO}$ – 0.4 | Note(3) | Note(3) |
| LVCMOS18, LVDCI18 | –0.3 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.3 | 0.45 | $V_{CCO}$ – 0.45 | Note(4) | Note(4) |
| LVCMOS15, LVDCI15 | –0.3 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.3 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | Note(4) | Note(4) |
| LVCMOS12 | –0.3 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.3 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | Note(5) | Note(5) |
| HSTL I_12 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | 6.3 | 6.3 |
| HSTL I(2) | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | 0.4 | $V_{CCO}$ – 0.4 | 8 | –8 |
| HSTL II(2) | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | 0.4 | $V_{CCO}$ – 0.4 | 16 | –16 |
| HSTL III(2) | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | 0.4 | $V_{CCO}$ – 0.4 | 24 | –8 |
| DIFF HSTL I(2) | –0.3 | 50% $V_{CCO}$ – 0.1 | 50% $V_{CCO}$ + 0.1 | $V_{CCO}$ + 0.3 | – | – | – | – |
| DIFF HSTL II(2) | –0.3 | 50% $V_{CCO}$ – 0.1 | 50% $V_{CCO}$ + 0.1 | $V_{CCO}$ + 0.3 | – | – | – | – |
| SSTL2 I | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.61 | $V_{TT}$ + 0.61 | 8.1 | –8.1 |
| SSTL2 II | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.81 | $V_{TT}$ + 0.81 | 16.2 | –16.2 |
| DIFF SSTL2 I | –0.3 | 50% $V_{CCO}$ – 0.15 | 50% $V_{CCO}$ + 0.15 | $V_{CCO}$ + 0.3 | – | – | – | – |
| DIFF SSTL2 II | –0.3 | 50% $V_{CCO}$ – 0.15 | 50% $V_{CCO}$ + 0.15 | $V_{CCO}$ + 0.3 | – | – | – | – |
| SSTL18 I | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.47 | $V_{TT}$ + 0.47 | 6.7 | –6.7 |
| SSTL18 II | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.60 | $V_{TT}$ + 0.60 | 13.4 | –13.4 |
| DIFF SSTL18 I | –0.3 | 50% $V_{CCO}$ – 0.125 | 50% $V_{CCO}$ + 0.125 | $V_{CCO}$ + 0.3 | – | – | – | – |
| DIFF SSTL18 II | –0.3 | 50% $V_{CCO}$ – 0.125 | 50% $V_{CCO}$ + 0.125 | $V_{CCO}$ + 0.3 | – | – | – | – |
| SSTL15 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.175 | $V_{TT}$ + 0.175 | 14.3 | 14.3 |

**Notes:**

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. Supported drive strengths of 2, 4, 6, or 8 mA.
6. For detailed interface specific DC voltage levels, see UG361:*Virtex-6 FPGA SelectIO Resources User Guide*.

## HT DC Specifications (HT_25)

*Table 8:* **HT DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| $V_{OD}$ | Differential Output Voltage for XC devices | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 480 | 600 | 885 | mV |
| | Differential Output Voltage for XQ devices | | 480 | 600 | 930 | mV |
| Δ $V_{OD}$ | Change in $V_{OD}$ Magnitude | | –15 | – | 15 | mV |
| $V_{OCM}$ | Output Common Mode Voltage | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 440 | 600 | 760 | mV |
| Δ $V_{OCM}$ | Change in $V_{OCM}$ Magnitude | | –15 | – | 15 | mV |
| $V_{ID}$ | Input Differential Voltage | | 200 | 600 | 1000 | mV |
| Δ $V_{ID}$ | Change in $V_{ID}$ Magnitude | | –15 | – | 15 | mV |
| $V_{ICM}$ | Input Common Mode Voltage | | 440 | 600 | 780 | mV |
| Δ $V_{ICM}$ | Change in $V_{ICM}$ Magnitude | | –15 | – | 15 | mV |

## LVDS DC Specifications (LVDS_25)

*Table 9:* **LVDS DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| $V_{OH}$ | Output High Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | – | – | 1.675 | V |
| $V_{OL}$ | Output Low Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 0.825 | – | – | V |
| $V_{ODIFF}$ | Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 247 | 350 | 600 | mV |
| $V_{OCM}$ | Output Common-Mode Voltage for XC devices | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.075 | 1.250 | 1.425 | V |
| | Output Common-Mode Voltage for XQ devices | | 1.000 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | | 100 | 350 | 600 | mV |
| $V_{ICM}$ | Input Common-Mode Voltage | | 0.3 | 1.2 | 2.2 | V |

## Extended LVDS DC Specifications (LVDSEXT_25)

*Table 10:* **Extended LVDS DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| $V_{OH}$ | Output High Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | – | – | 1.785 | V |
| $V_{OL}$ | Output Low Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 0.715 | – | – | V |
| $V_{ODIFF}$ | Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High for XC devices | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 350 | – | 840 | mV |
| | Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High for XQ devices | | 350 | – | 850 | mV |
| $V_{OCM}$ | Output Common-Mode Voltage for XC devices | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.075 | 1.250 | 1.425 | V |
| | Output Common-Mode Voltage for XQ devices | | 1.000 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | Common-mode input voltage = 1.25V | 100 | – | 1000 | mV |
| $V_{ICM}$ | Input Common-Mode Voltage | Differential input voltage = ±350 mV | 0.3 | 1.2 | 2.2 | V |

*Table 16:* **GTX Transceiver Quiescent Supply Current (per Lane)** (1)(2)(3)

| Symbol | Description | Typ(4) | Max | Units |
|---|---|---|---|---|
| $I_{MGTAVTTQ}$ | Quiescent MGTAVTT supply current for one GTX transceiver | 0.9 | Note 2 | mA |
| $I_{MGTAVCCQ}$ | Quiescent MGTAVCC supply current for one GTX transceiver | 3.5 | | mA |

**Notes:**

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.
3. GTX transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX transceivers.
4. Typical values are specified at nominal voltage, 25°C.

## GTX Transceiver DC Input and Output Levels

Table 17 summarizes the DC output specifications of the GTX transceivers in Virtex-6 FPGAs. Consult UG366: *Virtex-6 FPGA GTX Transceivers User Guide* for further details.

*Table 17:* **GTX Transceiver DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $DV_{PPIN}$ | Differential peak-to-peak input voltage | External AC coupled ≤ 4.25 Gb/s | 125 | – | 2000 | mV |
| | | External AC coupled > 4.25 Gb/s | 175 | – | 2000 | mV |
| $V_{IN}$ | Absolute input voltage | DC coupled<br>MGTAVTT = 1.2V | –400 | – | MGTAVTT | mV |
| $V_{CMIN}$ | Common mode input voltage | DC coupled<br>MGTAVTT = 1.2V | – | 2/3 MGTAVTT | – | mV |
| $DV_{PPOUT}$ | Differential peak-to-peak output voltage(1) | Transmitter output swing is set to maximum setting | – | – | 1000 | mV |
| $V_{CMOUTDC}$ | DC common mode output voltage. | Equation based | MGTAVTT – $DV_{PPOUT}/4$ | | | mV |
| $R_{IN}$ | Differential input resistance | | 80 | 100 | 130 | Ω |
| $R_{OUT}$ | Differential output resistance | | 80 | 100 | 120 | Ω |
| $T_{OSKEW}$ | Transmitter output pair (TXP and TXN) intra-pair skew | | – | 2 | 8 | ps |
| $C_{EXT}$ | Recommended external AC coupling capacitor(2) | | – | 100 | – | nF |

**Notes:**

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG366: *Virtex-6 FPGA GTX Transceivers User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

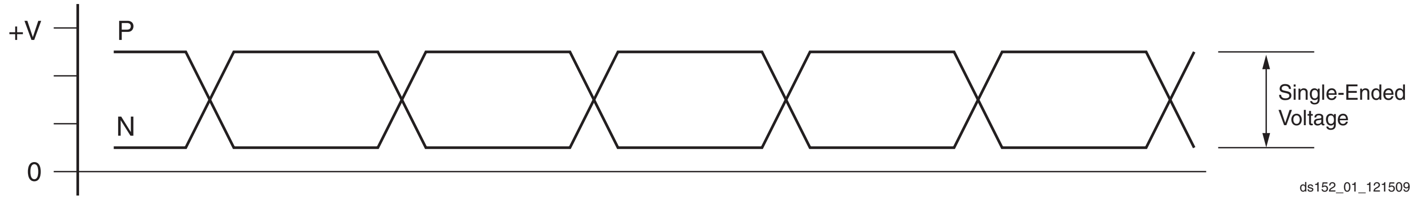

*Figure 1:* **Single-Ended Peak-to-Peak Voltage**

*Table 21:* **GTX Transceiver Reference Clock Switching Characteristics**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $F_{GCLK}$ | Reference clock frequency range | | 62.5 | – | 650 | MHz |
| $T_{RCLK}$ | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| $T_{FCLK}$ | Reference clock fall time | 80% – 20% | – | 200 | – | ps |
| $T_{DCREF}$ | Reference clock duty cycle | Transceiver PLL only | 45 | 50 | 55 | % |
| $T_{LOCK}$ | Clock recovery frequency acquisition time | Initial PLL lock | – | – | 1 | ms |
| $T_{PHASE}$ | Clock recovery phase acquisition time | Lock to data after PLL has locked to the reference clock | – | – | 200 | µs |

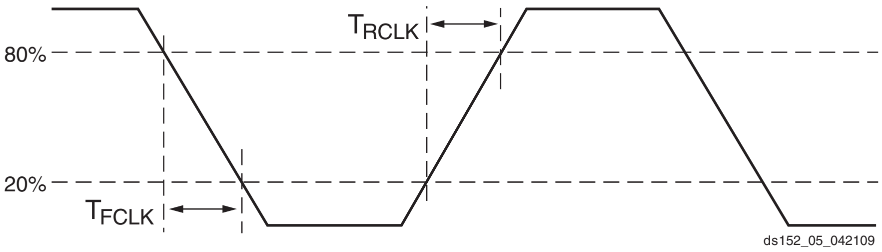

*Figure 3:* **Reference Clock Timing Parameters**

*Table 22:* **GTX Transceiver User Clock Switching Characteristics**(1)

| Symbol | Description | Conditions | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1L | |
| $F_{TXOUT}$ | TXOUTCLK maximum frequency | Internal 20-bit data path | 330 | 330 | 250 | 250 | MHz |
| | | Internal 16-bit data path | 412.5 | 412.5 | 312.5 | 250 | MHz |
| $F_{RXREC}$ | RXRECCLK maximum frequency | Internal 20-bit data path | 330 | 330 | 250 | 250 | MHz |
| | | Internal 16-bit data path | 412.5 | 412.5 | 312.5 | 250 | MHz |
| $T_{RX}$ | RXUSRCLK maximum frequency | | 412.5(2) | 412.5(2) | 312.5 | 250 | MHz |
| $T_{RX2}$ | RXUSRCLK2 maximum frequency | 1 byte interface | 376 | 376 | 312.5 | 250 | MHz |
| | | 2 byte interface | 406.25 | 406.25 | 312.5 | 250 | MHz |
| | | 4 byte interface | 206.25 | 206.25 | 156.25 | 125 | MHz |
| $T_{TX}$ | TXUSRCLK maximum frequency | | 412.5(3) | 412.5(3) | 312.5 | 250 | MHz |
| $T_{TX2}$ | TXUSRCLK2 maximum frequency | 1 byte interface | 376 | 376 | 312.5 | 250 | MHz |
| | | 2 byte interface | 406.25 | 406.25 | 312.5 | 250 | MHz |
| | | 4 byte interface | 206.25 | 206.25 | 156.25 | 125 | MHz |

**Notes:**

1. Clocking must be implemented as described in UG366:*Virtex-6 FPGA GTX Transceivers User Guide*.
2. 406.25 MHz when the RX elastic buffer is bypassed.
3. 406.25 MHz when the TX buffer is bypassed.

*Table 23:* **GTX Transceiver Transmitter Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTXTX}$ | Serial data rate range | | 0.480 | – | $F_{GTXMAX}$ | Gb/s |
| $T_{RTX}$ | TX Rise time | 20%–80% | – | 120 | – | ps |
| $T_{FTX}$ | TX Fall time | 80%–20% | – | 120 | – | ps |
| $T_{LLSKEW}$ | TX lane-to-lane skew(1) | | – | – | 350 | ps |
| $V_{TXOOBVDPP}$ | Electrical idle amplitude | | – | – | 15 | mV |
| $T_{TXOOBTRANSITION}$ | Electrical idle transition time | | – | – | 75 | ns |
| $TJ_{6.5}$ | Total Jitter(2)(3) | 6.5 Gb/s | – | – | 0.33 | UI |
| $DJ_{6.5}$ | Deterministic Jitter(2)(3) | | – | – | 0.17 | UI |
| $TJ_{5.0}$ | Total Jitter(2)(3) | 5.0 Gb/s | – | – | 0.33 | UI |
| $DJ_{5.0}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{4.25}$ | Total Jitter(2)(3) | 4.25 Gb/s | – | – | 0.33 | UI |
| $DJ_{4.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.14 | UI |
| $TJ_{3.75}$ | Total Jitter(2)(3) | 3.75 Gb/s | – | – | 0.34 | UI |
| $DJ_{3.75}$ | Deterministic Jitter(2)(3) | | – | – | 0.16 | UI |
| $TJ_{3.125}$ | Total Jitter(2)(3) | 3.125 Gb/s | – | – | 0.2 | UI |
| $DJ_{3.125}$ | Deterministic Jitter(2)(3) | | – | – | 0.1 | UI |
| $TJ_{3.125L}$ | Total Jitter(2)(3) | 3.125 Gb/s(4) | – | – | 0.35 | UI |
| $DJ_{3.125L}$ | Deterministic Jitter(2)(3) | | – | – | 0.16 | UI |
| $TJ_{2.5}$ | Total Jitter(2)(3) | 2.5 Gb/s(5) | – | – | 0.20 | UI |
| $DJ_{2.5}$ | Deterministic Jitter(2)(3) | | – | – | 0.08 | UI |
| $TJ_{1.25}$ | Total Jitter(2)(3) | 1.25 Gb/s(6) | – | – | 0.15 | UI |
| $DJ_{1.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.06 | UI |
| $TJ_{600}$ | Total Jitter(2)(3) | 600 Mb/s | – | – | 0.1 | UI |
| $DJ_{600}$ | Deterministic Jitter(2)(3) | | – | – | 0.03 | UI |
| $TJ_{480}$ | Total Jitter(2)(3) | 480 Mb/s | – | – | 0.1 | UI |
| $DJ_{480}$ | Deterministic Jitter(2)(3) | | – | – | 0.03 | UI |

**Notes:**

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
2. Using PLL_DIVSEL_FB = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 1.5625 GHz and OUTDIV = 1.
5. PLL frequency at 2.5 GHz and OUTDIV = 2.
6. PLL frequency at 2.5 GHz and OUTDIV = 4.

# GTH Transceiver Specifications

## GTH Transceiver DC Characteristics

*Table 25:* **Absolute Maximum Ratings for GTH Transceivers(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| MGTHAVCC | Analog supply voltage for the GTH transmitter, receiver, and common analog circuits | –0.5 | 1.125 | V |
| MGTHAVCCRX | Analog supply voltage for the GTH receiver circuits and common analog circuits | –0.5 | 1.125 | V |
| MGTHAVTT | Analog supply voltage for the GTH transmitter termination circuits | –0.5 | 1.32 | V |
| MGTHAVCCPLL | Analog supply voltage for the GTH receiver and PLL circuits | –0.5 | 1.935 | V |
| $V_{IN}$ | Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage | –0.5 | 1.125 | V |
| $V_{MGTREFCLK}$ | Reference clock absolute input voltage | –0.5 | 1.935 | V |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

*Table 26:* **Recommended Operating Conditions for GTH Transceivers (1)(2)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| MGTHAVCC | Analog supply voltage for the GTH transmitter, receiver, and common analog circuits | 1.075 | 1.1 | 1.125 | V |
| MGTHAVCCRX | Analog supply voltage for the GTH receiver circuits and common analog circuits | 1.075 | 1.1 | 1.125 | V |
| MGTHAVTT | Analog supply voltage for the GTH transmitter termination circuits | 1.140 | 1.2 | 1.26 | V |
| MGTHAVCCPLL | Analog supply voltage for the GTH receiver and PLL circuit | 1.710 | 1.8 | 1.89 | V |

**Notes:**

1. Each voltage listed requires the filter circuit described in UG371: *Virtex-6 FPGA GTH Transceivers User Guide*.
2. Voltages are specified for the temperature range of $T_j$ = –40°C to +100°C.

*Table 27:* **GTH Transceiver Power Supply Sequencing (1)(2)(3)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{HAVCC2HAVCCRX}$ | Maximum time between powering MGTHAVCC to when MGTHAVCCRX must be powered. | 0 | 5 | ms |
| $T_{HAVCCRX2HAVCCPLL}$ | Minimum time between powering MGTHAVCCRX to when MGTHAVCCPLL can be powered. | 10 | – | µs |
| $T_{HAVCCRX2HAVTT}$ | Minimum time between powering MGTHAVCCRX to when MGTHAVTT can be powered. | 10 | – | µs |

**Notes:**

1. MGTHAVCCRX must be powered simultaneously or within $T_{HAVCC2HAVCCRX}$ of MGTHAVCC, but it must not precede MGTHAVCC.
2. MGTHAVCC and MGTHAVCCRX must be powered before MGTHAVCCPLL and MGTHAVTT. This minimum time is defined by $T_{HAVCCRX2HAVCCPLL}$ and $T_{HAVCCRX2HAVTT}$.
3. At any time, the condition of MGTHAVCC being present and MGTHAVCCRX not being present should not occur for more than the maximum $T_{HAVCC2HAVCCRX}$.

## GTH Transceiver DC Input and Output Levels

Table 30 summarizes the DC output specifications of the GTH transceivers in Virtex-6 FPGAs. Consult UG371: *Virtex-6 FPGA GTH Transceivers User Guide* for further details.

*Table 30:* **GTH Transceiver DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $D_{VPPIN}$ | Differential peak-to-peak input voltage | External AC coupled | 175 | – | 1200 | mV |
| $D_{VPPOUT}$ | Differential peak-to-peak output voltage(1) | Transmitter output swing is set to maximum setting | 800 | – | 1200 | mV |
| $R_{IN}$ | Differential input resistance | | 80 | 100 | 120 | Ω |
| $R_{OUT}$ | Differential output resistance | | 80 | 100 | 120 | Ω |
| $T_{OSKEW}$ | Transmitter output pair (TXP and TXN) intra-pair skew | | – | 2 | – | ps |
| $C_{EXT}$ | Recommended external AC coupling capacitor(2) | | – | 100 | – | nF |

**Notes:**

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG371: *Virtex-6 FPGA GTH Transceivers User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 31 summarizes the DC specifications of the clock input of the GTH transceiver. Consult UG371: *Virtex-6 FPGA GTH Transceivers User Guide* for further details.

*Table 31:* **GTH Transceiver Clock DC Input Level Specification**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage | ≤ 600 MHz | 500 | – | 1600 | mV |
| | | > 600 MHz | 600 | – | 1600 | mV |
| $R_{IN}$ | Differential input resistance | | 80 | 100 | 120 | Ω |
| $C_{EXT}$ | Required external AC coupling capacitor | | – | 100 | – | nF |

## GTH Transceiver Switching Characteristics

Consult UG371: *Virtex-6 FPGA GTH Transceivers User Guide* for further information.

*Table 32:* **GTH Transceiver Maximum Data Rate and PLL Frequency Range**

| Symbol | Description | Conditions | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | |
| $F_{GTHMAX}$ | Maximum GTH transceiver data rate | PLL Output Divider = 1 | 11.182 | 11.182 | 10.32 | Gb/s |
| | | PLL Output Divider = 4 | 2.795 | 2.795 | 2.58 | Gb/s |
| $F_{GTHMIN}$ | Minimum GTH transceiver data rate(1) | PLL Output Divider = 1 | 9.92 | 9.92 | 9.92 | Gb/s |
| | | PLL Output Divider = 4 | 2.48 | 2.48 | 2.48 | Gb/s |
| $F_{GPLLMAX}$ | Maximum GTH PLL frequency | | 5.591 | 5.591 | 5.16 | GHz |
| $F_{GPLLMIN}$ | Minimum GTH PLL frequency | | 4.96 | 4.96 | 4.96 | GHz |

**Notes:**

1. Lower data rates can be achieved using FPGA logic based oversampling designs.

*Table 33:* **GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1 | |
| $F_{GTHDRPCLK}$ | GTHDRPCLK maximum frequency | 70 | 70 | 60 | MHz |

*Table 34:* **GTH Transceiver Reference Clock Switching Characteristics**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $F_{GCLK}$ | Reference clock frequency range | -1 speed grade | 150 | – | 645 | MHz |
| | | -2 and -3 speed grades | 150 | – | 700 | MHz |
| $T_{RCLK}$ | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| $T_{FCLK}$ | Reference clock fall time | 80% – 20% | – | 200 | – | ps |
| $T_{DCREF}$ | Reference clock duty cycle | CLK | 45 | 50 | 55 | % |
| $T_{LOCK}$ | Clock recovery frequency acquisition time | Initial PLL lock | – | – | 2 | ms |
| $T_{PHASE}$ | Clock recovery phase acquisition time | Lock to data after PLL has locked to the reference clock | – | – | 20 | µs |

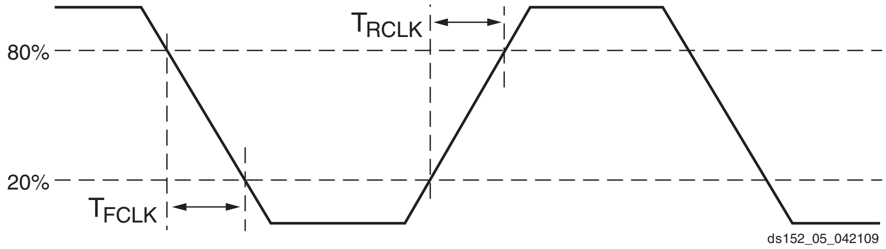

*Figure 5:* **Reference Clock Timing Parameters**

## Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.17 for -3, -2, and -1; and v1.10 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

### Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 42 correlates the current status of each Virtex-6 device on a per speed grade basis.

*Table 42:* **Virtex-6 Device Speed Grade Designations**

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XC6VLX75T | | | -3, -2, -1, -1L |
| XC6VLX130T | | | -3, -2, -1, -1L |
| XC6VLX195T | | | -3, -2, -1, -1L |
| XC6VLX240T | | | -3, -2, -1, -1L |
| XC6VLX365T | | | -3, -2, -1, -1L |
| XC6VLX550T | | | -2, -1, -1L |
| XC6VLX760 | | | -2, -1, -1L |
| XC6VSX315T | | | -3, -2, -1, -1L |
| XC6VSX475T | | | -2, -1, -1L |
| XC6VHX250T | | | -3, -2, -1 |
| XC6VHX255T | | | -3, -2, -1 |
| XC6VHX380T | | | -3, -2, -1 |
| XC6VHX565T | | | -2, -1 |
| XQ6VLX130T | | | -2, -1, -1L |
| XQ6VLX240T | | | -2, -1, -1L |
| XQ6VLX550T | | | -1, -1L |
| XQ6VSX315T | | | -2, -1, -1L |
| XQ6VSX475T | | | -1, -1L |

## Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 devices.

## IOB Pad Input/Output/3-State Switching Characteristics

Table 44 (for commercial (XC) Virtex-6 devices) and Table 45 (for the Defense-grade (XQ) Virtex-6 devices) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

$T_{IOPI}$ is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

$T_{IOOP}$ is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

$T_{IOTP}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 46 summarizes the value of $T_{IOTPHZ}$. $T_{IOTPHZ}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

*Table 44:* **IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices**

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | |
| LVDS_25 | 0.85 | 0.94 | 1.09 | 1.08 | 1.45 | 1.54 | 1.68 | 1.62 | 1.45 | 1.54 | 1.68 | 1.62 | ns |
| LVDSEXT_25 | 0.85 | 0.94 | 1.09 | 1.08 | 1.53 | 1.65 | 1.84 | 1.73 | 1.53 | 1.65 | 1.84 | 1.73 | ns |
| HT_25 | 0.85 | 0.94 | 1.09 | 1.08 | 1.51 | 1.62 | 1.78 | 1.69 | 1.51 | 1.62 | 1.78 | 1.69 | ns |
| BLVDS_25 | 0.85 | 0.94 | 1.09 | 1.08 | 1.39 | 1.50 | 1.67 | 1.65 | 1.39 | 1.50 | 1.67 | 1.65 | ns |
| RSDS_25 (point to point) | 0.85 | 0.94 | 1.09 | 1.08 | 1.45 | 1.54 | 1.68 | 1.62 | 1.45 | 1.54 | 1.68 | 1.62 | ns |
| HSTL_I | 0.81 | 0.91 | 1.06 | 1.06 | 1.45 | 1.56 | 1.73 | 1.71 | 1.45 | 1.56 | 1.73 | 1.71 | ns |
| HSTL_II | 0.81 | 0.91 | 1.06 | 1.06 | 1.44 | 1.56 | 1.74 | 1.72 | 1.44 | 1.56 | 1.74 | 1.72 | ns |
| HSTL_III | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.71 | 1.69 | 1.42 | 1.54 | 1.71 | 1.69 | ns |
| HSTL_I_18 | 0.81 | 0.91 | 1.06 | 1.06 | 1.47 | 1.58 | 1.75 | 1.72 | 1.47 | 1.58 | 1.75 | 1.72 | ns |
| HSTL_II_18 | 0.81 | 0.91 | 1.06 | 1.06 | 1.50 | 1.62 | 1.81 | 1.78 | 1.50 | 1.62 | 1.81 | 1.78 | ns |
| HSTL_III_18 | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.71 | 1.69 | 1.42 | 1.54 | 1.71 | 1.69 | ns |
| SSTL2_I | 0.81 | 0.91 | 1.06 | 1.06 | 1.49 | 1.60 | 1.77 | 1.74 | 1.49 | 1.60 | 1.77 | 1.74 | ns |
| SSTL2_II | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.72 | 1.71 | 1.42 | 1.54 | 1.72 | 1.71 | ns |
| SSTL15 | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.71 | 1.69 | 1.42 | 1.54 | 1.71 | 1.69 | ns |
| LVCMOS25, Slow, 2 mA | 0.51 | 0.57 | 0.66 | 0.70 | 5.09 | 5.46 | 6.01 | 5.63 | 5.09 | 5.46 | 6.01 | 5.63 | ns |
| LVCMOS25, Slow, 4 mA | 0.51 | 0.57 | 0.66 | 0.70 | 3.30 | 3.49 | 3.79 | 3.65 | 3.30 | 3.49 | 3.79 | 3.65 | ns |
| LVCMOS25, Slow, 6 mA | 0.51 | 0.57 | 0.66 | 0.70 | 2.62 | 2.81 | 3.08 | 2.95 | 2.62 | 2.81 | 3.08 | 2.95 | ns |
| LVCMOS25, Slow, 8 mA | 0.51 | 0.57 | 0.66 | 0.70 | 2.21 | 2.41 | 2.72 | 2.59 | 2.21 | 2.41 | 2.72 | 2.59 | ns |
| LVCMOS25, Slow, 12 mA | 0.51 | 0.57 | 0.66 | 0.70 | 1.80 | 1.95 | 2.17 | 2.10 | 1.80 | 1.95 | 2.17 | 2.10 | ns |
| LVCMOS25, Slow, 16 mA | 0.51 | 0.57 | 0.66 | 0.70 | 1.89 | 2.05 | 2.29 | 2.21 | 1.89 | 2.05 | 2.29 | 2.21 | ns |
| LVCMOS25, Slow, 24 mA | 0.51 | 0.57 | 0.66 | 0.70 | 1.68 | 1.82 | 2.02 | 1.98 | 1.68 | 1.82 | 2.02 | 1.98 | ns |
| LVCMOS25, Fast, 2 mA | 0.51 | 0.57 | 0.66 | 0.70 | 5.12 | 5.49 | 6.04 | 5.62 | 5.12 | 5.49 | 6.04 | 5.62 | ns |
| LVCMOS25, Fast, 4 mA | 0.51 | 0.57 | 0.66 | 0.70 | 3.28 | 3.50 | 3.82 | 3.65 | 3.28 | 3.50 | 3.82 | 3.65 | ns |
| LVCMOS25, Fast, 6 mA | 0.51 | 0.57 | 0.66 | 0.70 | 2.56 | 2.73 | 2.99 | 2.88 | 2.56 | 2.73 | 2.99 | 2.88 | ns |
| LVCMOS25, Fast, 8 mA | 0.51 | 0.57 | 0.66 | 0.70 | 2.11 | 2.33 | 2.65 | 2.53 | 2.11 | 2.33 | 2.65 | 2.53 | ns |
| LVCMOS25, Fast, 12 mA | 0.51 | 0.57 | 0.66 | 0.70 | 1.74 | 1.88 | 2.08 | 2.03 | 1.74 | 1.88 | 2.08 | 2.03 | ns |
| LVCMOS25, Fast, 16 mA | 0.51 | 0.57 | 0.66 | 0.70 | 1.77 | 1.92 | 2.13 | 2.08 | 1.77 | 1.92 | 2.13 | 2.08 | ns |

*Table 44:* **IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | |
| DIFF_SSTL18_I | 0.85 | 0.94 | 1.09 | 1.08 | 1.47 | 1.58 | 1.75 | 1.73 | 1.47 | 1.58 | 1.75 | 1.73 | ns |
| DIFF_SSTL18_I_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.40 | 1.51 | 1.67 | 1.65 | 1.40 | 1.51 | 1.67 | 1.65 | ns |
| DIFF_SSTL18_II | 0.85 | 0.94 | 1.09 | 1.08 | 1.39 | 1.50 | 1.67 | 1.66 | 1.39 | 1.50 | 1.67 | 1.66 | ns |
| DIFF_SSTL18_II_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.36 | 1.47 | 1.63 | 1.62 | 1.36 | 1.47 | 1.63 | 1.62 | ns |
| DIFF_SSTL18_II_T_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.40 | 1.51 | 1.67 | 1.65 | 1.40 | 1.51 | 1.67 | 1.65 | ns |
| DIFF_SSTL15 | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.71 | 1.69 | 1.42 | 1.54 | 1.71 | 1.69 | ns |
| DIFF_SSTL15_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.41 | 1.52 | 1.68 | 1.66 | 1.41 | 1.52 | 1.68 | 1.66 | ns |
| DIFF_SSTL15_T_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.41 | 1.52 | 1.68 | 1.66 | 1.41 | 1.52 | 1.68 | 1.66 | ns |

*Table 45:* **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices**

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| LVDS_25 | 0.94 | 1.09 | 1.08 | 1.54 | 2.16 | 1.62 | 1.54 | 2.16 | 1.62 | ns |
| LVDSEXT_25 | 0.94 | 1.09 | 1.08 | 1.65 | 2.20 | 1.73 | 1.65 | 2.20 | 1.73 | ns |
| HT_25 | 0.94 | 1.09 | 1.08 | 1.62 | 2.20 | 1.69 | 1.62 | 2.20 | 1.69 | ns |
| BLVDS_25 | 0.94 | 1.09 | 1.08 | 1.50 | 3.18 | 1.65 | 1.50 | 3.18 | 1.65 | ns |
| RSDS_25 (point to point) | 0.94 | 1.09 | 1.08 | 1.54 | 2.22 | 1.62 | 1.54 | 2.22 | 1.62 | ns |
| HSTL_I | 0.91 | 1.06 | 1.06 | 1.56 | 2.44 | 1.71 | 1.56 | 2.44 | 1.71 | ns |
| HSTL_II | 0.91 | 1.06 | 1.06 | 1.56 | 2.21 | 1.72 | 1.56 | 2.21 | 1.72 | ns |
| HSTL_III | 0.91 | 1.06 | 1.06 | 1.54 | 2.50 | 1.69 | 1.54 | 2.50 | 1.69 | ns |
| HSTL_I_18 | 0.91 | 1.06 | 1.06 | 1.58 | 2.43 | 1.72 | 1.58 | 2.43 | 1.72 | ns |
| HSTL_II_18 | 0.91 | 1.06 | 1.06 | 1.62 | 2.30 | 1.78 | 1.62 | 2.30 | 1.78 | ns |
| HSTL_III_18 | 0.91 | 1.06 | 1.06 | 1.54 | 2.49 | 1.69 | 1.54 | 2.49 | 1.69 | ns |
| SSTL2_I | 0.91 | 1.06 | 1.06 | 1.60 | 2.50 | 1.74 | 1.60 | 2.50 | 1.74 | ns |
| SSTL2_II | 0.91 | 1.06 | 1.06 | 1.54 | 2.49 | 1.71 | 1.54 | 2.49 | 1.71 | ns |
| SSTL15 | 0.91 | 1.06 | 1.06 | 1.54 | 2.07 | 1.69 | 1.54 | 2.07 | 1.69 | ns |
| LVCMOS25, Slow, 2 mA | 0.57 | 0.66 | 0.70 | 5.46 | 6.01 | 5.63 | 5.46 | 6.01 | 5.63 | ns |
| LVCMOS25, Slow, 4 mA | 0.57 | 0.66 | 0.70 | 3.49 | 3.79 | 3.65 | 3.49 | 3.79 | 3.65 | ns |
| LVCMOS25, Slow, 6 mA | 0.57 | 0.66 | 0.70 | 2.81 | 3.08 | 2.95 | 2.81 | 3.08 | 2.95 | ns |
| LVCMOS25, Slow, 8 mA | 0.57 | 0.66 | 0.70 | 2.41 | 2.72 | 2.59 | 2.41 | 2.72 | 2.59 | ns |
| LVCMOS25, Slow, 12 mA | 0.57 | 0.66 | 0.70 | 1.95 | 2.23 | 2.10 | 1.95 | 2.23 | 2.10 | ns |
| LVCMOS25, Slow, 16 mA | 0.57 | 0.66 | 0.70 | 2.05 | 2.29 | 2.21 | 2.05 | 2.29 | 2.21 | ns |
| LVCMOS25, Slow, 24 mA | 0.57 | 0.66 | 0.70 | 1.82 | 2.24 | 1.98 | 1.82 | 2.24 | 1.98 | ns |
| LVCMOS25, Fast, 2 mA | 0.57 | 0.66 | 0.70 | 5.49 | 6.04 | 5.62 | 5.49 | 6.04 | 5.62 | ns |
| LVCMOS25, Fast, 4 mA | 0.57 | 0.66 | 0.70 | 3.50 | 3.82 | 3.65 | 3.50 | 3.82 | 3.65 | ns |
| LVCMOS25, Fast, 6 mA | 0.57 | 0.66 | 0.70 | 2.73 | 2.99 | 2.88 | 2.73 | 2.99 | 2.88 | ns |
| LVCMOS25, Fast, 8 mA | 0.57 | 0.66 | 0.70 | 2.33 | 2.65 | 2.53 | 2.33 | 2.65 | 2.53 | ns |
| LVCMOS25, Fast, 12 mA | 0.57 | 0.66 | 0.70 | 1.88 | 2.08 | 2.03 | 1.88 | 2.08 | 2.03 | ns |

*Table 45:* **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| LVCMOS25, Fast, 16 mA | 0.57 | 0.66 | 0.70 | 1.92 | 2.15 | 2.08 | 1.92 | 2.15 | 2.08 | ns |
| LVCMOS25, Fast, 24 mA | 0.57 | 0.66 | 0.70 | 1.79 | 2.15 | 1.96 | 1.79 | 2.15 | 1.96 | ns |
| LVCMOS18, Slow, 2 mA | 0.61 | 0.71 | 0.73 | 4.47 | 4.87 | 4.30 | 4.47 | 4.87 | 4.30 | ns |
| LVCMOS18, Slow, 4 mA | 0.61 | 0.71 | 0.73 | 2.96 | 3.21 | 2.94 | 2.96 | 3.21 | 2.94 | ns |
| LVCMOS18, Slow, 6 mA | 0.61 | 0.71 | 0.73 | 2.43 | 2.64 | 2.47 | 2.43 | 2.64 | 2.47 | ns |
| LVCMOS18, Slow, 8 mA | 0.61 | 0.71 | 0.73 | 2.11 | 2.41 | 2.24 | 2.11 | 2.41 | 2.24 | ns |
| LVCMOS18, Slow, 12 mA | 0.61 | 0.71 | 0.73 | 1.99 | 2.30 | 2.10 | 1.99 | 2.30 | 2.10 | ns |
| LVCMOS18, Slow, 16 mA | 0.61 | 0.71 | 0.73 | 1.95 | 2.30 | 2.04 | 1.95 | 2.30 | 2.04 | ns |
| LVCMOS18, Fast, 2 mA | 0.61 | 0.71 | 0.73 | 4.23 | 4.57 | 4.08 | 4.23 | 4.57 | 4.08 | ns |
| LVCMOS18, Fast, 4 mA | 0.61 | 0.71 | 0.73 | 2.76 | 2.97 | 2.74 | 2.76 | 2.97 | 2.74 | ns |
| LVCMOS18, Fast, 6 mA | 0.61 | 0.71 | 0.73 | 2.28 | 2.46 | 2.32 | 2.28 | 2.46 | 2.32 | ns |
| LVCMOS18, Fast, 8 mA | 0.61 | 0.71 | 0.73 | 1.99 | 2.34 | 2.14 | 1.99 | 2.34 | 2.14 | ns |
| LVCMOS18, Fast, 12 mA | 0.61 | 0.71 | 0.73 | 1.80 | 2.19 | 1.88 | 1.80 | 2.19 | 1.88 | ns |
| LVCMOS18, Fast, 16 mA | 0.61 | 0.71 | 0.73 | 1.74 | 2.18 | 1.88 | 1.74 | 2.18 | 1.88 | ns |
| LVCMOS15, Slow, 2 mA | 0.73 | 0.85 | 0.85 | 3.77 | 4.29 | 3.91 | 3.77 | 4.29 | 3.91 | ns |
| LVCMOS15, Slow, 4 mA | 0.73 | 0.85 | 0.85 | 2.79 | 3.10 | 2.93 | 2.79 | 3.10 | 2.93 | ns |
| LVCMOS15, Slow, 6 mA | 0.73 | 0.85 | 0.85 | 2.32 | 2.68 | 2.50 | 2.32 | 2.68 | 2.50 | ns |
| LVCMOS15, Slow, 8 mA | 0.73 | 0.85 | 0.85 | 1.98 | 2.29 | 2.24 | 1.98 | 2.29 | 2.24 | ns |
| LVCMOS15, Slow, 12 mA | 0.73 | 0.85 | 0.85 | 1.91 | 2.23 | 2.07 | 1.91 | 2.23 | 2.07 | ns |
| LVCMOS15, Slow, 16 mA | 0.73 | 0.85 | 0.85 | 1.83 | 2.23 | 1.98 | 1.83 | 2.23 | 1.98 | ns |
| LVCMOS15, Fast, 2 mA | 0.73 | 0.85 | 0.85 | 3.77 | 4.28 | 3.91 | 3.77 | 4.28 | 3.91 | ns |
| LVCMOS15, Fast, 4 mA | 0.73 | 0.85 | 0.85 | 2.53 | 2.78 | 2.66 | 2.53 | 2.78 | 2.66 | ns |
| LVCMOS15, Fast, 6 mA | 0.73 | 0.85 | 0.85 | 2.05 | 2.42 | 2.16 | 2.05 | 2.42 | 2.16 | ns |
| LVCMOS15, Fast, 8 mA | 0.73 | 0.85 | 0.85 | 1.90 | 2.20 | 2.04 | 1.90 | 2.20 | 2.04 | ns |
| LVCMOS15, Fast, 12 mA | 0.73 | 0.85 | 0.85 | 1.77 | 2.11 | 1.90 | 1.77 | 2.11 | 1.90 | ns |
| LVCMOS15, Fast, 16 mA | 0.73 | 0.85 | 0.85 | 1.76 | 2.11 | 1.92 | 1.76 | 2.11 | 1.92 | ns |
| LVCMOS12, Slow, 2 mA | 0.81 | 0.93 | 0.95 | 3.39 | 3.75 | 3.54 | 3.39 | 3.75 | 3.54 | ns |
| LVCMOS12, Slow, 4 mA | 0.81 | 0.93 | 0.95 | 2.63 | 2.93 | 2.79 | 2.63 | 2.93 | 2.79 | ns |
| LVCMOS12, Slow, 6 mA | 0.81 | 0.93 | 0.95 | 2.11 | 2.67 | 2.26 | 2.11 | 2.67 | 2.26 | ns |
| LVCMOS12, Slow, 8 mA | 0.81 | 0.93 | 0.95 | 2.02 | 2.25 | 2.17 | 2.02 | 2.25 | 2.17 | ns |
| LVCMOS12, Fast, 2 mA | 0.81 | 0.93 | 0.95 | 2.98 | 3.39 | 3.11 | 2.98 | 3.39 | 3.11 | ns |
| LVCMOS12, Fast, 4 mA | 0.81 | 0.93 | 0.95 | 2.16 | 2.70 | 2.31 | 2.16 | 2.70 | 2.31 | ns |
| LVCMOS12, Fast, 6 mA | 0.81 | 0.93 | 0.95 | 1.89 | 2.34 | 2.05 | 1.89 | 2.34 | 2.05 | ns |
| LVCMOS12, Fast, 8 mA | 0.81 | 0.93 | 0.95 | 1.82 | 2.10 | 1.98 | 1.82 | 2.10 | 1.98 | ns |
| LVDCI_25 | 0.57 | 0.70 | 0.70 | 2.14 | 2.82 | 2.26 | 2.14 | 2.82 | 2.26 | ns |
| LVDCI_18 | 0.61 | 0.71 | 0.73 | 2.23 | 2.78 | 2.38 | 2.23 | 2.78 | 2.38 | ns |
| LVDCI_15 | 0.73 | 0.85 | 0.85 | 2.01 | 2.75 | 2.18 | 2.01 | 2.75 | 2.18 | ns |
| LVDCI_DV2_25 | 0.57 | 0.70 | 0.70 | 1.83 | 2.37 | 2.00 | 1.83 | 2.37 | 2.00 | ns |

# I/O Standard Adjustment Measurement Methodology

## Input Delay Measurements

Table 47 shows the test setup parameters used for measuring input delay.

*Table 47:* **Input Delay Measurement Methodology**

| Description | I/O Standard Attribute | $V_L$ (1)(2) | $V_H$ (1)(2) | $V_{MEAS}$ (1)(4)(5) | $V_{REF}$ (1)(3)(5) |
|---|---|---|---|---|---|
| LVCMOS, 2.5V | LVCMOS25 | 0 | 2.5 | 1.25 | – |
| LVCMOS, 1.8V | LVCMOS18 | 0 | 1.8 | 0.9 | – |
| LVCMOS, 1.5V | LVCMOS15 | 0 | 1.5 | 0.75 | – |
| HSTL (High-Speed Transceiver Logic), Class I & II | HSTL_I, HSTL_II | $V_{REF} – 0.5$ | $V_{REF} + 0.5$ | $V_{REF}$ | 0.75 |
| HSTL, Class III | HSTL_III | $V_{REF} – 0.5$ | $V_{REF} + 0.5$ | $V_{REF}$ | 0.90 |
| HSTL, Class I & II, 1.8V | HSTL_I_18, HSTL_II_18 | $V_{REF} – 0.5$ | $V_{REF} + 0.5$ | $V_{REF}$ | 0.90 |
| HSTL, Class III 1.8V | HSTL_III_18 | $V_{REF} – 0.5$ | $V_{REF} + 0.5$ | $V_{REF}$ | 1.08 |
| SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V | SSTL3_I, SSTL3_II | $V_{REF} – 1.00$ | $V_{REF} + 1.00$ | $V_{REF}$ | 1.5 |
| SSTL, Class I & II, 2.5V | SSTL2_I, SSTL2_II | $V_{REF} – 0.75$ | $V_{REF} + 0.75$ | $V_{REF}$ | 1.25 |
| SSTL, Class I & II, 1.8V | SSTL18_I, SSTL18_II | $V_{REF} – 0.5$ | $V_{REF} + 0.5$ | $V_{REF}$ | 0.90 |
| LVDS (Low-Voltage Differential Signaling), 2.5V | LVDS_25 | 1.2 – 0.125 | 1.2 + 0.125 | 0(6) | – |
| LVDSEXT (LVDS Extended Mode), 2.5V | LVDSEXT_25 | 1.2 – 0.125 | 1.2 + 0.125 | 0(6) | – |
| HT (HyperTransport), 2.5V | LDT_25 | 0.6 – 0.125 | 0.6 + 0.125 | 0(6) | – |

**Notes:**

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between $V_L$ and $V_H$.
3. Measurements are made at typical, minimum, and maximum $V_{REF}$ values. Reported delays reflect worst case of these measurements. $V_{REF}$ values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the $V_{REF}$ / $V_{MEAS}$ parameters found in IBIS models and/or noted in Figure 6.
6. The value given is the differential input voltage.

## Output Serializer/Deserializer Switching Characteristics

*Table 52:* **OSERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| **Setup/Hold** | | | | | | | |
| $T_{OSDCK\_D}/T_{OSCKD\_D}$ | D input Setup/Hold with respect to CLKDIV | 0.23/<br>–0.10 | 0.28/<br>–0.10 | 0.31/<br>–0.10 | 0.35/<br>–0.10 | 0.36/<br>–0.15 | ns |
| $T_{OSDCK\_T}/T_{OSCKD\_T}$(1) | T input Setup/Hold with respect to CLK | 0.44/<br>–0.10 | 0.51/<br>–0.09 | 0.56/<br>–0.08 | 0.60/<br>–0.08 | 0.68/<br>–0.15 | ns |
| $T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1) | T input Setup/Hold with respect to CLKDIV | 0.25/<br>–0.10 | 0.27/<br>–0.09 | 0.31/<br>–0.08 | 0.31/<br>–0.08 | 0.47/<br>–0.15 | ns |
| $T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$ | OCE input Setup/Hold with respect to CLK | 0.17/<br>–0.03 | 0.20/<br>–0.03 | 0.22/<br>–0.03 | 0.27/<br>–0.03 | 0.27/<br>–0.04 | ns |
| $T_{OSCCK\_S}$ | SR (Reset) input Setup with respect to CLKDIV | 0.07 | 0.07 | 0.07 | 0.07 | 0.08 | ns |
| $T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$ | TCE input Setup/Hold with respect to CLK | 0.15/<br>–0.04 | 0.19/<br>–0.04 | 0.21/<br>–0.04 | 0.27/<br>–0.04 | 0.29/<br>–0.05 | ns |
| **Sequential Delays** | | | | | | | |
| $T_{OSCKO\_OQ}$ | Clock to out from CLK to OQ | 0.63 | 0.71 | 0.82 | 0.82 | 0.93 | ns |
| $T_{OSCKO\_TQ}$ | Clock to out from CLK to TQ | 0.63 | 0.71 | 0.82 | 0.82 | 0.93 | ns |
| **Combinatorial** | | | | | | | |
| $T_{OSDO\_TTQ}$ | T input to TQ Out | 0.76 | 0.84 | 0.97 | 0.97 | 1.11 | ns |

**Notes:**

1. $T_{OSDCK\_T2}$ and $T_{OSCKD\_T2}$ are reported as $T_{OSDCK\_T}/T_{OSCKD\_T}$ in TRACE report.

## Input/Output Delay Switching Characteristics

*Table 53:* **Input/Output Delay Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| **IDELAYCTRL** | | | | | | |
| $T_{DLYCCO\_RDY}$ | Reset to Ready for IDELAYCTRL | 3.00 | 3.00 | 3.00 | 3.25 | µs |
| $F_{IDELAYCTRL\_REF}$ | REFCLK frequency = 200.0(1) | 200 | 200 | 200 | 200 | MHz |
| | REFCLK frequency = 300.0(1) | 300 | 300 | – | – | MHz |
| IDELAYCTRL_REF_PRECISION | REFCLK precision | ±10 | ±10 | ±10 | ±10 | MHz |
| $T_{IDELAYCTRL\_RPW}$ | Minimum Reset pulse width | 50.00 | 50.00 | 50.00 | 52.50 | ns |
| **IODELAY** | | | | | | |
| $T_{IDELAYRESOLUTION}$ | IODELAY Chain Delay Resolution | 1/(32 x 2 x $F_{REF}$) | | | | ps |
| $T_{IDELAYPAT\_JIT}$ | Pattern dependent period jitter in delay chain for clock pattern.(2) | 0 | 0 | 0 | 0 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(3) | ±5 | ±5 | ±5 | ±5 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(4) | ±9 | ±9 | ±9 | ±9 | ps per tap |
| $T_{IODELAY\_CLK\_MAX}$ | Maximum frequency of CLK input to IODELAY | 500.00 | 420.00 | 300.00 | 300.00 | MHz |
| $T_{IODCCK\_CE}$ / $T_{IODCKC\_CE}$ | CE pin Setup/Hold with respect to CK | 0.45/ –0.09 | 0.53/ –0.09 | 0.65/ –0.09 | 0.84/ –0.14 | ns |
| $T_{IODCK\_INC}$/ $T_{IODCKC\_INC}$ | INC pin Setup/Hold with respect to CK | 0.23/ –0.02 | 0.27/ –0.01 | 0.31/ 0.00 | 0.27/ –0.04 | ns |
| $T_{IODCCK\_RST}$/ $T_{IODCKC\_RST}$ | RST pin Setup/Hold with respect to CK | 0.57/ –0.08 | 0.62/ –0.08 | 0.69/ –0.08 | 0.74/ –0.13 | ns |
| $T_{IODDO\_T}$ | TSCONTROL delay to MUXE/MUXF switching and through IODELAY | Note 5 | Note 5 | Note 5 | Note 5 | ps |
| $T_{IODDO\_IDATAIN}$ | Propagation delay through IODELAY | Note 5 | Note 5 | Note 5 | Note 5 | ps |
| $T_{IODDO\_ODATAIN}$ | Propagation delay through IODELAY | Note 5 | Note 5 | Note 5 | Note 5 | ps |

**Notes:**

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IODELAY tap setting. See TRACE report for actual values.

## CLB Switching Characteristics

*Table 54:* **CLB Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| **Combinatorial Delays** | | | | | | |
| $T_{ILO}$ | An – Dn LUT address to A | 0.06 | 0.07 | 0.07 | 0.09 | ns, Max |
| | An – Dn LUT address to AMUX/CMUX | 0.18 | 0.20 | 0.22 | 0.25 | ns, Max |
| | An – Dn LUT address to BMUX_A | 0.28 | 0.31 | 0.36 | 0.40 | ns, Max |

*Table 59:* **Configuration Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $T_{MMCMDCK\_DI}$/<br>$T_{MMCMCKD\_DI}$ | DI Setup/Hold | 1.25/ 0.00 | 1.40/ 0.00 | 1.63/ 0.00 | 1.64/ 0.00 | ns |
| $T_{MMCMDCK\_DEN}$/<br>$T_{MMCMCKD\_DEN}$ | DEN Setup/Hold time | 1.25/ 0.00 | 1.40/ 0.00 | 1.63/ 0.00 | 1.64/ 0.00 | ns |
| $T_{MMCMDCK\_DWE}$/<br>$T_{MMCMCKD\_DWE}$ | DWE Setup/Hold time | 1.25/ 0.00 | 1.40/ 0.00 | 1.63/ 0.00 | 1.64/ 0.00 | ns |
| $T_{MMCMCKO\_DO}$ | CLK to out of DO(3) | 2.60 | 3.02 | 3.64 | 3.68 | ns |
| $T_{MMCMCKO\_DRDY}$ | CLK to out of DRDY | 0.32 | 0.34 | 0.38 | 0.38 | ns |

**Notes:**

1. To support longer delays in configuration, use the design solutions described in UG360: *Virtex-6 FPGA Configuration User Guide*.
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
3. DO will hold until next DRP operation.

## Clock Buffers and Networks

*Table 60:* **Global Clock Switching Characteristics (Including BUFGCTRL)**

| Symbol | Description | Devices | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1L | |
| $T_{BCCCK\_CE}$/$T_{BCCKC\_CE}$(1) | CE pins Setup/Hold | All | 0.11/ 0.00 | 0.13/ 0.00 | 0.16/ 0.00 | 0.13/ 0.00 | ns |
| $T_{BCCCK\_S}$/$T_{BCCKC\_S}$(1) | S pins Setup/Hold | All | 0.11/ 0.00 | 0.13/ 0.00 | 0.16/ 0.00 | 0.13/ 0.00 | ns |
| $T_{BCCKO\_O}$(2) | BUFGCTRL delay from I0/I1 to O | All | 0.07 | 0.08 | 0.10 | 0.10 | ns |
| **Maximum Frequency** | | | | | | | |
| $F_{MAX}$ | Global clock tree (BUFG) | All except LX760 | 800 | 750 | 700 | 667 | MHz |
| | | LX760 | N/A | 700 | 700 | 667 | MHz |

**Notes:**

1. $T_{BCCCK\_CE}$ and $T_{BCCKC\_CE}$ must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. $T_{BGCKO\_O}$ (BUFG delay from I0 to O) values are the same as $T_{BCCKO\_O}$ values.

*Table 61:* **Input/Output Clock Switching Characteristics (BUFIO)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $T_{BIOCKO\_O}$ | Clock to out delay from I to O | 0.14 | 0.16 | 0.18 | 0.21 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | I/O clock tree (BUFIO) | 800 | 800 | 710 | 710 | MHz |

*Table 62:* **Regional Clock Switching Characteristics (BUFR)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $T_{BRCKO\_O}$ | Clock to out delay from I to O | 0.56 | 0.62 | 0.73 | 0.82 | ns |
| $T_{BRCKO\_O\_BYP}$ | Clock to out delay from I to O with Divide Bypass attribute set | 0.28 | 0.31 | 0.36 | 0.41 | ns |

*Table 62:* **Regional Clock Switching Characteristics (BUFR)** ***(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $T_{BRDO\_O}$ | Propagation delay from CLR to O | 0.69 | 0.74 | 0.80 | 1.12 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$(1) | Regional clock tree (BUFR) | 500 | 420 | 300 | 300 | MHz |

**Notes:**

1. The maximum input frequency to the BUFR is the BUFIO $F_{MAX}$ frequency.

*Table 63:* **Horizontal Clock Buffer Switching Characteristics (BUFH)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $T_{BHCKO\_O}$ | BUFH delay from I to O | 0.10 | 0.11 | 0.13 | 0.15 | ns |
| $T_{BHCCK\_CE}/T_{BHCKC\_CE}$ | CE pin Setup and Hold | 0.04/ 0.04 | 0.04/ 0.04 | 0.05/ 0.05 | 0.04/ 0.04 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | Horizontal clock buffer (BUFH) | 800 | 750 | 700 | 667 | MHz |

## MMCM Switching Characteristics

*Table 64:* **MMCM Specification**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $F_{INMAX}$ | Maximum Input Clock Frequency(1) | 800 | 750 | 700 | 700 | MHz |
| $F_{INMIN}$ | Minimum Input Clock Frequency | 10 | 10 | 10 | 10 | MHz |
| $F_{INJITTER}$ | Maximum Input Clock Period Jitter | < 20% of clock input period or 1 ns Max | | | | |
| $F_{INDUTY}$(2) | Allowable Input Duty Cycle: 10—49 MHz | 25/75 | | | | % |
| | Allowable Input Duty Cycle: 50—199 MHz | 30/70 | | | | % |
| | Allowable Input Duty Cycle: 200—399 MHz | 35/65 | | | | % |
| | Allowable Input Duty Cycle: 400—499 MHz | 40/60 | | | | % |
| | Allowable Input Duty Cycle: >500 MHz | 45/55 | | | | % |
| $F_{MIN\_PSCLK}$ | Minimum Dynamic Phase Shift Clock Frequency | 0.01 | 0.01 | 0.01 | 0.01 | MHz |
| $F_{MAX\_PSCLK}$ | Maximum Dynamic Phase Shift Clock Frequency | 550 | 500 | 450 | 450 | MHz |
| $F_{VCOMIN}$ | Minimum MMCM VCO Frequency | 600 | 600 | 600 | 600 | MHz |
| $F_{VCOMAX}$ | Maximum MMCM VCO Frequency | 1600 | 1440 | 1200 | 1200 | MHz |
| $F_{BANDWIDTH}$ | Low MMCM Bandwidth at Typical(3) | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High MMCM Bandwidth at Typical(3) | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| $T_{STATPHAOFFSET}$ | Static Phase Offset of the MMCM Outputs(4) | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| $T_{OUTJITTER}$ | MMCM Output Jitter(5) | Note 3 | | | | |
| $T_{OUTDUTY}$ | MMCM Output Clock Duty Cycle Precision(6) | 0.15 | 0.20 | 0.20 | 0.20 | ns |
| $T_{LOCKMAX}$ | MMCM Maximum Lock Time | 100 | 100 | 100 | 100 | µs |
| $F_{OUTMAX}$ | MMCM Maximum Output Frequency | 800 | 750 | 700 | 700 | MHz |
| $F_{OUTMIN}$ | MMCM Minimum Output Frequency(7)(8) | 4.69 | 4.69 | 4.69 | 4.69 | MHz |
| $T_{EXTFDVAR}$ | External Clock Feedback Variation | < 20% of clock input period or 1 ns Max | | | | |

*Table 67:* **Clock-Capable Clock Input to Output Delay With MMCM**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1L | |
| LVCMOS25 Clock-capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM. | | | | | | | |
| $T_{ICKOFMMCMCC}$ | Clock-capable Clock Input and OUTFF *with* MMCM | XC6VLX75T | 2.22 | 2.38 | 2.63 | 2.72 | ns |
| | | XC6VLX130T | 2.24 | 2.39 | 2.65 | 2.74 | ns |
| | | XC6VLX195T | 2.24 | 2.40 | 2.65 | 2.75 | ns |
| | | XC6VLX240T | 2.24 | 2.40 | 2.65 | 2.75 | ns |
| | | XC6VLX365T | 2.25 | 2.42 | 2.65 | 2.76 | ns |
| | | XC6VLX550T | N/A | 2.43 | 2.68 | 2.80 | ns |
| | | XC6VLX760 | N/A | 2.42 | 2.69 | 2.79 | ns |
| | | XC6VSX315T | 2.23 | 2.38 | 2.65 | 2.73 | ns |
| | | XC6VSX475T | N/A | 2.30 | 2.57 | 2.66 | ns |
| | | XC6VHX250T | 2.25 | 2.41 | 2.67 | N/A | ns |
| | | XC6VHX255T | 2.35 | 2.51 | 2.78 | N/A | ns |
| | | XC6VHX380T | 2.27 | 2.43 | 2.69 | N/A | ns |
| | | XC6VHX565T | N/A | 2.41 | 2.68 | N/A | ns |
| | | XQ6VLX130T | N/A | 2.39 | 2.65 | 2.74 | ns |
| | | XQ6VLX240T | N/A | 2.40 | 2.65 | 2.75 | ns |
| | | XQ6VLX550T | N/A | N/A | 2.68 | 2.80 | ns |
| | | XQ6VSX315T | N/A | 2.38 | 2.65 | 2.73 | ns |
| | | XQ6VSX475T | N/A | N/A | 2.57 | 2.66 | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.