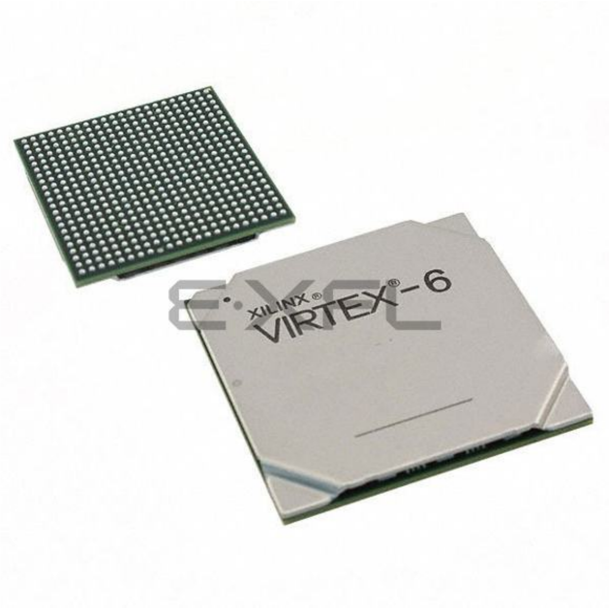


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 18840 |
| Number of Logic Elements/Cells | 241152 |
| Total RAM Bits | 15335424 |
| Number of I/O | 720 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.05V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1759-BBGA, FCBGA |
| Supplier Device Package | 1759-FCBGA (42.5x42.5) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc6vlx240t-1ffg1759i |

*Table 2:* **Recommended Operating Conditions**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{CCINT}$ | Internal supply voltage relative to GND for all devices except -1L devices. | 0.95 | 1.05 | V |
| | For -1L commercial temperature range devices: internal supply voltage relative to GND, $T_j$ = 0°C to +85°C | 0.87 | 0.93 | V |
| | For -1L industrial temperature range devices: internal supply voltage relative to GND, $T_j$ = –40°C to +100°C | 0.91 | 0.97 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage relative to GND | 2.375 | 2.625 | V |
| $V_{CCO}$ (1)(2)(3) | Supply voltage relative to GND | 1.14 | 2.625 | V |
| $V_{IN}$ | 2.5V supply voltage relative to GND | GND – 0.20 | 2.625 | V |
| | 2.5V and below supply voltage relative to GND | GND – 0.20 | $V_{CCO}$ + 0.2 | V |
| $I_{IN}$ (5) | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode. | – | 10 | mA |
| $V_{BATT}$ (6) | Battery voltage relative to GND | 1.0 | 2.5 | V |
| $V_{FS}$ (7) | External voltage supply for eFUSE programming | 2.375 | 2.625 | V |
| $T_j$ | Junction temperature operating range for commercial (C) temperature devices | 0 | 85 | °C |
| | Junction temperature operating range for extended (E) temperature devices | 0 | 100 | °C |
| | Junction temperature operating range for industrial (I) temperature devices | –40 | 100 | °C |
| | Junction temperature operating range for military (M) temperature devices | –55 | 125 | °C |

**Notes:**

1. Configuration data is retained even if $V_{CCO}$ drops to 0V.
2. Includes $V_{CCO}$ of 1.2V, 1.5V, 1.8V, and 2.5V.
3. The configuration supply voltage $V_{CC\_CONFIG}$ is also known as $V_{CCO\_0}$.
4. All voltages are relative to ground.
5. A total of 100 mA per bank should not be exceeded.
6. $V_{BATT}$ is required only when using bitstream encryption. If battery is not used, connect $V_{BATT}$ to either ground or $V_{CCAUX}$.
7. During eFUSE programming, $V_{FS}$ must be within the recommended operating range and $T_j$ = +15°C to +85°C. Otherwise, $V_{FS}$ can be connected to GND.

## Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on sequence and ramp rate of the power supply.

The recommended power-on sequence for Virtex-6 devices is $V_{CCINT}$, $V_{CCAUX}$, and $V_{CCO}$ to meet the power-up current requirements listed in Table 5. $V_{CCINT}$ can be powered up or down at any time, but power up current specifications can vary from Table 5. The device will have no physical damage or reliability concerns if $V_{CCINT}$, $V_{CCAUX}$, and $V_{CCO}$ sequence cannot be followed.

If the recommended power-up sequence cannot be followed and the I/Os must remain 3-stated throughout configuration, then $V_{CCAUX}$ must be powered prior to $V_{CCO}$ or $V_{CCAUX}$ and $V_{CCO}$ must be powered by the same supply. Similarly, for power-down, the reverse $V_{CCAUX}$ and $V_{CCO}$ sequence is recommended if the I/Os are to remain 3-stated.

The GTH transceiver supplies must be powered using a MGTHAVCC, MGTHAVCCRX, MGTHAVCCPLL, and MGTHAVTT sequence. There are no sequencing requirement for these supplies with respect to the other FPGA supply voltages. For more detail see Table 27: *GTH Transceiver Power Supply Sequencing*. There are no sequencing requirements for the GTX transceivers power supplies.

Table 5 shows the minimum current, in addition to $I_{CCQ}$, that are required by Virtex-6 devices for proper power-on and configuration. If the current minimums shown in Table 4 and Table 5 are met, the device powers on after all three supplies have passed through their power-on reset threshold voltages. The FPGA must be configured after applying $V_{CCINT}$, $V_{CCAUX}$, and $V_{CCO}$ for the appropriate configuration banks. Once initialized and configured, use the XPE tools to estimate current drain on these supplies.

*Table 5:* **Power-On Current for Virtex-6 Devices**

| Device | $I_{CCINTMIN}$ | $I_{CCAUXMIN}$ | $I_{CCOMIN}$ | Units |
|---|---|---|---|---|
| | Typ(1) | Typ(1) | Typ(1) | |
| XC6VLX75T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 10 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VLX130T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 10 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VLX195T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VLX240T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VLX365T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VLX550T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VLX760 | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VSX315T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VSX475T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 50 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VHX250T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VHX255T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VHX380T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VHX565T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XQ6VLX130T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 100 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XQ6VLX240T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 100 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XQ6VLX550T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 100 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XQ6VSX315T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 100 | $I_{CCOQ}$ + 40 mA per bank | mA |
| XQ6VSX475T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 100 | $I_{CCOQ}$ + 40 mA per bank | mA |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. Use the XPower Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.

## HT DC Specifications (HT_25)

*Table 8:* **HT DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| $V_{OD}$ | Differential Output Voltage for XC devices | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 480 | 600 | 885 | mV |
| | Differential Output Voltage for XQ devices | | 480 | 600 | 930 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ Magnitude | | –15 | – | 15 | mV |
| $V_{OCM}$ | Output Common Mode Voltage | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 440 | 600 | 760 | mV |
| $\Delta V_{OCM}$ | Change in $V_{OCM}$ Magnitude | | –15 | – | 15 | mV |
| $V_{ID}$ | Input Differential Voltage | | 200 | 600 | 1000 | mV |
| $\Delta V_{ID}$ | Change in $V_{ID}$ Magnitude | | –15 | – | 15 | mV |
| $V_{ICM}$ | Input Common Mode Voltage | | 440 | 600 | 780 | mV |
| $\Delta V_{ICM}$ | Change in $V_{ICM}$ Magnitude | | –15 | – | 15 | mV |

## LVDS DC Specifications (LVDS_25)

*Table 9:* **LVDS DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| $V_{OH}$ | Output High Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | – | – | 1.675 | V |
| $V_{OL}$ | Output Low Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 0.825 | – | – | V |
| $V_{ODIFF}$ | Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 247 | 350 | 600 | mV |
| $V_{OCM}$ | Output Common-Mode Voltage for XC devices | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.075 | 1.250 | 1.425 | V |
| | Output Common-Mode Voltage for XQ devices | | 1.000 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | | 100 | 350 | 600 | mV |
| $V_{ICM}$ | Input Common-Mode Voltage | | 0.3 | 1.2 | 2.2 | V |

## Extended LVDS DC Specifications (LVDSEXT_25)

*Table 10:* **Extended LVDS DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| $V_{OH}$ | Output High Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | – | – | 1.785 | V |
| $V_{OL}$ | Output Low Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 0.715 | – | – | V |
| $V_{ODIFF}$ | Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High for XC devices | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 350 | – | 840 | mV |
| | Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High for XQ devices | | 350 | – | 850 | mV |
| $V_{OCM}$ | Output Common-Mode Voltage for XC devices | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.075 | 1.250 | 1.425 | V |
| | Output Common-Mode Voltage for XQ devices | | 1.000 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | Common-mode input voltage = 1.25V | 100 | – | 1000 | mV |
| $V_{ICM}$ | Input Common-Mode Voltage | Differential input voltage = ±350 mV | 0.3 | 1.2 | 2.2 | V |

*Table 21:* **GTX Transceiver Reference Clock Switching Characteristics**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $F_{GCLK}$ | Reference clock frequency range | | 62.5 | – | 650 | MHz |
| $T_{RCLK}$ | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| $T_{FCLK}$ | Reference clock fall time | 80% – 20% | – | 200 | – | ps |
| $T_{DCREF}$ | Reference clock duty cycle | Transceiver PLL only | 45 | 50 | 55 | % |
| $T_{LOCK}$ | Clock recovery frequency acquisition time | Initial PLL lock | – | – | 1 | ms |
| $T_{PHASE}$ | Clock recovery phase acquisition time | Lock to data after PLL has locked to the reference clock | – | – | 200 | µs |

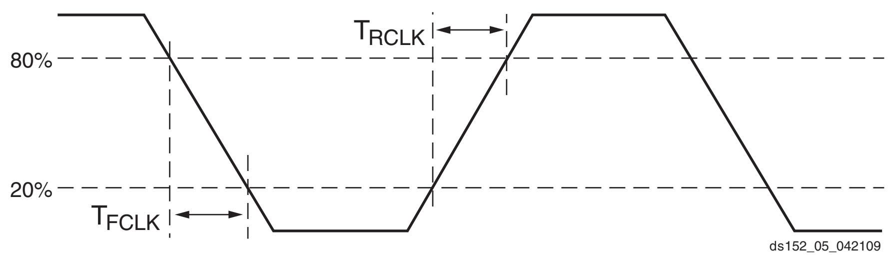


*Figure 3:* **Reference Clock Timing Parameters**

*Table 22:* **GTX Transceiver User Clock Switching Characteristics**[(1)]

| Symbol | Description | Conditions | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1L | |
| $F_{TXOUT}$ | TXOUTCLK maximum frequency | Internal 20-bit data path | 330 | 330 | 250 | 250 | MHz |
| | | Internal 16-bit data path | 412.5 | 412.5 | 312.5 | 250 | MHz |
| $F_{RXREC}$ | RXRECCLK maximum frequency | Internal 20-bit data path | 330 | 330 | 250 | 250 | MHz |
| | | Internal 16-bit data path | 412.5 | 412.5 | 312.5 | 250 | MHz |
| $T_{RX}$ | RXUSRCLK maximum frequency | | 412.5[(2)] | 412.5[(2)] | 312.5 | 250 | MHz |
| $T_{RX2}$ | RXUSRCLK2 maximum frequency | 1 byte interface | 376 | 376 | 312.5 | 250 | MHz |
| | | 2 byte interface | 406.25 | 406.25 | 312.5 | 250 | MHz |
| | | 4 byte interface | 206.25 | 206.25 | 156.25 | 125 | MHz |
| $T_{TX}$ | TXUSRCLK maximum frequency | | 412.5[(3)] | 412.5[(3)] | 312.5 | 250 | MHz |
| $T_{TX2}$ | TXUSRCLK2 maximum frequency | 1 byte interface | 376 | 376 | 312.5 | 250 | MHz |
| | | 2 byte interface | 406.25 | 406.25 | 312.5 | 250 | MHz |
| | | 4 byte interface | 206.25 | 206.25 | 156.25 | 125 | MHz |

**Notes:**

1. Clocking must be implemented as described in UG366:*Virtex-6 FPGA GTX Transceivers User Guide*.
2. 406.25 MHz when the RX elastic buffer is bypassed.
3. 406.25 MHz when the TX buffer is bypassed.

# GTH Transceiver Specifications

## GTH Transceiver DC Characteristics

*Table 25:* **Absolute Maximum Ratings for GTH Transceivers(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| MGTHAVCC | Analog supply voltage for the GTH transmitter, receiver, and common analog circuits | –0.5 | 1.125 | V |
| MGTHAVCCRX | Analog supply voltage for the GTH receiver circuits and common analog circuits | –0.5 | 1.125 | V |
| MGTHAVTT | Analog supply voltage for the GTH transmitter termination circuits | –0.5 | 1.32 | V |
| MGTHAVCCPLL | Analog supply voltage for the GTH receiver and PLL circuits | –0.5 | 1.935 | V |
| $V_{IN}$ | Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage | –0.5 | 1.125 | V |
| $V_{MGTREFCLK}$ | Reference clock absolute input voltage | –0.5 | 1.935 | V |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

*Table 26:* **Recommended Operating Conditions for GTH Transceivers (1)(2)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| MGTHAVCC | Analog supply voltage for the GTH transmitter, receiver, and common analog circuits | 1.075 | 1.1 | 1.125 | V |
| MGTHAVCCRX | Analog supply voltage for the GTH receiver circuits and common analog circuits | 1.075 | 1.1 | 1.125 | V |
| MGTHAVTT | Analog supply voltage for the GTH transmitter termination circuits | 1.140 | 1.2 | 1.26 | V |
| MGTHAVCCPLL | Analog supply voltage for the GTH receiver and PLL circuit | 1.710 | 1.8 | 1.89 | V |

**Notes:**

1. Each voltage listed requires the filter circuit described in UG371: *Virtex-6 FPGA GTH Transceivers User Guide*.
2. Voltages are specified for the temperature range of $T_j$ = –40°C to +100°C.

*Table 27:* **GTH Transceiver Power Supply Sequencing (1)(2)(3)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{HAVCC2HAVCCRX}$ | Maximum time between powering MGTHAVCC to when MGTHAVCCRX must be powered. | 0 | 5 | ms |
| $T_{HAVCCRX2HAVCCPLL}$ | Minimum time between powering MGTHAVCCRX to when MGTHAVCCPLL can be powered. | 10 | – | µs |
| $T_{HAVCCRX2HAVTT}$ | Minimum time between powering MGTHAVCCRX to when MGTHAVTT can be powered. | 10 | – | µs |

**Notes:**

1. MGTHAVCCRX must be powered simultaneously or within $T_{HAVCC2HAVCCRX}$ of MGTHAVCC, but it must not precede MGTHAVCC.
2. MGTHAVCC and MGTHAVCCRX must be powered before MGTHAVCCPLL and MGTHAVTT. This minimum time is defined by $T_{HAVCCRX2HAVCCPLL}$ and $T_{HAVCCRX2HAVTT}$.
3. At any time, the condition of MGTHAVCC being present and MGTHAVCCRX not being present should not occur for more than the maximum $T_{HAVCC2HAVCCRX}$.

Figure 4 shows the timing parameters in Table 27.

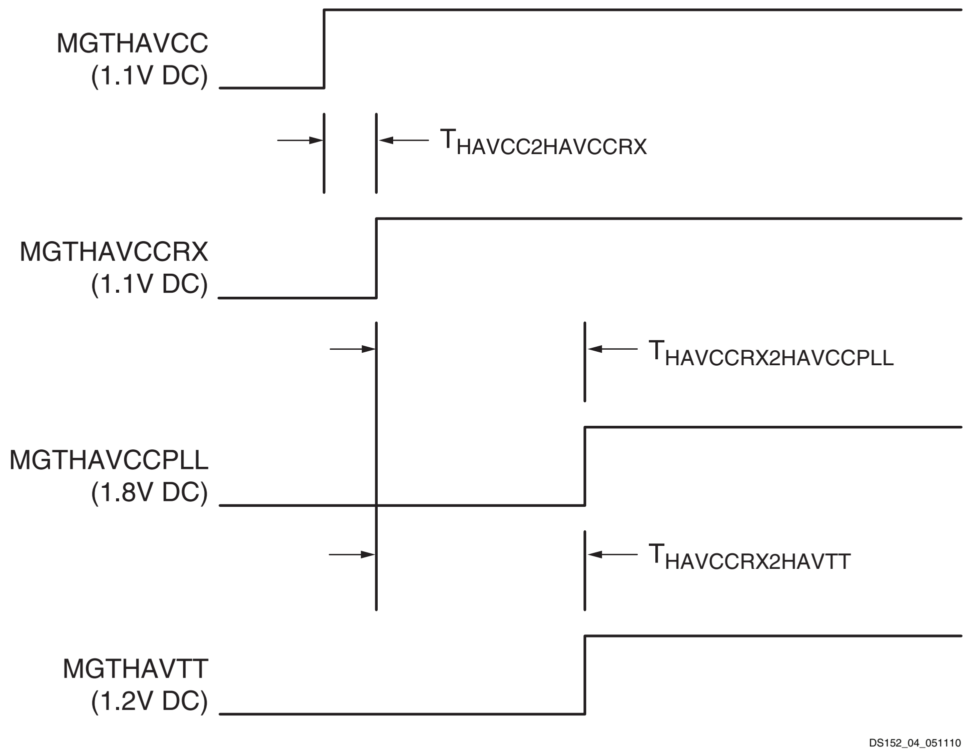


*Figure 4:* **GTH Transceiver Power Supply Power-On Sequencing**

*Table 28:* **GTH Transceiver Supply Current**

| Symbol | Description | Typ(1) | Max | Units |
|---|---|---|---|---|
| $I_{MGTHAVCC}$ | MGTHAVCC supply current for one GTH Quad (4 lanes) | 571 | Note 2 | mA |
| $I_{MGTHAVCCRX}$ | MGTHAVCCRX supply current for a GTH Quad (4 lanes) | 254 | Note 2 | mA |
| $I_{MGTHAVTT}$ | MGTHAVTT supply current for one GTH Quad (4 lanes) | 93 | Note 2 | mA |
| $I_{MGTHAVCCPLL}$ | MGTHAVCCPLL supply current for one GTH Quad (4 lanes) | 219 | Note 2 | mA |
| $MGTR_{REF}$ | Precision reference resistor for internal calibration termination | 1000.0 ± 1% tolerance | | Ω |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C, with a 10.3125 Gb/s line rate.
2. Values for currents other than the values specified in this table can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

*Table 29:* **GTH Transceiver Quiescent Supply Current(1)(2)**

| Symbol | Description | Typ(3) | Max | Units |
|---|---|---|---|---|
| $I_{MGTHAVCCQ}$ | Quiescent MGTHAVCC Supply Current for one GTH Quad (4 lanes) | 65 | Note 4 | mA |
| $I_{MGTHAVCCRXQ}$ | Quiescent MGTHAVCCRX Supply Current for one GTH Quad (4 lanes) | 17 | Note 4 | mA |
| $I_{MGTHAVTTQ}$ | Quiescent MGTHAVTT Supply Current for one GTH Quad (4 lanes) | 1 | Note 4 | mA |
| $I_{MGTHAVCCPLLQ}$ | Quiescent MGTHAVCCPLL Supply Current for one GTH Quad (4 lanes) | 1 | Note 4 | mA |

**Notes:**

1. Device powered and unconfigured.
2. GTH transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTH transceivers.
3. Typical values are specified at nominal voltage, 25°C.
4. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.

## Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

*Table 39:* **Maximum Performance for PCI Express Designs**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $F_{PIPECLK}$ | Pipe clock maximum frequency | 250 | 250 | 250 | 250 | MHz |
| $F_{USERCLK}$ | User clock maximum frequency | 500 | 500 | 250 | 250 | MHz |
| $F_{DRPCLK}$ | DRP clock maximum frequency | 250 | 250 | 250 | 250 | MHz |

## System Monitor Analog-to-Digital Converter Specification

*Table 40:* **Analog-to-Digital Specifications**

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $AV_{DD}$ = 2.5V ± 5%, $V_{REFP}$ = 1.25V, $V_{REFN}$ = 0V, ADCCLK = 5.2 MHz, $T_j$ = –55°C to 125°C M-Grade, Typical values at $T_j$=+35°C | | | | | | |
| **DC Accuracy:** All external input channels. Both unipolar and bipolar modes. | | | | | | |
| Resolution | | | 10 | – | – | Bits |
| Integral Nonlinearity | INL | | – | – | ±1 | LSBs |
| Differential Nonlinearity | DNL | No missing codes ($T_{MIN}$ to $T_{MAX}$)<br>Guaranteed Monotonic | – | – | ±0.9 | LSBs |
| Unipolar Offset Error (1) | | Uncalibrated | – | ±2 | ±30 | LSBs |
| Bipolar Offset Error (1) | | Uncalibrated measured in bipolar mode | – | ±2 | ±30 | LSBs |
| Gain Error | | Uncalibrated - External Reference | – | ±0.2 | ±2 | % |
| | | Uncalibrated - Internal Reference | – | ±2 | – | % |
| Bipolar Gain Error (1) | | Uncalibrated - External Reference | – | ±0.2 | ±2 | % |
| | | Uncalibrated - Internal Reference | – | ±2 | – | % |
| Total Unadjusted Error (Uncalibrated) | TUE | Deviation from ideal transfer function. External 1.25V reference | – | ±10 | – | LSBs |
| | | Deviation from ideal transfer function. Internal reference | – | ±20 | – | LSBs |
| Total Unadjusted Error (Calibrated) | TUE | Deviation from ideal transfer function. External 1.25V reference | – | ±1 | ±2 | LSBs |
| Calibrated Gain Temperature Coefficient | | Variation of FS code with temperature | – | ±0.01 | – | LSB/°C |
| DC Common-Mode Reject | $CMRR_{DC}$ | $V_N = V_{CM}$ = 0.5V ± 0.5V,<br>$V_P - V_N$ = 100mV | – | 70 | – | dB |
| **Conversion Rate**(2) | | | | | | |
| Conversion Time - Continuous | $t_{CONV}$ | Number of CLK cycles | 26 | – | 32 | |
| Conversion Time - Event | $t_{CONV}$ | Number of CLK cycles | – | – | 21 | |
| T/H Acquisition Time | $t_{ACQ}$ | Number of CLK cycles | 4 | – | – | |
| DRP Clock Frequency | DCLK | DRP clock frequency | 8 | – | 80 | MHz |
| ADC Clock Frequency | ADCCLK | Derived from DCLK | 1 | – | 5.2 | MHz |
| CLK Duty cycle | | | 40 | – | 60 | % |

*Table 40:* **Analog-to-Digital Specifications *(Cont'd)***

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Analog Inputs**[3] | | | | | | |
| Dedicated Analog Inputs Input Voltage Range $V_P$ - $V_N$ | | Unipolar Operation | 0 | – | 1 | Volts |
| | | Bipolar Operation | –0.5 | – | +0.5 | |
| | | Unipolar Common Mode Range (FS input) | 0 | – | +0.5 | |
| | | Bipolar Common Mode Range (FS input) | +0.5 | – | +0.6 | |
| | | Bandwidth | – | 20 | – | MHz |
| Auxiliary Analog Inputs Input Voltage Range $V_{AUXP[0]}$ /$V_{AUXN[0]}$ to $V_{AUXP[15]}$ /$V_{AUXN[15]}$ $T_j$ = –55°C to 125°C | | Unipolar Operation | 0 | – | 1 | Volts |
| | | Bipolar Operation | –0.5 | – | +0.5 | |
| | | Unipolar Common Mode Range (FS input) | 0 | – | +0.5 | |
| | | Bipolar Common Mode Range (FS input) | +0.5 | – | +0.6 | |
| | | Bandwidth | – | 10 | – | kHz |
| Input Leakage Current | | A/D not converting, ADCCLK stopped | – | ±1.0 | – | µA |
| Input Capacitance | | | – | 10 | – | pF |
| On-chip Supply Monitor Error | | $V_{CCINT}$ and $V_{CCAUX}$ with calibration enabled. External 1.25V reference $T_j$ = –55°C to 125°C. | – | – | ±1.0 | % Reading |
| | | $V_{CCINT}$ and $V_{CCAUX}$ with calibration enabled. Internal reference $T_j$ = –40°C to 100°C.[4] | – | ±2 | – | % Reading |
| On-chip Temperature Monitor Error | | $T_j$ = –55°C to +125°C with calibration enabled. External 1.25V reference. | – | – | ±4 | °C |
| | | $T_j$ = –40°C to +100°C with calibration enabled. Internal reference.[4] | – | ±5 | – | °C |
| **External Reference Inputs**[5] | | | | | | |
| Positive Reference Input Voltage Range | $V_{REFP}$ | Measured Relative to $V_{REFN}$ | 1.20 | 1.25 | 1.30 | Volts |
| Negative Reference Input Voltage Range | $V_{REFN}$ | Measured Relative to AGND | –50 | 0 | 100 | mV |
| Input current | $I_{REF}$ | ADCCLK = 5.2 MHz | – | – | 100 | µA |
| **Power Requirements** | | | | | | |
| Analog Power Supply | $AV_{DD}$ | Measured Relative to $AV_{SS}$ | 2.375 | 2.5 | 2.625 | Volts |
| Analog Supply Current | $AI_{DD}$ | ADCCLK = 5.2 MHz | – | – | 12 | mA |

**Notes:**

1. Offset errors are removed by enabling the System Monitor automatic gain calibration feature.
2. See "System Monitor Timing" in UG370: *Virtex-6 FPGA System Monitor User Guide*
3. See "Analog Inputs" in UG370: *Virtex-6 FPGA System Monitor User Guide* for a detailed description.
4. These internal references are not specified over the junction temperature operating range for military (M) temperature devices.
5. Any variation in the reference voltage from the nominal $V_{REFP}$ = 1.25V and $V_{REFN}$ = 0V will result in a deviation from the ideal transfer function.This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

## Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.17 for -3, -2, and -1; and v1.10 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

### Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 42 correlates the current status of each Virtex-6 device on a per speed grade basis.

*Table 42:* **Virtex-6 Device Speed Grade Designations**

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XC6VLX75T | | | -3, -2, -1, -1L |
| XC6VLX130T | | | -3, -2, -1, -1L |
| XC6VLX195T | | | -3, -2, -1, -1L |
| XC6VLX240T | | | -3, -2, -1, -1L |
| XC6VLX365T | | | -3, -2, -1, -1L |
| XC6VLX550T | | | -2, -1, -1L |
| XC6VLX760 | | | -2, -1, -1L |
| XC6VSX315T | | | -3, -2, -1, -1L |
| XC6VSX475T | | | -2, -1, -1L |
| XC6VHX250T | | | -3, -2, -1 |
| XC6VHX255T | | | -3, -2, -1 |
| XC6VHX380T | | | -3, -2, -1 |
| XC6VHX565T | | | -2, -1 |
| XQ6VLX130T | | | -2, -1, -1L |
| XQ6VLX240T | | | -2, -1, -1L |
| XQ6VLX550T | | | -1, -1L |
| XQ6VSX315T | | | -2, -1, -1L |
| XQ6VSX475T | | | -1, -1L |

## Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 devices.

*Table 44:* **IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | |
| DIFF_SSTL18_I | 0.85 | 0.94 | 1.09 | 1.08 | 1.47 | 1.58 | 1.75 | 1.73 | 1.47 | 1.58 | 1.75 | 1.73 | ns |
| DIFF_SSTL18_I_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.40 | 1.51 | 1.67 | 1.65 | 1.40 | 1.51 | 1.67 | 1.65 | ns |
| DIFF_SSTL18_II | 0.85 | 0.94 | 1.09 | 1.08 | 1.39 | 1.50 | 1.67 | 1.66 | 1.39 | 1.50 | 1.67 | 1.66 | ns |
| DIFF_SSTL18_II_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.36 | 1.47 | 1.63 | 1.62 | 1.36 | 1.47 | 1.63 | 1.62 | ns |
| DIFF_SSTL18_II_T_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.40 | 1.51 | 1.67 | 1.65 | 1.40 | 1.51 | 1.67 | 1.65 | ns |
| DIFF_SSTL15 | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.71 | 1.69 | 1.42 | 1.54 | 1.71 | 1.69 | ns |
| DIFF_SSTL15_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.41 | 1.52 | 1.68 | 1.66 | 1.41 | 1.52 | 1.68 | 1.66 | ns |
| DIFF_SSTL15_T_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.41 | 1.52 | 1.68 | 1.66 | 1.41 | 1.52 | 1.68 | 1.66 | ns |

*Table 45:* **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices**

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| LVDS_25 | 0.94 | 1.09 | 1.08 | 1.54 | 2.16 | 1.62 | 1.54 | 2.16 | 1.62 | ns |
| LVDSEXT_25 | 0.94 | 1.09 | 1.08 | 1.65 | 2.20 | 1.73 | 1.65 | 2.20 | 1.73 | ns |
| HT_25 | 0.94 | 1.09 | 1.08 | 1.62 | 2.20 | 1.69 | 1.62 | 2.20 | 1.69 | ns |
| BLVDS_25 | 0.94 | 1.09 | 1.08 | 1.50 | 3.18 | 1.65 | 1.50 | 3.18 | 1.65 | ns |
| RSDS_25 (point to point) | 0.94 | 1.09 | 1.08 | 1.54 | 2.22 | 1.62 | 1.54 | 2.22 | 1.62 | ns |
| HSTL_I | 0.91 | 1.06 | 1.06 | 1.56 | 2.44 | 1.71 | 1.56 | 2.44 | 1.71 | ns |
| HSTL_II | 0.91 | 1.06 | 1.06 | 1.56 | 2.21 | 1.72 | 1.56 | 2.21 | 1.72 | ns |
| HSTL_III | 0.91 | 1.06 | 1.06 | 1.54 | 2.50 | 1.69 | 1.54 | 2.50 | 1.69 | ns |
| HSTL_I_18 | 0.91 | 1.06 | 1.06 | 1.58 | 2.43 | 1.72 | 1.58 | 2.43 | 1.72 | ns |
| HSTL_II_18 | 0.91 | 1.06 | 1.06 | 1.62 | 2.30 | 1.78 | 1.62 | 2.30 | 1.78 | ns |
| HSTL_III_18 | 0.91 | 1.06 | 1.06 | 1.54 | 2.49 | 1.69 | 1.54 | 2.49 | 1.69 | ns |
| SSTL2_I | 0.91 | 1.06 | 1.06 | 1.60 | 2.50 | 1.74 | 1.60 | 2.50 | 1.74 | ns |
| SSTL2_II | 0.91 | 1.06 | 1.06 | 1.54 | 2.49 | 1.71 | 1.54 | 2.49 | 1.71 | ns |
| SSTL15 | 0.91 | 1.06 | 1.06 | 1.54 | 2.07 | 1.69 | 1.54 | 2.07 | 1.69 | ns |
| LVCMOS25, Slow, 2 mA | 0.57 | 0.66 | 0.70 | 5.46 | 6.01 | 5.63 | 5.46 | 6.01 | 5.63 | ns |
| LVCMOS25, Slow, 4 mA | 0.57 | 0.66 | 0.70 | 3.49 | 3.79 | 3.65 | 3.49 | 3.79 | 3.65 | ns |
| LVCMOS25, Slow, 6 mA | 0.57 | 0.66 | 0.70 | 2.81 | 3.08 | 2.95 | 2.81 | 3.08 | 2.95 | ns |
| LVCMOS25, Slow, 8 mA | 0.57 | 0.66 | 0.70 | 2.41 | 2.72 | 2.59 | 2.41 | 2.72 | 2.59 | ns |
| LVCMOS25, Slow, 12 mA | 0.57 | 0.66 | 0.70 | 1.95 | 2.23 | 2.10 | 1.95 | 2.23 | 2.10 | ns |
| LVCMOS25, Slow, 16 mA | 0.57 | 0.66 | 0.70 | 2.05 | 2.29 | 2.21 | 2.05 | 2.29 | 2.21 | ns |
| LVCMOS25, Slow, 24 mA | 0.57 | 0.66 | 0.70 | 1.82 | 2.24 | 1.98 | 1.82 | 2.24 | 1.98 | ns |
| LVCMOS25, Fast, 2 mA | 0.57 | 0.66 | 0.70 | 5.49 | 6.04 | 5.62 | 5.49 | 6.04 | 5.62 | ns |
| LVCMOS25, Fast, 4 mA | 0.57 | 0.66 | 0.70 | 3.50 | 3.82 | 3.65 | 3.50 | 3.82 | 3.65 | ns |
| LVCMOS25, Fast, 6 mA | 0.57 | 0.66 | 0.70 | 2.73 | 2.99 | 2.88 | 2.73 | 2.99 | 2.88 | ns |
| LVCMOS25, Fast, 8 mA | 0.57 | 0.66 | 0.70 | 2.33 | 2.65 | 2.53 | 2.33 | 2.65 | 2.53 | ns |
| LVCMOS25, Fast, 12 mA | 0.57 | 0.66 | 0.70 | 1.88 | 2.08 | 2.03 | 1.88 | 2.08 | 2.03 | ns |

*Table 45:* **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| LVCMOS25, Fast, 16 mA | 0.57 | 0.66 | 0.70 | 1.92 | 2.15 | 2.08 | 1.92 | 2.15 | 2.08 | ns |
| LVCMOS25, Fast, 24 mA | 0.57 | 0.66 | 0.70 | 1.79 | 2.15 | 1.96 | 1.79 | 2.15 | 1.96 | ns |
| LVCMOS18, Slow, 2 mA | 0.61 | 0.71 | 0.73 | 4.47 | 4.87 | 4.30 | 4.47 | 4.87 | 4.30 | ns |
| LVCMOS18, Slow, 4 mA | 0.61 | 0.71 | 0.73 | 2.96 | 3.21 | 2.94 | 2.96 | 3.21 | 2.94 | ns |
| LVCMOS18, Slow, 6 mA | 0.61 | 0.71 | 0.73 | 2.43 | 2.64 | 2.47 | 2.43 | 2.64 | 2.47 | ns |
| LVCMOS18, Slow, 8 mA | 0.61 | 0.71 | 0.73 | 2.11 | 2.41 | 2.24 | 2.11 | 2.41 | 2.24 | ns |
| LVCMOS18, Slow, 12 mA | 0.61 | 0.71 | 0.73 | 1.99 | 2.30 | 2.10 | 1.99 | 2.30 | 2.10 | ns |
| LVCMOS18, Slow, 16 mA | 0.61 | 0.71 | 0.73 | 1.95 | 2.30 | 2.04 | 1.95 | 2.30 | 2.04 | ns |
| LVCMOS18, Fast, 2 mA | 0.61 | 0.71 | 0.73 | 4.23 | 4.57 | 4.08 | 4.23 | 4.57 | 4.08 | ns |
| LVCMOS18, Fast, 4 mA | 0.61 | 0.71 | 0.73 | 2.76 | 2.97 | 2.74 | 2.76 | 2.97 | 2.74 | ns |
| LVCMOS18, Fast, 6 mA | 0.61 | 0.71 | 0.73 | 2.28 | 2.46 | 2.32 | 2.28 | 2.46 | 2.32 | ns |
| LVCMOS18, Fast, 8 mA | 0.61 | 0.71 | 0.73 | 1.99 | 2.34 | 2.14 | 1.99 | 2.34 | 2.14 | ns |
| LVCMOS18, Fast, 12 mA | 0.61 | 0.71 | 0.73 | 1.80 | 2.19 | 1.88 | 1.80 | 2.19 | 1.88 | ns |
| LVCMOS18, Fast, 16 mA | 0.61 | 0.71 | 0.73 | 1.74 | 2.18 | 1.88 | 1.74 | 2.18 | 1.88 | ns |
| LVCMOS15, Slow, 2 mA | 0.73 | 0.85 | 0.85 | 3.77 | 4.29 | 3.91 | 3.77 | 4.29 | 3.91 | ns |
| LVCMOS15, Slow, 4 mA | 0.73 | 0.85 | 0.85 | 2.79 | 3.10 | 2.93 | 2.79 | 3.10 | 2.93 | ns |
| LVCMOS15, Slow, 6 mA | 0.73 | 0.85 | 0.85 | 2.32 | 2.68 | 2.50 | 2.32 | 2.68 | 2.50 | ns |
| LVCMOS15, Slow, 8 mA | 0.73 | 0.85 | 0.85 | 1.98 | 2.29 | 2.24 | 1.98 | 2.29 | 2.24 | ns |
| LVCMOS15, Slow, 12 mA | 0.73 | 0.85 | 0.85 | 1.91 | 2.23 | 2.07 | 1.91 | 2.23 | 2.07 | ns |
| LVCMOS15, Slow, 16 mA | 0.73 | 0.85 | 0.85 | 1.83 | 2.23 | 1.98 | 1.83 | 2.23 | 1.98 | ns |
| LVCMOS15, Fast, 2 mA | 0.73 | 0.85 | 0.85 | 3.77 | 4.28 | 3.91 | 3.77 | 4.28 | 3.91 | ns |
| LVCMOS15, Fast, 4 mA | 0.73 | 0.85 | 0.85 | 2.53 | 2.78 | 2.66 | 2.53 | 2.78 | 2.66 | ns |
| LVCMOS15, Fast, 6 mA | 0.73 | 0.85 | 0.85 | 2.05 | 2.42 | 2.16 | 2.05 | 2.42 | 2.16 | ns |
| LVCMOS15, Fast, 8 mA | 0.73 | 0.85 | 0.85 | 1.90 | 2.20 | 2.04 | 1.90 | 2.20 | 2.04 | ns |
| LVCMOS15, Fast, 12 mA | 0.73 | 0.85 | 0.85 | 1.77 | 2.11 | 1.90 | 1.77 | 2.11 | 1.90 | ns |
| LVCMOS15, Fast, 16 mA | 0.73 | 0.85 | 0.85 | 1.76 | 2.11 | 1.92 | 1.76 | 2.11 | 1.92 | ns |
| LVCMOS12, Slow, 2 mA | 0.81 | 0.93 | 0.95 | 3.39 | 3.75 | 3.54 | 3.39 | 3.75 | 3.54 | ns |
| LVCMOS12, Slow, 4 mA | 0.81 | 0.93 | 0.95 | 2.63 | 2.93 | 2.79 | 2.63 | 2.93 | 2.79 | ns |
| LVCMOS12, Slow, 6 mA | 0.81 | 0.93 | 0.95 | 2.11 | 2.67 | 2.26 | 2.11 | 2.67 | 2.26 | ns |
| LVCMOS12, Slow, 8 mA | 0.81 | 0.93 | 0.95 | 2.02 | 2.25 | 2.17 | 2.02 | 2.25 | 2.17 | ns |
| LVCMOS12, Fast, 2 mA | 0.81 | 0.93 | 0.95 | 2.98 | 3.39 | 3.11 | 2.98 | 3.39 | 3.11 | ns |
| LVCMOS12, Fast, 4 mA | 0.81 | 0.93 | 0.95 | 2.16 | 2.70 | 2.31 | 2.16 | 2.70 | 2.31 | ns |
| LVCMOS12, Fast, 6 mA | 0.81 | 0.93 | 0.95 | 1.89 | 2.34 | 2.05 | 1.89 | 2.34 | 2.05 | ns |
| LVCMOS12, Fast, 8 mA | 0.81 | 0.93 | 0.95 | 1.82 | 2.10 | 1.98 | 1.82 | 2.10 | 1.98 | ns |
| LVDCI_25 | 0.57 | 0.70 | 0.70 | 2.14 | 2.82 | 2.26 | 2.14 | 2.82 | 2.26 | ns |
| LVDCI_18 | 0.61 | 0.71 | 0.73 | 2.23 | 2.78 | 2.38 | 2.23 | 2.78 | 2.38 | ns |
| LVDCI_15 | 0.73 | 0.85 | 0.85 | 2.01 | 2.75 | 2.18 | 2.01 | 2.75 | 2.18 | ns |
| LVDCI_DV2_25 | 0.57 | 0.70 | 0.70 | 1.83 | 2.37 | 2.00 | 1.83 | 2.37 | 2.00 | ns |

*Table 48:* **Output Delay Measurement Methodology *(Cont'd)***

| Description | I/O Standard Attribute | $R_{REF}$ ($\Omega$) | $C_{REF}$[(1)] (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| HT (HyperTransport), 2.5V | LDT_25 | 100 | 0 | 0[(2)] | 0.6 |
| LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V | LVPECL_25 | 100 | 0 | 0[(2)] | 0 |
| LVDCI/HSLVDCI, 2.5V | LVDCI_25, HSLVDCI_25 | 1M | 0 | 1.25 | 0 |
| LVDCI/HSLVDCI, 1.8V | LVDCI_18, HSLVDCI_18 | 1M | 0 | 0.9 | 0 |
| LVDCI/HSLVDCI, 1.5V | LVDCI_15, HSLVDCI_15 | 1M | 0 | 0.75 | 0 |
| HSTL (High-Speed Transceiver Logic), Class I & II, with DCI | HSTL_I_DCI, HSTL_II_DCI | 50 | 0 | $V_{REF}$ | 0.75 |
| HSTL, Class III, with DCI | HSTL_III_DCI | 50 | 0 | 0.9 | 1.5 |
| HSTL, Class I & II, 1.8V, with DCI | HSTL_I_DCI_18, HSTL_II_DCI_18 | 50 | 0 | $V_{REF}$ | 0.9 |
| HSTL, Class III, 1.8V, with DCI | HSTL_III_DCI_18 | 50 | 0 | 1.1 | 1.8 |
| SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI | SSTL18_I_DCI, SSTL18_II_DCI | 50 | 0 | $V_{REF}$ | 0.9 |
| SSTL, Class I & II, 2.5V, with DCI | SSTL2_I_DCI, SSTL2_II_DCI | 50 | 0 | $V_{REF}$ | 1.25 |

**Notes:**

1. $C_{REF}$ is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

## Input/Output Logic Switching Characteristics

*Table 49:* **ILOGIC Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| **Setup/Hold** | | | | | | |
| $T_{ICE1CK}/T_{ICKCE1}$ | CE1 pin Setup/Hold with respect to CLK | 0.21/ 0.03 | 0.25/ 0.04 | 0.27/ 0.04 | 0.31/ 0.05 | ns |
| $T_{ISRCK}/T_{ICKSR}$ | SR pin Setup/Hold with respect to CLK | 0.66/ –0.08 | 0.78/ –0.08 | 0.96/ –0.08 | 1.09/ –0.11 | ns |
| $T_{IDOCK}/T_{IOCKD}$ | D pin Setup/Hold with respect to CLK without Delay | 0.07/ 0.41 | 0.08/ 0.46 | 0.10/ 0.54 | 0.11/ 0.64 | ns |
| $T_{IDOCKD}/T_{IOCKDD}$ | DDLY pin Setup/Hold with respect to CLK (using IODELAY) | 0.10/ 0.32 | 0.12/ 0.36 | 0.14/ 0.42 | 0.16/ 0.50 | ns |
| **Combinatorial** | | | | | | |
| $T_{IDI}$ | D pin to O pin propagation delay, no Delay | 0.15 | 0.17 | 0.20 | 0.23 | ns |
| $T_{IDID}$ | DDLY pin to O pin propagation delay (using IODELAY) | 0.19 | 0.22 | 0.25 | 0.28 | ns |
| **Sequential Delays** | | | | | | |
| $T_{IDLO}$ | D pin to Q1 pin using flip-flop as a latch without Delay | 0.48 | 0.54 | 0.64 | 0.73 | ns |
| $T_{IDLOD}$ | DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY) | 0.52 | 0.58 | 0.68 | 0.78 | ns |
| $T_{ICKQ}$ | CLK to Q outputs | 0.54 | 0.61 | 0.70 | 0.93 | ns |
| $T_{RQ\_ILOGIC}$ | SR pin to OQ/TQ out | 0.85 | 0.97 | 1.15 | 1.32 | ns |
| $T_{GSRQ\_ILOGIC}$ | Global Set/Reset to Q outputs | 7.60 | 7.60 | 10.51 | 10.51 | ns |
| **Set/Reset** | | | | | | |
| $T_{RPW\_ILOGIC}$ | Minimum Pulse Width, SR inputs | 0.78 | 0.95 | 1.20 | 1.30 | ns, Min |

## Input Serializer/Deserializer Switching Characteristics

*Table 51:* **ISERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| **Setup/Hold for Control Lines** | | | | | | | |
| $T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$ | BITSLIP pin Setup/Hold with respect to CLKDIV | 0.07/ 0.15 | 0.08/ 0.16 | 0.09/ 0.17 | 0.09/ 0.17 | 0.14/ 0.17 | ns |
| $T_{ISCCK\_CE}$ / $T_{ISCKC\_CE}$[(2)] | CE pin Setup/Hold with respect to CLK (for CE1) | 0.20/ 0.03 | 0.25/ 0.04 | 0.27/ 0.04 | 0.27/ 0.04 | 0.31/ 0.05 | ns |
| $T_{ISCCK\_CE2}$ / $T_{ISCKC\_CE2}$[(2)] | CE pin Setup/Hold with respect to CLKDIV (for CE2) | 0.01/ 0.27 | 0.01 0.29 | 0.01/ 0.31 | 0.01/ 0.31 | –0.05/ 0.35 | ns |
| **Setup/Hold for Data Lines** | | | | | | | |
| $T_{ISDCK\_D}$ /$T_{ISCKD\_D}$ | D pin Setup/Hold with respect to CLK | 0.07/ 0.08 | 0.08/ 0.09 | 0.09/ 0.11 | 0.09/ 0.11 | 0.11/ 0.19 | ns |
| $T_{ISDCK\_DDLY}$ /$T_{ISCKD\_DDLY}$ | DDLY pin Setup/Hold with respect to CLK (using IODELAY)[(1)] | 0.10/ 0.05 | 0.12/ 0.06 | 0.14/ 0.07 | 0.14/ 0.07 | 0.16/ 0.15 | ns |
| $T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$ | D pin Setup/Hold with respect to CLK at DDR mode | 0.07/ 0.08 | 0.08/ 0.09 | 0.09/ 0.11 | 0.09/ 0.11 | 0.11/ 0.19 | ns |
| $T_{ISDCK\_DDLY\_DDR}$ $T_{ISCKD\_DDLY\_DDR}$ | D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY)[(1)] | 0.10/ 0.05 | 0.12/ 0.06 | 0.14/ 0.07 | 0.14/ 0.07 | 0.16/ 0.15 | ns |
| **Sequential Delays** | | | | | | | |
| $T_{ISCKO\_Q}$ | CLKDIV to out at Q pin | 0.57 | 0.66 | 0.75 | 0.80 | 0.88 | ns |
| **Propagation Delays** | | | | | | | |
| $T_{ISDO\_DO}$ | D input to DO output pin | 0.19 | 0.22 | 0.25 | 0.25 | 0.28 | ns |

**Notes:**

1. Recorded at 0 tap value.
2. $T_{ISCCK\_CE2}$ and $T_{ISCKC\_CE2}$ are reported as $T_{ISCCK\_CE}$/$T_{ISCKC\_CE}$ in TRACE report.

## Input/Output Delay Switching Characteristics

*Table 53:* **Input/Output Delay Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| **IDELAYCTRL** | | | | | | |
| $T_{DLYCCO\_RDY}$ | Reset to Ready for IDELAYCTRL | 3.00 | 3.00 | 3.00 | 3.25 | µs |
| $F_{IDELAYCTRL\_REF}$ | REFCLK frequency = 200.0[1] | 200 | 200 | 200 | 200 | MHz |
| | REFCLK frequency = 300.0[1] | 300 | 300 | – | – | MHz |
| IDELAYCTRL_REF_PRECISION | REFCLK precision | ±10 | ±10 | ±10 | ±10 | MHz |
| $T_{IDELAYCTRL\_RPW}$ | Minimum Reset pulse width | 50.00 | 50.00 | 50.00 | 52.50 | ns |
| **IODELAY** | | | | | | |
| $T_{IDELAYRESOLUTION}$ | IODELAY Chain Delay Resolution | 1/(32 x 2 x $F_{REF}$) | | | | ps |
| $T_{IDELAYPAT\_JIT}$ | Pattern dependent period jitter in delay chain for clock pattern.[2] | 0 | 0 | 0 | 0 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).[3] | ±5 | ±5 | ±5 | ±5 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).[4] | ±9 | ±9 | ±9 | ±9 | ps per tap |
| $T_{IODELAY\_CLK\_MAX}$ | Maximum frequency of CLK input to IODELAY | 500.00 | 420.00 | 300.00 | 300.00 | MHz |
| $T_{IODCCK\_CE}$ / $T_{IODCKC\_CE}$ | CE pin Setup/Hold with respect to CK | 0.45/ –0.09 | 0.53/ –0.09 | 0.65/ –0.09 | 0.84/ –0.14 | ns |
| $T_{IODCK\_INC}$/ $T_{IODCKC\_INC}$ | INC pin Setup/Hold with respect to CK | 0.23/ –0.02 | 0.27/ –0.01 | 0.31/ 0.00 | 0.27/ –0.04 | ns |
| $T_{IODCCK\_RST}$/ $T_{IODCKC\_RST}$ | RST pin Setup/Hold with respect to CK | 0.57/ –0.08 | 0.62/ –0.08 | 0.69/ –0.08 | 0.74/ –0.13 | ns |
| $T_{IODDO\_T}$ | TSCONTROL delay to MUXE/MUXF switching and through IODELAY | Note 5 | Note 5 | Note 5 | Note 5 | ps |
| $T_{IODDO\_IDATAIN}$ | Propagation delay through IODELAY | Note 5 | Note 5 | Note 5 | Note 5 | ps |
| $T_{IODDO\_ODATAIN}$ | Propagation delay through IODELAY | Note 5 | Note 5 | Note 5 | Note 5 | ps |

**Notes:**

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IODELAY tap setting. See TRACE report for actual values.

## CLB Switching Characteristics

*Table 54:* **CLB Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| **Combinatorial Delays** | | | | | | |
| $T_{ILO}$ | An – Dn LUT address to A | 0.06 | 0.07 | 0.07 | 0.09 | ns, Max |
| | An – Dn LUT address to AMUX/CMUX | 0.18 | 0.20 | 0.22 | 0.25 | ns, Max |
| | An – Dn LUT address to BMUX_A | 0.28 | 0.31 | 0.36 | 0.40 | ns, Max |

*Table 57:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $T_{RCCK\_WE}/T_{RCKC\_WE}$ | Write Enable (WE) input (Block RAM only) | 0.44/ 0.19 | 0.47/ 0.25 | 0.52/ 0.35 | 0.67/ 0.24 | ns, Min |
| $T_{RCCK\_WREN}/T_{RCKC\_WREN}$ | WREN FIFO inputs | 0.47/ 0.26 | 0.50/ 0.27 | 0.55/ 0.30 | 0.68/ 0.31 | ns, Min |
| $T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$ | RDEN FIFO inputs | 0.46/ 0.26 | 0.50/ 0.27 | 0.55/ 0.30 | 0.67/ 0.31 | ns, Min |
| **Reset Delays** | | | | | | |
| $T_{RCO\_FLAGS}$ | Reset RST to FIFO Flags/Pointers(10) | 0.90 | 0.98 | 1.10 | 1.23 | ns, Max |
| $T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$ | FIFO reset timing(11) | 0.22/ 0.23 | 0.24/ 0.24 | 0.28/ 0.26 | 0.31/ 0.27 | ns, Min |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | Block RAM in TDP and SDP modes (Write First and No Change modes) | 600 | 540 | 450 | 340 | MHz |
| | Block RAM (Read First mode) | 525 | 475 | 400 | 275 | MHz |
| | Block RAM (SDP mode)(12) | 525 | 475 | 400 | 275 | MHz |
| $F_{MAX\_CASCADE}$ | Block RAM Cascade (Write First and No Change modes) | 550 | 490 | 400 | 300 | MHz |
| | Block RAM Cascade (Read First mode) | 475 | 425 | 350 | 235 | MHz |
| $F_{MAX\_FIFO}$ | FIFO in all modes | 600 | 540 | 450 | 340 | MHz |
| $F_{MAX\_ECC}$ | Block RAM and FIFO in ECC configuration | 450 | 400 | 325 | 250 | MHz |

**Notes:**

1. TRACE will report all of these parameters as $T_{RCKO\_DO}$.
2. $T_{RCKO\_DOR}$ includes $T_{RCKO\_DOW}$, $T_{RCKO\_DOPR}$, and $T_{RCKO\_DOPW}$ as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. $T_{RCKO\_DO}$ includes $T_{RCKO\_DOP}$ as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. $T_{RCKO\_FLAGS}$ includes the following parameters: $T_{RCKO\_AEMPTY}$, $T_{RCKO\_AFULL}$, $T_{RCKO\_EMPTY}$, $T_{RCKO\_FULL}$, $T_{RCKO\_RDERR}$, $T_{RCKO\_WRERR}$.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. $T_{RCKO\_DI}$ includes both A and B inputs as well as the parity inputs of A and B.
10. $T_{RCO\_FLAGS}$ includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. The FIFO reset must be asserted for at least three positive clock edges.
12. When using ISE software v12.4 or later, if the RDADDR_COLLISION_HWCONFIG attribute is set to PERFORMANCE or the block RAM is in single-port operation, then the faster $F_{MAX}$ for WRITE_FIRST/NO_CHANGE modes apply.

*Table 62:* **Regional Clock Switching Characteristics (BUFR) *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $T_{BRDO\_O}$ | Propagation delay from CLR to O | 0.69 | 0.74 | 0.80 | 1.12 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$(1) | Regional clock tree (BUFR) | 500 | 420 | 300 | 300 | MHz |

**Notes:**

1. The maximum input frequency to the BUFR is the BUFIO $F_{MAX}$ frequency.

*Table 63:* **Horizontal Clock Buffer Switching Characteristics (BUFH)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $T_{BHCKO\_O}$ | BUFH delay from I to O | 0.10 | 0.11 | 0.13 | 0.15 | ns |
| $T_{BHCCK\_CE}/T_{BHCKC\_CE}$ | CE pin Setup and Hold | 0.04/ 0.04 | 0.04/ 0.04 | 0.05/ 0.05 | 0.04/ 0.04 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | Horizontal clock buffer (BUFH) | 800 | 750 | 700 | 667 | MHz |

## MMCM Switching Characteristics

*Table 64:* **MMCM Specification**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $F_{INMAX}$ | Maximum Input Clock Frequency(1) | 800 | 750 | 700 | 700 | MHz |
| $F_{INMIN}$ | Minimum Input Clock Frequency | 10 | 10 | 10 | 10 | MHz |
| $F_{INJITTER}$ | Maximum Input Clock Period Jitter | < 20% of clock input period or 1 ns Max | | | | |
| $F_{INDUTY}$(2) | Allowable Input Duty Cycle: 10—49 MHz | 25/75 | | | | % |
| | Allowable Input Duty Cycle: 50—199 MHz | 30/70 | | | | % |
| | Allowable Input Duty Cycle: 200—399 MHz | 35/65 | | | | % |
| | Allowable Input Duty Cycle: 400—499 MHz | 40/60 | | | | % |
| | Allowable Input Duty Cycle: >500 MHz | 45/55 | | | | % |
| $F_{MIN\_PSCLK}$ | Minimum Dynamic Phase Shift Clock Frequency | 0.01 | 0.01 | 0.01 | 0.01 | MHz |
| $F_{MAX\_PSCLK}$ | Maximum Dynamic Phase Shift Clock Frequency | 550 | 500 | 450 | 450 | MHz |
| $F_{VCOMIN}$ | Minimum MMCM VCO Frequency | 600 | 600 | 600 | 600 | MHz |
| $F_{VCOMAX}$ | Maximum MMCM VCO Frequency | 1600 | 1440 | 1200 | 1200 | MHz |
| $F_{BANDWIDTH}$ | Low MMCM Bandwidth at Typical(3) | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High MMCM Bandwidth at Typical(3) | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| $T_{STATPHAOFFSET}$ | Static Phase Offset of the MMCM Outputs(4) | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| $T_{OUTJITTER}$ | MMCM Output Jitter(5) | Note 3 | | | | |
| $T_{OUTDUTY}$ | MMCM Output Clock Duty Cycle Precision(6) | 0.15 | 0.20 | 0.20 | 0.20 | ns |
| $T_{LOCKMAX}$ | MMCM Maximum Lock Time | 100 | 100 | 100 | 100 | µs |
| $F_{OUTMAX}$ | MMCM Maximum Output Frequency | 800 | 750 | 700 | 700 | MHz |
| $F_{OUTMIN}$ | MMCM Minimum Output Frequency(7)(8) | 4.69 | 4.69 | 4.69 | 4.69 | MHz |
| $T_{EXTFDVAR}$ | External Clock Feedback Variation | < 20% of clock input period or 1 ns Max | | | | |

*Table 64:* **MMCM Specification *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $RST_{MINPULSE}$ | Minimum Reset Pulse Width | 1.5 | 1.5 | 1.5 | 1.5 | ns |
| $F_{PFDMAX}$ | Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized(9) | 550 | 500 | 450 | 450 | MHz |
| | Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low | 300 | 300 | 300 | 300 | MHz |
| $F_{PFDMIN}$ | Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized | 135 | 135 | 135 | 135 | MHz |
| | Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to Low | 10 | 10 | 10 | 10 | MHz |
| $T_{FBDELAY}$ | Maximum Delay in the Feedback Path | 3 ns Max or one CLKIN cycle | | | | |
| $T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$ | Setup and Hold of Phase Shift Enable | 1.04<br>0.00 | 1.04<br>0.00 | 1.04<br>0.00 | 1.04<br>0.00 | ns |
| $T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$ | Setup and Hold of Phase Shift Increment/Decrement | 1.04<br>0.00 | 1.04<br>0.00 | 1.04<br>0.00 | 1.04<br>0.00 | ns |
| $T_{MMCMCKO\_PSDONE}$ | Phase Shift Clock-to-Out of PSDONE | 0.32 | 0.34 | 0.38 | 0.38 | ns |

**Notes:**

1. When DIVCLK_DIVIDE = 3 or 4, $F_{INMAX}$ is 315 MHz.
2. This duty cycle specification does not apply to the GTH_QUAD (GTH) to MMCM connection. The GTH transceivers drive the MMCMs at the following maximum frequencies: 323 MHz for -1 speed grade devices, 350 MHz for -2 speed grade devices, or 350 MHz for -3 speed grade devices.
3. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. The static offset is measured between any MMCM outputs with identical phase.
5. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
6. Includes global clock buffer.
7. Calculated as $F_{VCO}$/128 assuming output duty cycle is 50%.
8. When CASCADE4_OUT = TRUE, $F_{OUTMIN}$ is 0.036 MHz.
9. In ISE software 12.3 (or earlier versions supporting the Virtex-6 family), the phase frequency detector Optimized bandwidth setting is equivalent to the High bandwidth setting. Starting with ISE software 12.4, the Optimized bandwidth setting is automatically adjusted to Low when the software can determine that the phase frequency detector input is less than 135 MHz.

*Table 67:* **Clock-Capable Clock Input to Output Delay With MMCM**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1L | |
| LVCMOS25 Clock-capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM. | | | | | | | |
| $T_{ICKOFMMCMCC}$ | Clock-capable Clock Input and OUTFF *with* MMCM | XC6VLX75T | 2.22 | 2.38 | 2.63 | 2.72 | ns |
| | | XC6VLX130T | 2.24 | 2.39 | 2.65 | 2.74 | ns |
| | | XC6VLX195T | 2.24 | 2.40 | 2.65 | 2.75 | ns |
| | | XC6VLX240T | 2.24 | 2.40 | 2.65 | 2.75 | ns |
| | | XC6VLX365T | 2.25 | 2.42 | 2.65 | 2.76 | ns |
| | | XC6VLX550T | N/A | 2.43 | 2.68 | 2.80 | ns |
| | | XC6VLX760 | N/A | 2.42 | 2.69 | 2.79 | ns |
| | | XC6VSX315T | 2.23 | 2.38 | 2.65 | 2.73 | ns |
| | | XC6VSX475T | N/A | 2.30 | 2.57 | 2.66 | ns |
| | | XC6VHX250T | 2.25 | 2.41 | 2.67 | N/A | ns |
| | | XC6VHX255T | 2.35 | 2.51 | 2.78 | N/A | ns |
| | | XC6VHX380T | 2.27 | 2.43 | 2.69 | N/A | ns |
| | | XC6VHX565T | N/A | 2.41 | 2.68 | N/A | ns |
| | | XQ6VLX130T | N/A | 2.39 | 2.65 | 2.74 | ns |
| | | XQ6VLX240T | N/A | 2.40 | 2.65 | 2.75 | ns |
| | | XQ6VLX550T | N/A | N/A | 2.68 | 2.80 | ns |
| | | XQ6VSX315T | N/A | 2.38 | 2.65 | 2.73 | ns |
| | | XQ6VSX475T | N/A | N/A | 2.57 | 2.66 | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

*Table 72:* **Package Skew**

| Symbol | Description | Device | Package | Value | Units |
|---|---|---|---|---|---|
| $T_{PKGSKEW}$ | Package Skew[1] | XC6VLX75T | FF484 | 95 | ps |
| | | | FF784 | 146 | ps |
| | | XC6VLX130T | FF484 | 95 | ps |
| | | | FF784 | 146 | ps |
| | | | FF1156 | 165 | ps |
| | | XC6VLX195T | FF784 | 145 | ps |
| | | | FF1156 | 182 | ps |
| | | XC6VLX240T | FF784 | 146 | ps |
| | | | FF1156 | 182 | ps |
| | | | FF1759 | 187 | ps |
| | | XC6VLX365T | FF1156 | 189 | ps |
| | | | FF1759 | 184 | ps |
| | | XC6VLX550T | FF1759 | 196 | ps |
| | | | FF1760 | 249 | ps |
| | | XC6VLX760 | FF1760 | 236 | ps |
| | | XC6VSX315T | FF1156 | 168 | ps |
| | | | FF1759 | 190 | ps |
| | | XC6VSX475T | FF1156 | 168 | ps |
| | | | FF1759 | 204 | ps |
| | | XC6VHX250T | FF1154 | 166 | ps |
| | | XC6VHX255T | FF1155 | 168 | ps |
| | | | FF1923 | 228 | ps |
| | | XC6VHX380T | FF1154 | 159 | ps |
| | | | FF1155 | 172 | ps |
| | | | FF1923 | 227 | ps |
| | | | FF1924 | 220 | ps |
| | | XC6VHX565T | FF1923 | 232 | ps |
| | | | FF1924 | 197 | ps |
| | | XQ6VLX130T | RF784 | 146 | ps |
| | | | RF1156 | 165 | ps |
| | | | FFG1156 | 165 | ps |
| | | XQ6VLX240T | RF784 | 146 | ps |
| | | | RF1156 | 182 | ps |
| | | | FFG1156 | 182 | ps |
| | | | RF1759 | 187 | ps |
| | | XQ6VLX550T | RF1759 | 196 | ps |
| | | XQ6VSX315T | RF1156 | 168 | ps |
| | | | FFG1156 | 168 | ps |
| | | | RF1759 | 190 | ps |
| | | XQ6VSX475T | RF1156 | 168 | ps |
| | | | FFG1156 | 168 | ps |
| | | | RF1759 | 204 | ps |

**Notes:**

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

| Date | Version | Description of Revisions |
|---|---|---|
| 02/08/11 | 2.12 | Removed note 1 from Table 4 as the larger devices (XC6VLX550T, XC6VLX760, XC6VSX475T, and XC6VHX565T) are now offered in -2I. Updated Table 4 and Table 5 with data for the XC6VHX380T in the FF(G)1154 package. In Table 41, updated -1L specification for DDR3. Added Note 1 to Table 42. Moved the XC6VHX380Tdevices in the FF(G)1154 package to production release in Table 43 using ISE 12.4 software with current speed specifications. Updated description for $F_{INDUTY}$ in Table 64. |
| 02/25/11 | 3.0 | Designated the data sheet as Preliminary for all devices not already labeled production in Table 42. Changed the XC6VHX380T devices in all packages to production status in Table 42 and Table 43. Removed note 1 from Table 42.<br>Added maximum specifications to Table 25. Updated $T_{HAVCC2HAVCCRX}$ in Table 27. Updated the typical values and notes in Table 28 and Table 29. Added values to Table 30 and Table 31. In Table 34, added values for $T_{LOCK}$ and $T_{PHASE}$. Updated the values in Table 36 and added note 3. Updated Table 37 and added note 4. |
| 03/21/11 | 3.1 | Updated Table 2 including Note 7. In Table 4, added Note 3 and -2E, extended temperature range to the XC6VLX550T, XC6VLX760, XC6VSX475T, and XC6VHX380T devices, and added Note 5 for the XC6VHX565T. Updated Table 28 typical values. Updated the description for $F_{IDELAYCTRL\_REF}$ in Table 53. Updated $F_{MCCK}$ in Table 59. |
| 04/01/11 | 3.2 | Added Tj values for C, E, and I temperature ranges to Table 2. Updated the $I_{CCQ}$ values in Table 4. Updated $F_{GCLK}$ in Table 34.<br>Designated the data sheet as Production for all devices not already labeled production in Table 42. Changed the XC6VHX255T and XC6VHX565T devices in all packages to production status in Table 42 and Table 43. This included updates to the Virtex-6 Device Pin-to-Pin Output Parameter Guidelines and Virtex-6 Device Pin-to-Pin Input Parameter Guidelines for these devices. Production speed specifications for these devices are available using the speed specification v1.14 in the ISE 13.1 software update.<br>Updated and added package skew values to Table 72; these values are correct with regards to previous production released speed specifications in software. Updated copyright page 1 and Notice of Disclaimer. |
| 12/08/11 | 3.3 | Production release of the Defense-grade XQ devices in Table 42 and Table 43 using ISE v13.3 v1.17 Patch for -2 and -1 speed specifications; and v1.10 for -1L speed specifications. Added the XQ6VLX130T, XQ6VLX240T, XQ6VLX550T, XQ6VSX315T, and XQ6VSX475T to the data sheet which included adding Table 45. Updated $T_j$ in Table 2. In Table 40, updated $T_j$ for most specifications and added Note 4. Added Note 4 to Table 41. Added -1(XQ) speed specification columns only to Table 50, Table 51, Table 52, and Table 58.<br>Updated $V_{OD}$ in Table 8, $V_{OCM}$ in Table 9, and $V_{OCM}$ and $V_{DIFF}$ in Table 10. Updated the Power-On Power Supply Requirements section. In Table 27, updated maximum specification for $T_{HAVCC2HAVCCRX}$ and added Note 3. Updated Tj in Table 40. In Table 41, increased the DDR LVDS receiver (SPI-4.2) -1 speed grade performance value from 1.0 Gb/s to 1.1 Gb/s. In Table 60, updated the $F_{MAX}$ to add a separate row for the LX760 device values. The speed specifications in the software tools have always matched these values for the LX760, the data sheet is now correct. Updated the notes for $T_{OUTJITTER}$ in Table 64. |
| 01/12/12 | 3.4 | Added the temperature range -2E to Note 5 in Table 4. |