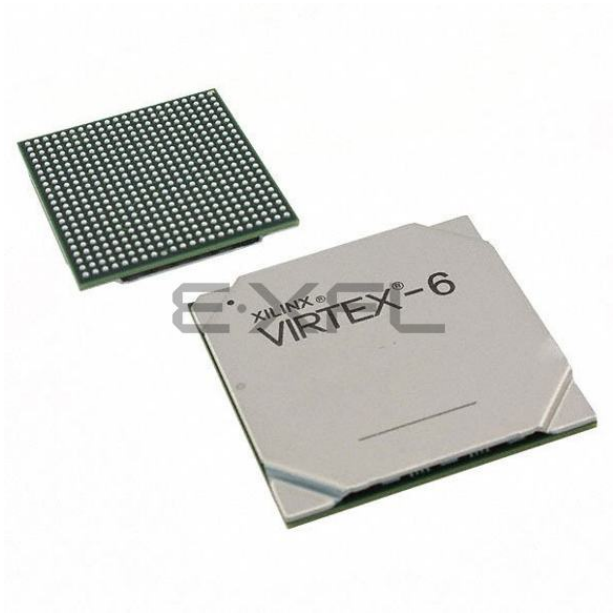
AMD Xilinx - XC6VLX240T-2FFG784I Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	18840
Number of Logic Elements/Cells	241152
Total RAM Bits	15335424
Number of I/O	400
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	784-BBGA, FCBGA
Supplier Device Package	784-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vlx240t-2ffg784i

Table 3: **DC Characteristics Over Recommended Operating Conditions (1)(2)**

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	10	µA
I_L	Input or output leakage current per pin (sample-tested)	–	–	10	µA
C_{IN}(3)	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V	20	–	80	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	8	–	40	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	5	–	30	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V	1	–	20	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 2.5V	3	–	80	µA
I_{BATT}	Battery supply current	–	–	150	nA
n	Temperature diode ideality factor	–	1.0002	–	n
r	Series resistance	–	5	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst case process at 25°C.
3. This measurement represents the die capacitance at the pad, not including the package.

Table 4: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed and Temperature Grade						Units
			-3 (C)	-2 (C, E, & I)	-1 (C & I)	-1 (I & M)(2)	-1L (C)	-1L (I)(1)	
I_{CCOQ}	Quiescent V_{CCO} supply current	XC6VLX75T	1	1	1	N/A	1	1	mA
		XC6VLX130T	1	1	1	N/A	1	1	mA
		XC6VLX195T	1	1	1	N/A	1	1	mA
		XC6VLX240T	2	2	2	N/A	2	2	mA
		XC6VLX365T	2	2	2	N/A	2	2	mA
		XC6VLX550T(3)	N/A	3	3	N/A	3	3	mA
		XC6VLX760(3)	N/A	3	3	N/A	3	3	mA
		XC6VSX315T	2	2	2	N/A	2	2	mA
		XC6VSX475T(3)	N/A	2	2	N/A	2	2	mA
		XC6VHX250T	1	1	1	N/A	N/A	N/A	mA
		XC6VHX255T	1	1	1	N/A	N/A	N/A	mA
		XC6VHX380T(4)	2	2	2	N/A	N/A	N/A	mA
		XC6VHX565T(5)	N/A	2	2	N/A	N/A	N/A	mA
		XQ6VLX130T	N/A	1	N/A	1	N/A	1	mA
		XQ6VLX240T	N/A	2	N/A	2	N/A	2	mA
		XQ6VLX550T(7)	N/A	N/A	N/A	3	N/A	3	mA
		XQ6VSX315T	N/A	2	N/A	2	N/A	2	mA
		XQ6VSX475T(7)	N/A	N/A	N/A	2	N/A	2	mA

Table 4: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed and Temperature Grade						Units
			-3 (C)	-2 (C, E, & I)	-1 (C & I)	-1 (I & M)(2)	-1L (C)	-1L (I)(1)	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC6VLX75T	45	45	45	N/A	45	45	mA
		XC6VLX130T	75	75	75	N/A	75	75	mA
		XC6VLX195T	113	113	113	N/A	113	113	mA
		XC6VLX240T	135	135	135	N/A	135	135	mA
		XC6VLX365T	191	191	191	N/A	191	191	mA
		XC6VLX550T(3)	N/A	286	286	N/A	286	286	mA
		XC6VLX760(3)	N/A	387	387	N/A	387	387	mA
		XC6VSX315T	186	186	186	N/A	186	186	mA
		XC6VSX475T(3)	N/A	279	279	N/A	279	279	mA
		XC6VHX250T	152	152	152	N/A	N/A	N/A	mA
		XC6VHX255T	152	152	152	N/A	N/A	N/A	mA
		XC6VHX380T(4)	227	227	227	N/A	N/A	N/A	mA
		XC6VHX565T(5)	N/A	315	315	N/A	N/A	N/A	mA
		XQ6VLX130T(6)	N/A	75	N/A	75	N/A	75	mA
		XQ6VLX240T(6)	N/A	135	N/A	135	N/A	135	mA
		XQ6VLX550T(7)	N/A	N/A	N/A	286	N/A	286	mA
		XQ6VSX315T(6)	N/A	186	N/A	186	N/A	186	mA
		XQ6VSX475T(7)	N/A	N/A	N/A	279	N/A	279	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j). -1 and -2 industrial (I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. -1L industrial temperature range devices have the values specified in this column.
2. Use the XPE tool to calculate 125°C values for -1M temperature range devices.
3. The -2E extended temperature range (T_j = 0°C to +100°C) is only available in these devices. The -2I temperature range (T_j = –40°C to +100°C) is available for all other devices except the XC6VHX565T.
4. The XC6VHX380T is available with both -2E and -2I temperature ranges.
5. The XC6VHX565T is only available in the following temperature ranges: -1C, -1I, -2C, and -2E.
6. The XQ6VLX130T, XQ6VLX240T, and XQ6VSX315T are available in -2I, -1I, -1M, and -1LI temperature ranges.
7. The XQ6VLX550T and the XQ6VSX475T are only available in -1I and -1LI temperature ranges.
8. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
9. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPE or XPower Analyzer (XPA) tools.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on sequence and ramp rate of the power supply.

The recommended power-on sequence for Virtex-6 devices is V_{CCINT}, V_{CCAUX}, and V_{CCO} to meet the power-up current requirements listed in Table 5. V_{CCINT} can be powered up or down at any time, but power up current specifications can vary from Table 5. The device will have no physical damage or reliability concerns if V_{CCINT}, V_{CCAUX}, and V_{CCO} sequence cannot be followed.

If the recommended power-up sequence cannot be followed and the I/Os must remain 3-stated throughout configuration, then V_{CCAUX} must be powered prior to V_{CCO} or V_{CCAUX} and V_{CCO} must be powered by the same supply. Similarly, for power-down, the reverse V_{CCAUX} and V_{CCO} sequence is recommended if the I/Os are to remain 3-stated.

The GTH transceiver supplies must be powered using a MGTHAVCC, MGTHAVCCRX, MGTHAVCCPLL, and MGTHAVTT sequence. There are no sequencing requirement for these supplies with respect to the other FPGA supply voltages. For more detail see Table 27: *GTH Transceiver Power Supply Sequencing*. There are no sequencing requirements for the GTX transceivers power supplies.

Table 5 shows the minimum current, in addition to I_{CCQ}, that are required by Virtex-6 devices for proper power-on and configuration. If the current minimums shown in Table 4 and Table 5 are met, the device powers on after all three supplies have passed through their power-on reset threshold voltages. The FPGA must be configured after applying V_{CCINT}, V_{CCAUX}, and V_{CCO} for the appropriate configuration banks. Once initialized and configured, use the XPE tools to estimate current drain on these supplies.

Table 5: **Power-On Current for Virtex-6 Devices**

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	Units
	Typ(1)	Typ(1)	Typ(1)	
XC6VLX75T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 10	I_{CCOQ} + 30 mA per bank	mA
XC6VLX130T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 10	I_{CCOQ} + 30 mA per bank	mA
XC6VLX195T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VLX240T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VLX365T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VLX550T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VLX760	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VSX315T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VSX475T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 50	I_{CCOQ} + 30 mA per bank	mA
XC6VHX250T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VHX255T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VHX380T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VHX565T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XQ6VLX130T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 100	I_{CCOQ} + 30 mA per bank	mA
XQ6VLX240T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 100	I_{CCOQ} + 30 mA per bank	mA
XQ6VLX550T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 100	I_{CCOQ} + 30 mA per bank	mA
XQ6VSX315T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 100	I_{CCOQ} + 40 mA per bank	mA
XQ6VSX475T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 100	I_{CCOQ} + 40 mA per bank	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Use the XPower Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.

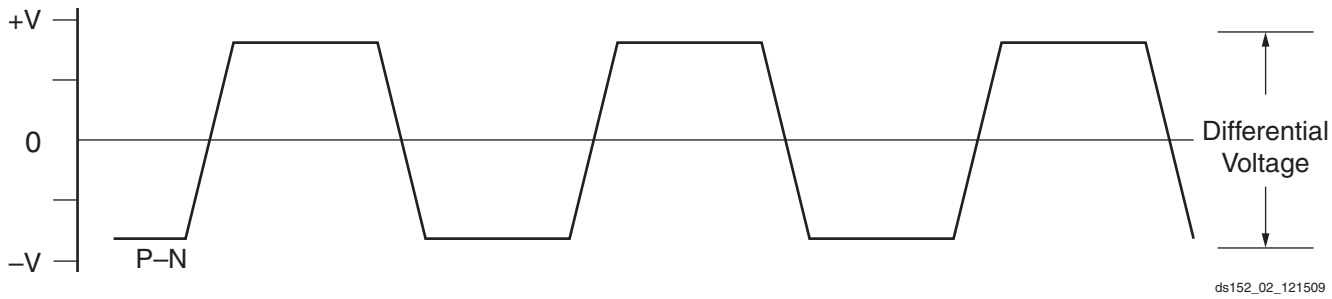

Figure 2: **Differential Peak-to-Peak Voltage**

Table 18 summarizes the DC specifications of the clock input of the GTX transceiver. Consult UG366: *Virtex-6 FPGA GTX Transceivers User Guide* for further details.

Table 18: **GTX Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	210	800	2000	mV
R_{IN}	Differential input resistance	90	100	130	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTX Transceiver Switching Characteristics

Consult UG366: *Virtex-6 FPGA GTX Transceivers User Guide* for further information.

Table 19: **GTX Transceiver Performance**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F_{GTXMAX}	Maximum GTX transceiver data rate	6.6	6.6	5.0	5.0	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	3.3(1)	3.3(1)	2.7	2.7	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.2	1.2	1.2	1.2	GHz

Notes:

1. See Table 14 for MGTAVCC requirements when PLL frequency is greater than 2.7 GHz.

Table 20: **GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	150	150	125	100	MHz

Table 24: **GTX Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTXRX}	Serial data rate	RX oversampler not enabled	0.600	–	F_{GTXMAX}	Gb/s
		RX oversampler enabled	0.480	–	0.600	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–	75	–	ns
$RX_{OOBVDPP}$	OOB detect threshold peak-to-peak		60	–	150	mV
RX_{SST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000	–	0	ppm
RX_{RL}	Run length (CID)	Internal AC capacitor bypassed	–	–	512	UI
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance	CDR 2nd-order loop disabled	–200	–	200	ppm
		CDR 2nd-order loop enabled	–2000	–	2000	ppm
SJ Jitter Tolerance(2)						
$JT\_SJ_{6.5}$	Sinusoidal Jitter(3)	6.5 Gb/s	0.44	–	–	UI
$JT\_SJ_{5.0}$	Sinusoidal Jitter(3)	5.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{4.25}$	Sinusoidal Jitter(3)	4.25 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.75}$	Sinusoidal Jitter(3)	3.75 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.125}$	Sinusoidal Jitter(3)	3.125 Gb/s	0.45	–	–	UI
$JT\_SJ_{3.125L}$	Sinusoidal Jitter(3)	3.125 Gb/s(4)	0.45	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter(3)	2.5 Gb/s(5)	0.5	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter(3)	1.25 Gb/s(6)	0.5	–	–	UI
JT_SJ_{600}	Sinusoidal Jitter(3)	600 Mb/s	0.4	–	–	UI
JT_SJ_{480}	Sinusoidal Jitter(3)	480 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$JT\_TJSE_{3.125}$	Total Jitter with Stressed Eye(7)	3.125 Gb/s	0.70	–	–	UI
		5.0 Gb/s	0.70	–	–	UI
$JT\_SJSE_{3.125}$	Sinusoidal Jitter with Stressed Eye(7)	3.125 Gb/s	0.1	–	–	UI
		5.0 Gb/s	0.1	–	–	UI

Notes:

1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. PLL frequency at 1.5625 GHz and OUTDIV = 1.
5. PLL frequency at 2.5 GHz and OUTDIV = 2.
6. PLL frequency at 2.5 GHz and OUTDIV = 4.
7. Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Specifications

GTH Transceiver DC Characteristics

Table 25: **Absolute Maximum Ratings for GTH Transceivers(1)**

Symbol	Description	Min	Max	Units
MGTHAVCC	Analog supply voltage for the GTH transmitter, receiver, and common analog circuits	–0.5	1.125	V
MGTHAVCCRX	Analog supply voltage for the GTH receiver circuits and common analog circuits	–0.5	1.125	V
MGTHAVTT	Analog supply voltage for the GTH transmitter termination circuits	–0.5	1.32	V
MGTHAVCCPLL	Analog supply voltage for the GTH receiver and PLL circuits	–0.5	1.935	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.125	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.935	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 26: **Recommended Operating Conditions for GTH Transceivers (1)(2)**

Symbol	Description	Min	Typ	Max	Units
MGTHAVCC	Analog supply voltage for the GTH transmitter, receiver, and common analog circuits	1.075	1.1	1.125	V
MGTHAVCCRX	Analog supply voltage for the GTH receiver circuits and common analog circuits	1.075	1.1	1.125	V
MGTHAVTT	Analog supply voltage for the GTH transmitter termination circuits	1.140	1.2	1.26	V
MGTHAVCCPLL	Analog supply voltage for the GTH receiver and PLL circuit	1.710	1.8	1.89	V

Notes:

1. Each voltage listed requires the filter circuit described in UG371: *Virtex-6 FPGA GTH Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +100°C.

Table 27: **GTH Transceiver Power Supply Sequencing (1)(2)(3)**

Symbol	Description	Min	Max	Units
$T_{HAVCC2HAVCCRX}$	Maximum time between powering MGTHAVCC to when MGTHAVCCRX must be powered.	0	5	ms
$T_{HAVCCRX2HAVCCPLL}$	Minimum time between powering MGTHAVCCRX to when MGTHAVCCPLL can be powered.	10	–	µs
$T_{HAVCCRX2HAVTT}$	Minimum time between powering MGTHAVCCRX to when MGTHAVTT can be powered.	10	–	µs

Notes:

1. MGTHAVCCRX must be powered simultaneously or within $T_{HAVCC2HAVCCRX}$ of MGTHAVCC, but it must not precede MGTHAVCC.
2. MGTHAVCC and MGTHAVCCRX must be powered before MGTHAVCCPLL and MGTHAVTT. This minimum time is defined by $T_{HAVCCRX2HAVCCPLL}$ and $T_{HAVCCRX2HAVTT}$.
3. At any time, the condition of MGTHAVCC being present and MGTHAVCCRX not being present should not occur for more than the maximum $T_{HAVCC2HAVCCRX}$.

Table 37: **GTH Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
R_{XRL}	Run length (CID)		8000	–	–	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance		–200	–	200	ppm
SJ Jitter Tolerance(1)(2)(3)(4)						
$JT\_SJ_{11.18}$	Sinusoidal Jitter	11.18 Gb/s	0.3	–	–	UI
$JT\_SJ_{10.32}$	Sinusoidal Jitter	10.32 Gb/s	0.3	–	–	UI
$JT\_SJ_{9.95}$	Sinusoidal Jitter	9.95 Gb/s	0.3	–	–	UI
$JT\_SJ_{2.667}$	Sinusoidal Jitter	2.667 Gb/s	0.5	–	–	UI
$JT\_SJ_{2.48}$	Sinusoidal Jitter	2.48 Gb/s	0.5	–	–	UI

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. High-frequency jitter tolerance including 6 db of channel loss at a high frequency of the data rate divided by two.

Ethernet MAC Switching Characteristics

Consult UG368: *Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide* for further information.

Table 38: **Maximum Ethernet MAC Performance**

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1	-1L	
$F_{TEMACCLIENT}$	Client interface maximum frequency	10 Mb/s – 8-bit width	2.5(1)	2.5(1)	2.5(1)	2.5(1)	MHz
		100 Mb/s – 8-bit width	25(2)	25(2)	25(2)	25(2)	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		1000 Mb/s – 16-bit width	62.5	62.5	62.5	62.5	MHz
		2000 Mb/s – 16-bit width	125	125	125	N/A	MHz
		2500 Mb/s – 16-bit width	156.25	156.25	156.25	N/A	MHz
$F_{TEMACPHY}$	Physical interface maximum frequency	10 Mb/s – 4-bit width	2.5	2.5	2.5	2.5	MHz
		100 Mb/s – 4-bit width	25	25	25	25	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		2000 Mb/s – 8-bit width	250	250	250	N/A	MHz
		2500 Mb/s – 8-bit width	312.5	312.5	312.5	N/A	MHz

Notes:

1. When not using clock enable, the F_{MAX} is lowered to 1.25 MHz.
2. When not using clock enable, the F_{MAX} is lowered to 12.5 MHz.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

Table 39: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$F_{PIPECLK}$	Pipe clock maximum frequency	250	250	250	250	MHz
$F_{USERCLK}$	User clock maximum frequency	500	500	250	250	MHz
F_{DRPCLK}	DRP clock maximum frequency	250	250	250	250	MHz

System Monitor Analog-to-Digital Converter Specification

Table 40: **Analog-to-Digital Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
AV_{DD} = 2.5V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_j = –55°C to 125°C M-Grade, Typical values at T_j=+35°C						
DC Accuracy: All external input channels. Both unipolar and bipolar modes.						
Resolution			10	–	–	Bits
Integral Nonlinearity	INL		–	–	±1	LSBs
Differential Nonlinearity	DNL	No missing codes (T_{MIN} to T_{MAX}) Guaranteed Monotonic	–	–	±0.9	LSBs
Unipolar Offset Error (1)		Uncalibrated	–	±2	±30	LSBs
Bipolar Offset Error (1)		Uncalibrated measured in bipolar mode	–	±2	±30	LSBs
Gain Error		Uncalibrated - External Reference	–	±0.2	±2	%
		Uncalibrated - Internal Reference	–	±2	–	%
Bipolar Gain Error (1)		Uncalibrated - External Reference	–	±0.2	±2	%
		Uncalibrated - Internal Reference	–	±2	–	%
Total Unadjusted Error (Uncalibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	–	±10	–	LSBs
		Deviation from ideal transfer function. Internal reference	–	±20	–	LSBs
Total Unadjusted Error (Calibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	–	±1	±2	LSBs
Calibrated Gain Temperature Coefficient		Variation of FS code with temperature	–	±0.01	–	LSB/°C
DC Common-Mode Reject	$CMRR_{DC}$	$V_N = V_{CM}$ = 0.5V ± 0.5V, $V_P – V_N$ = 100mV	–	70	–	dB
Conversion Rate(2)						
Conversion Time - Continuous	t_{CONV}	Number of CLK cycles	26	–	32	
Conversion Time - Event	t_{CONV}	Number of CLK cycles	–	–	21	
T/H Acquisition Time	t_{ACQ}	Number of CLK cycles	4	–	–	
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	80	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
CLK Duty cycle			40	–	60	%

IOB Pad Input/Output/3-State Switching Characteristics

Table 44 (for commercial (XC) Virtex-6 devices) and Table 45 (for the Defense-grade (XQ) Virtex-6 devices) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 46 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 44: **IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDS_25	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
LVDSEXT_25	0.85	0.94	1.09	1.08	1.53	1.65	1.84	1.73	1.53	1.65	1.84	1.73	ns
HT_25	0.85	0.94	1.09	1.08	1.51	1.62	1.78	1.69	1.51	1.62	1.78	1.69	ns
BLVDS_25	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.65	1.39	1.50	1.67	1.65	ns
RSDS_25 (point to point)	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
HSTL_I	0.81	0.91	1.06	1.06	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns
HSTL_II	0.81	0.91	1.06	1.06	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
HSTL_III	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
HSTL_I_18	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
HSTL_II_18	0.81	0.91	1.06	1.06	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
HSTL_III_18	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
SSTL2_I	0.81	0.91	1.06	1.06	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
SSTL2_II	0.81	0.91	1.06	1.06	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
LVCMOS25, Slow, 2 mA	0.51	0.57	0.66	0.70	5.09	5.46	6.01	5.63	5.09	5.46	6.01	5.63	ns
LVCMOS25, Slow, 4 mA	0.51	0.57	0.66	0.70	3.30	3.49	3.79	3.65	3.30	3.49	3.79	3.65	ns
LVCMOS25, Slow, 6 mA	0.51	0.57	0.66	0.70	2.62	2.81	3.08	2.95	2.62	2.81	3.08	2.95	ns
LVCMOS25, Slow, 8 mA	0.51	0.57	0.66	0.70	2.21	2.41	2.72	2.59	2.21	2.41	2.72	2.59	ns
LVCMOS25, Slow, 12 mA	0.51	0.57	0.66	0.70	1.80	1.95	2.17	2.10	1.80	1.95	2.17	2.10	ns
LVCMOS25, Slow, 16 mA	0.51	0.57	0.66	0.70	1.89	2.05	2.29	2.21	1.89	2.05	2.29	2.21	ns
LVCMOS25, Slow, 24 mA	0.51	0.57	0.66	0.70	1.68	1.82	2.02	1.98	1.68	1.82	2.02	1.98	ns
LVCMOS25, Fast, 2 mA	0.51	0.57	0.66	0.70	5.12	5.49	6.04	5.62	5.12	5.49	6.04	5.62	ns
LVCMOS25, Fast, 4 mA	0.51	0.57	0.66	0.70	3.28	3.50	3.82	3.65	3.28	3.50	3.82	3.65	ns
LVCMOS25, Fast, 6 mA	0.51	0.57	0.66	0.70	2.56	2.73	2.99	2.88	2.56	2.73	2.99	2.88	ns
LVCMOS25, Fast, 8 mA	0.51	0.57	0.66	0.70	2.11	2.33	2.65	2.53	2.11	2.33	2.65	2.53	ns
LVCMOS25, Fast, 12 mA	0.51	0.57	0.66	0.70	1.74	1.88	2.08	2.03	1.74	1.88	2.08	2.03	ns
LVCMOS25, Fast, 16 mA	0.51	0.57	0.66	0.70	1.77	1.92	2.13	2.08	1.77	1.92	2.13	2.08	ns

Table 44: **IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDCI_DV2_25	0.51	0.57	0.66	0.70	1.71	1.83	2.01	2.00	1.71	1.83	2.01	2.00	ns
LVDCI_DV2_18	0.55	0.61	0.71	0.73	1.69	1.81	2.00	1.98	1.69	1.81	2.00	1.98	ns
LVDCI_DV2_15	0.64	0.73	0.85	0.85	1.68	1.77	1.91	1.98	1.68	1.77	1.91	1.98	ns
LVPECL_25	0.85	0.94	1.09	1.08	1.38	1.49	1.65	1.64	1.38	1.49	1.65	1.64	ns
HSTL_I_12	0.81	0.91	1.06	1.06	1.48	1.60	1.78	1.74	1.48	1.60	1.78	1.74	ns
HSTL_I_DCI	0.81	0.91	1.06	1.06	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
HSTL_II_DCI	0.81	0.91	1.06	1.06	1.37	1.49	1.68	1.66	1.37	1.49	1.68	1.66	ns
HSTL_II_T_DCI	0.81	0.91	1.06	1.06	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
HSTL_III_DCI	0.81	0.91	1.06	1.06	1.34	1.45	1.62	1.61	1.34	1.45	1.62	1.61	ns
HSTL_I_DCI_18	0.81	0.91	1.06	1.06	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
HSTL_II_DCI_18	0.81	0.91	1.06	1.06	1.36	1.46	1.62	1.59	1.36	1.46	1.62	1.59	ns
HSTL_II _T_DCI_18	0.81	0.91	1.06	1.06	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
HSTL_III_DCI_18	0.81	0.91	1.06	1.06	1.43	1.54	1.69	1.67	1.43	1.54	1.69	1.67	ns
DIFF_HSTL_I_18	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
DIFF_HSTL_I_DCI_18	0.85	0.94	1.09	1.08	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
DIFF_HSTL_I	0.85	0.94	1.09	1.08	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns
DIFF_HSTL_I_DCI	0.85	0.94	1.09	1.08	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
DIFF_HSTL_II_18	0.85	0.94	1.09	1.08	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
DIFF_HSTL_II_DCI_18	0.85	0.94	1.09	1.08	1.36	1.46	1.62	1.59	1.36	1.46	1.62	1.59	ns
DIFF_HSTL_II _T_DCI_18	0.85	0.94	1.09	1.08	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
DIFF_HSTL_II	0.85	0.94	1.09	1.08	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
DIFF_HSTL_II_DCI	0.85	0.94	1.09	1.08	1.37	1.49	1.68	1.66	1.37	1.49	1.68	1.66	ns
SSTL2_I_DCI	0.81	0.91	1.06	1.06	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
SSTL2_II_DCI	0.81	0.91	1.06	1.06	1.39	1.50	1.67	1.69	1.39	1.50	1.67	1.69	ns
SSTL2_II_T_DCI	0.81	0.91	1.06	1.06	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
SSTL18_I	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
SSTL18_II	0.81	0.91	1.06	1.06	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
SSTL18_I_DCI	0.81	0.91	1.06	1.06	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
SSTL18_II_DCI	0.81	0.91	1.06	1.06	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
SSTL18_II_T_DCI	0.81	0.91	1.06	1.06	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL2_I	0.85	0.94	1.09	1.08	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
DIFF_SSTL2_I_DCI	0.85	0.94	1.09	1.08	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
DIFF_SSTL2_II	0.85	0.94	1.09	1.08	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
DIFF_SSTL2_II_DCI	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.69	1.39	1.50	1.67	1.69	ns
DIFF_SSTL2_II_T_DCI	0.85	0.94	1.09	1.08	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns

Table 45: **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
DIFF_SSTL18_II	0.94	1.09	1.08	1.50	2.27	1.66	1.50	2.27	1.66	ns
DIFF_SSTL18_II_DCI	0.94	1.09	1.08	1.47	2.20	1.62	1.47	2.20	1.62	ns
DIFF_SSTL18_II_T_DCI	0.94	1.09	1.08	1.51	2.30	1.65	1.51	2.30	1.65	ns
DIFF_SSTL15	0.91	1.06	1.06	1.54	2.25	1.69	1.54	2.25	1.69	ns
DIFF_SSTL15_DCI	0.91	1.06	1.06	1.52	2.25	1.66	1.52	2.25	1.66	ns
DIFF_SSTL15_T_DCI	0.91	1.06	1.06	1.52	2.25	1.66	1.52	2.25	1.66	ns

Table 46: **IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{IOTPHZ}	T input to Pad high-impedance	0.86	0.92	0.99	0.99	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 47 shows the test setup parameters used for measuring input delay.

Table 47: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(5)	V_{REF} (1)(3)(5)
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III	HSTL_III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	V_{REF} – 1.00	V_{REF} + 1.00	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
HT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 6.
6. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 6 and Figure 7.

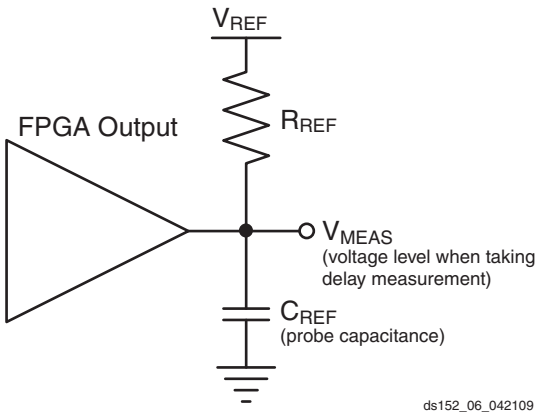

Figure 6: **Single Ended Test Setup**

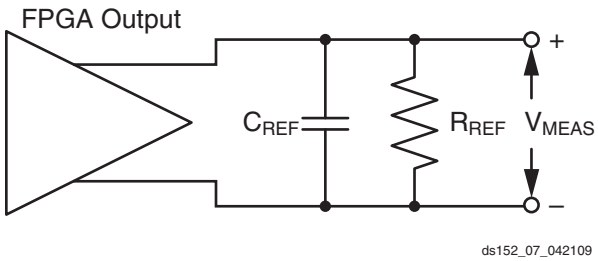

Figure 7: **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 48.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 48: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	100	0	0[2]	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDS_25	100	0	0[2]	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[2]	0

Table 48: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
HT (HyperTransport), 2.5V	LDT_25	100	0	0[2]	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	100	0	0[2]	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III, with DCI	HSTL_III_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 49: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Setup/Hold						
T_{ICE1CK}/T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.21/ 0.03	0.25/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	0.66/ –0.08	0.78/ –0.08	0.96/ –0.08	1.09/ –0.11	ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.07/ 0.41	0.08/ 0.46	0.10/ 0.54	0.11/ 0.64	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.10/ 0.32	0.12/ 0.36	0.14/ 0.42	0.16/ 0.50	ns
Combinatorial						
T_{IDI}	D pin to O pin propagation delay, no Delay	0.15	0.17	0.20	0.23	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.19	0.22	0.25	0.28	ns
Sequential Delays						
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.48	0.54	0.64	0.73	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.52	0.58	0.68	0.78	ns
T_{ICKQ}	CLK to Q outputs	0.54	0.61	0.70	0.93	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	0.85	0.97	1.15	1.32	ns
T_{GSRQ_ILOGIC}	Global Set/Reset to Q outputs	7.60	7.60	10.51	10.51	ns
Set/Reset						
T_{RPW_ILOGIC}	Minimum Pulse Width, SR inputs	0.78	0.95	1.20	1.30	ns, Min

Table 54: **CLB Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{ITO}	An – Dn inputs to A – D Q outputs	0.59	0.67	0.79	0.85	ns, Max
T_{AXA}	AX inputs to AMUX output	0.31	0.35	0.42	0.44	ns, Max
T_{AXB}	AX inputs to BMUX output	0.35	0.39	0.47	0.50	ns, Max
T_{AXC}	AX inputs to CMUX output	0.39	0.44	0.52	0.56	ns, Max
T_{AXD}	AX inputs to DMUX output	0.42	0.47	0.55	0.60	ns, Max
T_{BXB}	BX inputs to BMUX output	0.30	0.34	0.39	0.44	ns, Max
T_{BXD}	BX inputs to DMUX output	0.38	0.43	0.50	0.55	ns, Max
T_{CXC}	CX inputs to CMUX output	0.26	0.29	0.34	0.37	ns, Max
T_{CXD}	CX inputs to DMUX output	0.30	0.34	0.40	0.44	ns, Max
T_{DXD}	DX inputs to DMUX output	0.30	0.33	0.38	0.43	ns, Max
T_{OPCYA}	An input to COUT output	0.32	0.36	0.41	0.47	ns, Max
T_{OPCYB}	Bn input to COUT output	0.32	0.36	0.41	0.47	ns, Max
T_{OPCYC}	Cn input to COUT output	0.27	0.30	0.34	0.40	ns, Max
T_{OPCYD}	Dn input to COUT output	0.25	0.28	0.32	0.37	ns, Max
T_{AXCY}	AX input to COUT output	0.25	0.28	0.33	0.36	ns, Max
T_{BXCY}	BX input to COUT output	0.22	0.24	0.28	0.31	ns, Max
T_{CXCY}	CX input to COUT output	0.15	0.17	0.20	0.22	ns, Max
T_{DXCY}	DX input to COUT output	0.14	0.16	0.19	0.21	ns, Max
T_{BYP}	CIN input to COUT output	0.06	0.07	0.08	0.09	ns, Max
T_{CINA}	CIN input to AMUX output	0.21	0.24	0.28	0.30	ns, Max
T_{CINB}	CIN input to BMUX output	0.23	0.25	0.29	0.31	ns, Max
T_{CINC}	CIN input to CMUX output	0.23	0.26	0.30	0.33	ns, Max
T_{CIND}	CIN input to DMUX output	0.25	0.29	0.33	0.36	ns, Max
Sequential Delays						
T_{CKO}	Clock to AQ – DQ outputs	0.29	0.33	0.39	0.44	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs	0.36	0.40	0.47	0.53	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T_{DICK}/T_{CKDI}	A – D input to CLK on A – D Flip Flops	0.30/0.17	0.36/0.18	0.43/0.20	0.44/0.25	ns, Min
$T_{CECK\_CLB}/T_{CKCE\_CLB}$	CE input to CLK on A – D Flip Flops	0.20/0.00	0.25/0.00	0.32/0.00	0.32/0.01	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D Flip Flops	0.39/–0.07	0.44/–0.07	0.52/–0.07	0.58/–0.08	ns, Min
T_{CINCK}/T_{CKCIN}	CIN input to CLK on A – D Flip Flops	0.16/0.12	0.19/0.14	0.24/0.16	0.23/0.22	ns, Min
Set/Reset						
T_{SRMIN}	SR input minimum pulse width	0.90	0.90	0.97	0.80	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.52	0.58	0.68	0.77	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.41	0.48	0.59	0.61	ns, Max
F_{TOG}	Toggle frequency (for export control)	1412.00	1286.40	1098.00	1098.00	MHz

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

Table 58: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.26/ 0.04	0.30/ 0.04	0.35/ 0.05	0.35/ 0.05	0.43/ 0.06	ns
Combinatorial Delays from Input Pins to Output Pins							
$T_{DSPDO\_\{A, B\}\_\{P, CARRYOUT\}\_MULT}$	{A, B} input to {P, CARRYOUT} output using multiplier	3.76	4.29	5.08	5.08	5.87	ns
$T_{DSPDO\_D\_\{P, CARRYOUT\}\_MULT}$	D input to {P, CARRYOUT} output using multiplier	3.57	4.07	4.82	4.82	5.57	ns
$T_{DSPDO\_\{A, B\}\_\{P, CARRYOUT\}}$	{A, B} input to {P, CARRYOUT} output not using multiplier	1.55	1.76	2.07	2.07	2.41	ns
$T_{DSPDO\_\{C, CARRYIN\}\_\{P, CARRYOUT\}}$	{C, CARRYIN} input to {P, CARRYOUT} output	1.38	1.56	1.83	1.83	2.13	ns
Combinatorial Delays from Input Pins to Cascading Output Pins							
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.49	0.56	0.65	0.65	0.73	ns
$T_{DSPDO\_\{A, B\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.87	4.42	5.24	5.24	6.09	ns
$T_{DSPDO\_D\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$	D input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.66	4.17	4.94	4.94	5.76	ns
$T_{DSPDO\_\{A, B\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.64	1.86	2.19	2.19	2.60	ns
$T_{DSPDO\_\_\{C, CARRYIN\}\_\{PCOUT, CARRYCASCOUT,MULTSIGNOUT\}}$	{C, CARRYIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.46	1.66	1.95	1.95	2.32	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins							
$T_{DSPDO\_\{ACIN, BCIN\}\_\{P, CARRYOUT\}\_MULT}$	{ACIN, BCIN} input to {P, CARRYOUT} output using multiplier	3.67	4.19	4.97	4.97	5.75	ns
$T_{DSPDO\_\{ACIN, BCIN\}\_\{P, CARRYOUT}$	{ACIN, BCIN} input to {P, CARRYOUT} output not using multiplier	1.43	1.63	1.92	1.92	2.25	ns
$T_{DSPDO\_\{ACIN; BCIN\}\_\{ACOUT; BCOUT\}}$	{ACIN, BCIN} input to {ACOUT, BCOUT} output	0.36	0.42	0.49	0.49	0.56	ns
$T_{DSPDO\_\{ACIN, BCIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.76	4.29	5.10	5.10	5.94	ns
$T_{DSPDO\_\{ACIN, BCIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.52	1.73	2.05	2.05	2.44	ns
$T_{DSPDO\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_\{P, CARRYOUT\}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {P, CARRYOUT} output	1.19	1.35	1.60	1.60	1.87	ns

Table 62: **Regional Clock Switching Characteristics (BUFR) *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BRDO_O}	Propagation delay from CLR to O	0.69	0.74	0.80	1.12	ns
Maximum Frequency						
F_{MAX}[1]	Regional clock tree (BUFR)	500	420	300	300	MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

Table 63: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	0.15	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin Setup and Hold	0.04/ 0.04	0.04/ 0.04	0.05/ 0.05	0.04/ 0.04	ns
Maximum Frequency						
F_{MAX}	Horizontal clock buffer (BUFH)	800	750	700	667	MHz

MMCM Switching Characteristics

Table 64: **MMCM Specification**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F_{INMAX}	Maximum Input Clock Frequency[1]	800	750	700	700	MHz
F_{INMIN}	Minimum Input Clock Frequency	10	10	10	10	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
F_{INDUTY}[2]	Allowable Input Duty Cycle: 10—49 MHz	25/75				%
	Allowable Input Duty Cycle: 50—199 MHz	30/70				%
	Allowable Input Duty Cycle: 200—399 MHz	35/65				%
	Allowable Input Duty Cycle: 400—499 MHz	40/60				%
	Allowable Input Duty Cycle: >500 MHz	45/55				%
F_{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	0.01	0.01	MHz
F_{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	550	500	450	450	MHz
F_{VCOMIN}	Minimum MMCM VCO Frequency	600	600	600	600	MHz
F_{VCOMAX}	Maximum MMCM VCO Frequency	1600	1440	1200	1200	MHz
$F_{BANDWIDTH}$	Low MMCM Bandwidth at Typical[3]	1.00	1.00	1.00	1.00	MHz
	High MMCM Bandwidth at Typical[3]	4.00	4.00	4.00	4.00	MHz
$T_{STATPHAOFFSET}$	Static Phase Offset of the MMCM Outputs[4]	0.12	0.12	0.12	0.12	ns
$T_{OUTJITTER}$	MMCM Output Jitter[5]	Note 3				
$T_{OUTDUTY}$	MMCM Output Clock Duty Cycle Precision[6]	0.15	0.20	0.20	0.20	ns
$T_{LOCKMAX}$	MMCM Maximum Lock Time	100	100	100	100	µs
F_{OUTMAX}	MMCM Maximum Output Frequency	800	750	700	700	MHz
F_{OUTMIN}	MMCM Minimum Output Frequency[7][8]	4.69	4.69	4.69	4.69	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				

Table 66: **Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM.							
$T_{ICKOFMMCMGC}$	Global Clock Input and OUTFF *with* MMCM	XC6VLX75T	2.34	2.50	2.77	2.85	ns
		XC6VLX130T	2.35	2.51	2.78	2.87	ns
		XC6VLX195T	2.36	2.52	2.79	2.88	ns
		XC6VLX240T	2.36	2.52	2.79	2.88	ns
		XC6VLX365T	2.37	2.53	2.79	2.89	ns
		XC6VLX550T	N/A	2.55	2.82	2.93	ns
		XC6VLX760	N/A	2.54	2.82	2.92	ns
		XC6VSX315T	2.35	2.51	2.79	2.87	ns
		XC6VSX475T	N/A	2.43	2.70	2.79	ns
		XC6VHX250T	2.36	2.53	2.80	N/A	ns
		XC6VHX255T	2.46	2.63	2.91	N/A	ns
		XC6VHX380T	2.39	2.59	2.83	N/A	ns
		XC6VHX565T	N/A	2.54	2.81	N/A	ns
		XQ6VLX130T	N/A	2.51	2.78	2.87	ns
		XQ6VLX240T	N/A	2.52	2.79	2.88	ns
		XQ6VLX550T	N/A	N/A	2.82	2.93	ns
		XQ6VSX315T	N/A	2.51	2.79	2.87	ns
		XQ6VSX475T	N/A	N/A	2.70	2.79	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 72: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC6VLX75T	FF484	95	ps
			FF784	146	ps
		XC6VLX130T	FF484	95	ps
			FF784	146	ps
			FF1156	165	ps
		XC6VLX195T	FF784	145	ps
			FF1156	182	ps
		XC6VLX240T	FF784	146	ps
			FF1156	182	ps
			FF1759	187	ps
		XC6VLX365T	FF1156	189	ps
			FF1759	184	ps
		XC6VLX550T	FF1759	196	ps
			FF1760	249	ps
		XC6VLX760	FF1760	236	ps
		XC6VSX315T	FF1156	168	ps
			FF1759	190	ps
		XC6VSX475T	FF1156	168	ps
			FF1759	204	ps
		XC6VHX250T	FF1154	166	ps
		XC6VHX255T	FF1155	168	ps
			FF1923	228	ps
		XC6VHX380T	FF1154	159	ps
			FF1155	172	ps
			FF1923	227	ps
			FF1924	220	ps
		XC6VHX565T	FF1923	232	ps
			FF1924	197	ps
		XQ6VLX130T	RF784	146	ps
			RF1156	165	ps
			FFG1156	165	ps
		XQ6VLX240T	RF784	146	ps
			RF1156	182	ps
			FFG1156	182	ps
			RF1759	187	ps
		XQ6VLX550T	RF1759	196	ps
		XQ6VSX315T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	190	ps
		XQ6VSX475T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	204	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.