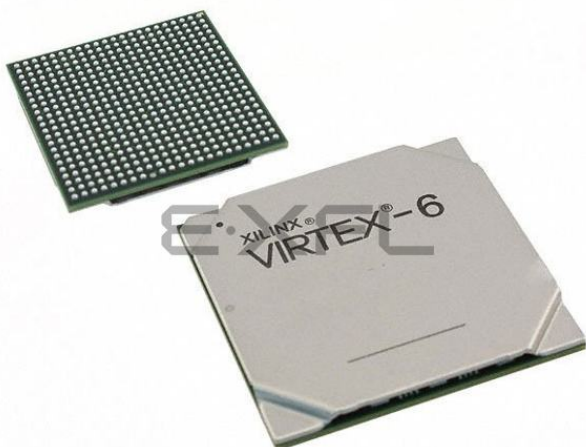




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	18840
Number of Logic Elements/Cells	241152
Total RAM Bits	15335424
Number of I/O	720
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1759-BBGA, FCBGA
Supplier Device Package	1759-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vlx240t-3ffg1759c

Table 23: GTX Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTXTX}	Serial data rate range		0.480	–	F _{GTXMAX}	Gb/s
T _{RTX}	TX Rise time	20%–80%	–	120	–	ps
T _{FTX}	TX Fall time	80%–20%	–	120	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	350	ps
V _{TXOOBVDPP}	Electrical idle amplitude		–	–	15	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		–	–	75	ns
TJ _{6.5}	Total Jitter ⁽²⁾⁽³⁾	6.5 Gb/s	–	–	0.33	UI
DJ _{6.5}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.17	UI
TJ _{5.0}	Total Jitter ⁽²⁾⁽³⁾	5.0 Gb/s	–	–	0.33	UI
DJ _{5.0}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.15	UI
TJ _{4.25}	Total Jitter ⁽²⁾⁽³⁾	4.25 Gb/s	–	–	0.33	UI
DJ _{4.25}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.14	UI
TJ _{3.75}	Total Jitter ⁽²⁾⁽³⁾	3.75 Gb/s	–	–	0.34	UI
DJ _{3.75}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.16	UI
TJ _{3.125}	Total Jitter ⁽²⁾⁽³⁾	3.125 Gb/s	–	–	0.2	UI
DJ _{3.125}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.1	UI
TJ _{3.125L}	Total Jitter ⁽²⁾⁽³⁾	3.125 Gb/s ⁽⁴⁾	–	–	0.35	UI
DJ _{3.125L}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.16	UI
TJ _{2.5}	Total Jitter ⁽²⁾⁽³⁾	2.5 Gb/s ⁽⁵⁾	–	–	0.20	UI
DJ _{2.5}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.08	UI
TJ _{1.25}	Total Jitter ⁽²⁾⁽³⁾	1.25 Gb/s ⁽⁶⁾	–	–	0.15	UI
DJ _{1.25}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.06	UI
TJ ₆₀₀	Total Jitter ⁽²⁾⁽³⁾	600 Mb/s	–	–	0.1	UI
DJ ₆₀₀	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.03	UI
TJ ₄₈₀	Total Jitter ⁽²⁾⁽³⁾	480 Mb/s	–	–	0.1	UI
DJ ₄₈₀	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
- Using PLL_DIVSEL_FB = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 1e⁻¹².
- PLL frequency at 1.5625 GHz and OUTDIV = 1.
- PLL frequency at 2.5 GHz and OUTDIV = 2.
- PLL frequency at 2.5 GHz and OUTDIV = 4.

Table 24: GTX Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
F _{GTXRX}	Serial data rate	RX oversampler not enabled	0.600	–	F _{GTXMAX}	Gb/s
		RX oversampler enabled	0.480	–	0.600	Gb/s
T _{RXELECIDLE}	Time for RXELECIDLE to respond to loss or restoration of data		–	75	–	ns
RX _{OOBVDPP}	OOB detect threshold peak-to-peak		60	–	150	mV
RX _{SST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated @ 33 KHz	–5000	–	0	ppm
RX _{RL}	Run length (CID)	Internal AC capacitor bypassed	–	–	512	UI
RX _{PPMTOL}	Data/REFCLK PPM offset tolerance	CDR 2 nd -order loop disabled	–200	–	200	ppm
		CDR 2 nd -order loop enabled	–2000	–	2000	ppm
SJ Jitter Tolerance ⁽²⁾						
JT_SJ _{6.5}	Sinusoidal Jitter ⁽³⁾	6.5 Gb/s	0.44	–	–	UI
JT_SJ _{5.0}	Sinusoidal Jitter ⁽³⁾	5.0 Gb/s	0.44	–	–	UI
JT_SJ _{4.25}	Sinusoidal Jitter ⁽³⁾	4.25 Gb/s	0.44	–	–	UI
JT_SJ _{3.75}	Sinusoidal Jitter ⁽³⁾	3.75 Gb/s	0.44	–	–	UI
JT_SJ _{3.125}	Sinusoidal Jitter ⁽³⁾	3.125 Gb/s	0.45	–	–	UI
JT_SJ _{3.125L}	Sinusoidal Jitter ⁽³⁾	3.125 Gb/s ⁽⁴⁾	0.45	–	–	UI
JT_SJ _{2.5}	Sinusoidal Jitter ⁽³⁾	2.5 Gb/s ⁽⁵⁾	0.5	–	–	UI
JT_SJ _{1.25}	Sinusoidal Jitter ⁽³⁾	1.25 Gb/s ⁽⁶⁾	0.5	–	–	UI
JT_SJ ₆₀₀	Sinusoidal Jitter ⁽³⁾	600 Mb/s	0.4	–	–	UI
JT_SJ ₄₈₀	Sinusoidal Jitter ⁽³⁾	480 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye ⁽²⁾						
JT_TJSE _{3.125}	Total Jitter with Stressed Eye ⁽⁷⁾	3.125 Gb/s	0.70	–	–	UI
		5.0 Gb/s	0.70	–	–	UI
JT_SJSE _{3.125}	Sinusoidal Jitter with Stressed Eye ⁽⁷⁾	3.125 Gb/s	0.1	–	–	UI
		5.0 Gb/s	0.1	–	–	UI

Notes:

- Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 1e^{–12}.
- The frequency of the injected sinusoidal jitter is 80 MHz.
- PLL frequency at 1.5625 GHz and OUTDIV = 1.
- PLL frequency at 2.5 GHz and OUTDIV = 2.
- PLL frequency at 2.5 GHz and OUTDIV = 4.
- Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Switching Characteristics

Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further information.

Table 32: GTH Transceiver Maximum Data Rate and PLL Frequency Range

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F_{GTHMAX}	Maximum GTH transceiver data rate	PLL Output Divider = 1	11.182	11.182	10.32	Gb/s
		PLL Output Divider = 4	2.795	2.795	2.58	Gb/s
F_{GTHMIN}	Minimum GTH transceiver data rate ⁽¹⁾	PLL Output Divider = 1	9.92	9.92	9.92	Gb/s
		PLL Output Divider = 4	2.48	2.48	2.48	Gb/s
$F_{GPLLMAX}$	Maximum GTH PLL frequency		5.591	5.591	5.16	GHz
$F_{GPLLMIN}$	Minimum GTH PLL frequency		4.96	4.96	4.96	GHz

Notes:

1. Lower data rates can be achieved using FPGA logic based oversampling designs.

Table 33: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{GTHDRPCLK}$	GTHDRPCLK maximum frequency	70	70	60	MHz

Table 34: GTH Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range	-1 speed grade	150	—	645	MHz
		-2 and -3 speed grades	150	—	700	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	—	200	—	ps
T_{FCLK}	Reference clock fall time	80% – 20%	—	200	—	ps
T_{DCREF}	Reference clock duty cycle	CLK	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	—	—	2	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	—	—	20	μs

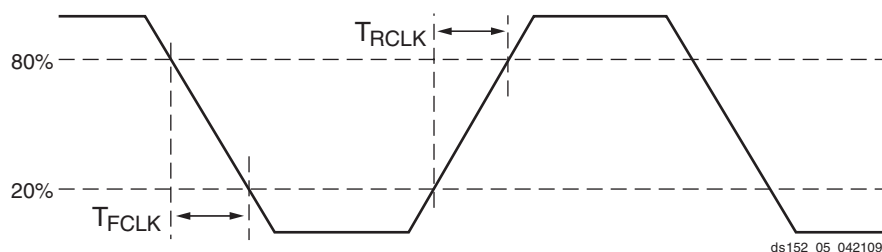


Figure 5: Reference Clock Timing Parameters

Table 37: GTH Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
R _{XRL}	Run length (CID)		8000	–	–	UI
R _{XPPMTOL}	Data/REFCLK PPM offset tolerance		–200	–	200	ppm
SJ Jitter Tolerance ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾						
JT_SJ _{11.18}	Sinusoidal Jitter	11.18 Gb/s	0.3	–	–	UI
JT_SJ _{10.32}	Sinusoidal Jitter	10.32 Gb/s	0.3	–	–	UI
JT_SJ _{9.95}	Sinusoidal Jitter	9.95 Gb/s	0.3	–	–	UI
JT_SJ _{2.667}	Sinusoidal Jitter	2.667 Gb/s	0.5	–	–	UI
JT_SJ _{2.48}	Sinusoidal Jitter	2.48 Gb/s	0.5	–	–	UI

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. High-frequency jitter tolerance including 6 db of channel loss at a high frequency of the data rate divided by two.

Ethernet MAC Switching Characteristics

Consult [UG368: Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide](#) for further information.

Table 38: Maximum Ethernet MAC Performance

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1	-1L	
F _{TEMACCLIENT}	Client interface maximum frequency	10 Mb/s – 8-bit width	2.5 ⁽¹⁾	2.5 ⁽¹⁾	2.5 ⁽¹⁾	2.5 ⁽¹⁾	MHz
		100 Mb/s – 8-bit width	25 ⁽²⁾	25 ⁽²⁾	25 ⁽²⁾	25 ⁽²⁾	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		1000 Mb/s – 16-bit width	62.5	62.5	62.5	62.5	MHz
		2000 Mb/s – 16-bit width	125	125	125	N/A	MHz
		2500 Mb/s – 16-bit width	156.25	156.25	156.25	N/A	MHz
F _{TEMACPHY}	Physical interface maximum frequency	10 Mb/s – 4-bit width	2.5	2.5	2.5	2.5	MHz
		100 Mb/s – 4-bit width	25	25	25	25	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		2000 Mb/s – 8-bit width	250	250	250	N/A	MHz
		2500 Mb/s – 8-bit width	312.5	312.5	312.5	N/A	MHz

Notes:

1. When not using clock enable, the F_{MAX} is lowered to 1.25 MHz.
2. When not using clock enable, the F_{MAX} is lowered to 12.5 MHz.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 39: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F _{PIPECLK}	Pipe clock maximum frequency	250	250	250	250	MHz
F _{USERCLK}	User clock maximum frequency	500	500	250	250	MHz
F _{DRPCLK}	DRP clock maximum frequency	250	250	250	250	MHz

System Monitor Analog-to-Digital Converter Specification

Table 40: Analog-to-Digital Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
AV _{DD} = 2.5V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 5.2 MHz, T _j = -55°C to 125°C M-Grade, Typical values at T _j = +35°C						
DC Accuracy: All external input channels. Both unipolar and bipolar modes.						
Resolution			10	—	—	Bits
Integral Nonlinearity	INL		—	—	±1	LSBs
Differential Nonlinearity	DNL	No missing codes (T _{MIN} to T _{MAX}) Guaranteed Monotonic	—	—	±0.9	LSBs
Unipolar Offset Error ⁽¹⁾		Uncalibrated	—	±2	±30	LSBs
Bipolar Offset Error ⁽¹⁾		Uncalibrated measured in bipolar mode	—	±2	±30	LSBs
Gain Error		Uncalibrated - External Reference	—	±0.2	±2	%
		Uncalibrated - Internal Reference	—	±2	—	%
Bipolar Gain Error ⁽¹⁾		Uncalibrated - External Reference	—	±0.2	±2	%
		Uncalibrated - Internal Reference	—	±2	—	%
Total Unadjusted Error (Uncalibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	—	±10	—	LSBs
		Deviation from ideal transfer function. Internal reference	—	±20	—	LSBs
Total Unadjusted Error (Calibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	—	±1	±2	LSBs
Calibrated Gain Temperature Coefficient		Variation of FS code with temperature	—	±0.01	—	LSB/°C
DC Common-Mode Reject	CMRR _{DC}	V _N = V _{CM} = 0.5V ± 0.5V, V _P - V _N = 100mV	—	70	—	dB
Conversion Rate ⁽²⁾						
Conversion Time - Continuous	t _{CONV}	Number of CLK cycles	26	—	32	
Conversion Time - Event	t _{CONV}	Number of CLK cycles	—	—	21	
T/H Acquisition Time	t _{ACQ}	Number of CLK cycles	4	—	—	
DRP Clock Frequency	DCLK	DRP clock frequency	8	—	80	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	—	5.2	MHz
CLK Duty cycle			40	—	60	%

Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.17 for -3, -2, and -1; and v1.10 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 42 correlates the current status of each Virtex-6 device on a per speed grade basis.

Table 42: Virtex-6 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6VLX75T			-3, -2, -1, -1L
XC6VLX130T			-3, -2, -1, -1L
XC6VLX195T			-3, -2, -1, -1L
XC6VLX240T			-3, -2, -1, -1L
XC6VLX365T			-3, -2, -1, -1L
XC6VLX550T			-2, -1, -1L
XC6VLX760			-2, -1, -1L
XC6VSX315T			-3, -2, -1, -1L
XC6VSX475T			-2, -1, -1L
XC6VHX250T			-3, -2, -1
XC6VHX255T			-3, -2, -1
XC6VHX380T			-3, -2, -1
XC6VHX565T			-2, -1
XQ6VLX130T			-2, -1, -1L
XQ6VLX240T			-2, -1, -1L
XQ6VLX550T			-1, -1L
XQ6VSX315T			-2, -1, -1L
XQ6VSX475T			-1, -1L

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 devices.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label ([Advance](#), [Preliminary](#), [Production](#)). Any labeling discrepancies are corrected in subsequent speed specification releases.

[Table 43](#) lists the production released Virtex-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE® software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 43: Virtex-6 Device Production Software and Speed Specification Release

Device	Speed Grade Designations			
	-3	-2	-1	-1L
XC6VLX75T	ISE 12.2 v1.08			ISE 12.3 v1.07 Patch
XC6VLX130T	ISE 12.1 v1.06	ISE 11.5 v1.05 ⁽²⁾	ISE 11.5 v1.05 ⁽²⁾	ISE 12.2 v1.05
XC6VLX195T	ISE 12.1 v1.06	ISE 12.1 v1.06	ISE 12.1 v1.06	ISE 12.2 v1.04
XC6VLX240T	ISE 12.1 v1.06	ISE 11.4.1 v1.04 ⁽²⁾	ISE 11.4.1 v1.04 ⁽²⁾	ISE 12.2 v1.04
XC6VLX365T	ISE 12.2 v1.08			ISE 12.2 v1.04
XC6VLX550T	N/A	ISE 12.2 v1.07		ISE 12.2 v1.04
XC6VLX760	N/A	ISE 12.2 v1.08		ISE 12.3 v1.07 Patch
XC6VSX315T	ISE 12.2 v1.08	ISE 12.1 v1.06		ISE 12.3 v1.07 Patch
XC6VSX475T	N/A	ISE 12.2 v1.08		ISE 12.3 v1.07 Patch
XC6VHX250T	ISE 12.4 v1.10			N/A
XC6VHX255T	ISE 13.1 v1.14 using the ISE 13.1 software update			N/A
XC6VHX380T	ISE 12.4 v1.10			N/A
XC6VHX565T	N/A	ISE 13.1 v1.14 using the ISE 13.1 software update		N/A
XQ6VLX130T	N/A	ISE 13.3 v1.17 Patch		ISE 13.3 v1.10
XQ6VLX240T	N/A	ISE 13.3 v1.17 Patch		ISE 13.3 v1.10
XQ6VLX550T	N/A	N/A	ISE 13.3 v1.17 Patch	ISE 13.3 v1.10
XQ6VSX315T	N/A	ISE 13.3 v1.17 Patch		ISE 13.3 v1.10
XQ6VSX475T	N/A	N/A	ISE 13.3 v1.17 Patch	ISE 13.3 v1.10

Notes:

- Blank entries indicate a device and/or speed grade in advance or preliminary status.
- Designs utilizing the GTX transceivers must use the software version ISE 12.1 v1.06 or later.

IOB Pad Input/Output/3-State Switching Characteristics

Table 44 (for commercial (XC) Virtex-6 devices) and **Table 45** (for the Defense-grade (XQ) Virtex-6 devices) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 46 summarizes the value of T_{IOTPHZ} . T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDS_25	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
LVDSEXT_25	0.85	0.94	1.09	1.08	1.53	1.65	1.84	1.73	1.53	1.65	1.84	1.73	ns
HT_25	0.85	0.94	1.09	1.08	1.51	1.62	1.78	1.69	1.51	1.62	1.78	1.69	ns
BLVDS_25	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.65	1.39	1.50	1.67	1.65	ns
RSDS_25 (point to point)	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
HSTL_I	0.81	0.91	1.06	1.06	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns
HSTL_II	0.81	0.91	1.06	1.06	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
HSTL_III	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
HSTL_I_18	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
HSTL_II_18	0.81	0.91	1.06	1.06	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
HSTL_III_18	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
SSTL2_I	0.81	0.91	1.06	1.06	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
SSTL2_II	0.81	0.91	1.06	1.06	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
LVC MOS25, Slow, 2 mA	0.51	0.57	0.66	0.70	5.09	5.46	6.01	5.63	5.09	5.46	6.01	5.63	ns
LVC MOS25, Slow, 4 mA	0.51	0.57	0.66	0.70	3.30	3.49	3.79	3.65	3.30	3.49	3.79	3.65	ns
LVC MOS25, Slow, 6 mA	0.51	0.57	0.66	0.70	2.62	2.81	3.08	2.95	2.62	2.81	3.08	2.95	ns
LVC MOS25, Slow, 8 mA	0.51	0.57	0.66	0.70	2.21	2.41	2.72	2.59	2.21	2.41	2.72	2.59	ns
LVC MOS25, Slow, 12 mA	0.51	0.57	0.66	0.70	1.80	1.95	2.17	2.10	1.80	1.95	2.17	2.10	ns
LVC MOS25, Slow, 16 mA	0.51	0.57	0.66	0.70	1.89	2.05	2.29	2.21	1.89	2.05	2.29	2.21	ns
LVC MOS25, Slow, 24 mA	0.51	0.57	0.66	0.70	1.68	1.82	2.02	1.98	1.68	1.82	2.02	1.98	ns
LVC MOS25, Fast, 2 mA	0.51	0.57	0.66	0.70	5.12	5.49	6.04	5.62	5.12	5.49	6.04	5.62	ns
LVC MOS25, Fast, 4 mA	0.51	0.57	0.66	0.70	3.28	3.50	3.82	3.65	3.28	3.50	3.82	3.65	ns
LVC MOS25, Fast, 6 mA	0.51	0.57	0.66	0.70	2.56	2.73	2.99	2.88	2.56	2.73	2.99	2.88	ns
LVC MOS25, Fast, 8 mA	0.51	0.57	0.66	0.70	2.11	2.33	2.65	2.53	2.11	2.33	2.65	2.53	ns
LVC MOS25, Fast, 12 mA	0.51	0.57	0.66	0.70	1.74	1.88	2.08	2.03	1.74	1.88	2.08	2.03	ns
LVC MOS25, Fast, 16 mA	0.51	0.57	0.66	0.70	1.77	1.92	2.13	2.08	1.77	1.92	2.13	2.08	ns

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDCI_DV2_25	0.51	0.57	0.66	0.70	1.71	1.83	2.01	2.00	1.71	1.83	2.01	2.00	ns
LVDCI_DV2_18	0.55	0.61	0.71	0.73	1.69	1.81	2.00	1.98	1.69	1.81	2.00	1.98	ns
LVDCI_DV2_15	0.64	0.73	0.85	0.85	1.68	1.77	1.91	1.98	1.68	1.77	1.91	1.98	ns
LVPECL_25	0.85	0.94	1.09	1.08	1.38	1.49	1.65	1.64	1.38	1.49	1.65	1.64	ns
HSTL_I_12	0.81	0.91	1.06	1.06	1.48	1.60	1.78	1.74	1.48	1.60	1.78	1.74	ns
HSTL_I_DCI	0.81	0.91	1.06	1.06	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
HSTL_II_DCI	0.81	0.91	1.06	1.06	1.37	1.49	1.68	1.66	1.37	1.49	1.68	1.66	ns
HSTL_II_T_DCI	0.81	0.91	1.06	1.06	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
HSTL_III_DCI	0.81	0.91	1.06	1.06	1.34	1.45	1.62	1.61	1.34	1.45	1.62	1.61	ns
HSTL_I_DCI_18	0.81	0.91	1.06	1.06	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
HSTL_II_DCI_18	0.81	0.91	1.06	1.06	1.36	1.46	1.62	1.59	1.36	1.46	1.62	1.59	ns
HSTL_II_T_DCI_18	0.81	0.91	1.06	1.06	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
HSTL_III_DCI_18	0.81	0.91	1.06	1.06	1.43	1.54	1.69	1.67	1.43	1.54	1.69	1.67	ns
DIFF_HSTL_I_18	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
DIFF_HSTL_I_DCI_18	0.85	0.94	1.09	1.08	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
DIFF_HSTL_I	0.85	0.94	1.09	1.08	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns
DIFF_HSTL_I_DCI	0.85	0.94	1.09	1.08	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
DIFF_HSTL_II_18	0.85	0.94	1.09	1.08	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
DIFF_HSTL_II_DCI_18	0.85	0.94	1.09	1.08	1.36	1.46	1.62	1.59	1.36	1.46	1.62	1.59	ns
DIFF_HSTL_II_T_DCI_18	0.85	0.94	1.09	1.08	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
DIFF_HSTL_II	0.85	0.94	1.09	1.08	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
DIFF_HSTL_II_DCI	0.85	0.94	1.09	1.08	1.37	1.49	1.68	1.66	1.37	1.49	1.68	1.66	ns
SSTL2_I_DCI	0.81	0.91	1.06	1.06	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
SSTL2_II_DCI	0.81	0.91	1.06	1.06	1.39	1.50	1.67	1.69	1.39	1.50	1.67	1.69	ns
SSTL2_II_T_DCI	0.81	0.91	1.06	1.06	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
SSTL18_I	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
SSTL18_II	0.81	0.91	1.06	1.06	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
SSTL18_I_DCI	0.81	0.91	1.06	1.06	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
SSTL18_II_DCI	0.81	0.91	1.06	1.06	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
SSTL18_II_T_DCI	0.81	0.91	1.06	1.06	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL2_I	0.85	0.94	1.09	1.08	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
DIFF_SSTL2_I_DCI	0.85	0.94	1.09	1.08	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
DIFF_SSTL2_II	0.85	0.94	1.09	1.08	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
DIFF_SSTL2_II_DCI	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.69	1.39	1.50	1.67	1.69	ns
DIFF_SSTL2_II_T_DCI	0.85	0.94	1.09	1.08	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
DIFF_SSTL18_I	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
DIFF_SSTL18_I_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL18_II	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
DIFF_SSTL18_II_DCI	0.85	0.94	1.09	1.08	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
DIFF_SSTL18_II_T_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
DIFF_SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVDS_25	0.94	1.09	1.08	1.54	2.16	1.62	1.54	2.16	1.62	ns
LVDSEXT_25	0.94	1.09	1.08	1.65	2.20	1.73	1.65	2.20	1.73	ns
HT_25	0.94	1.09	1.08	1.62	2.20	1.69	1.62	2.20	1.69	ns
BLVDS_25	0.94	1.09	1.08	1.50	3.18	1.65	1.50	3.18	1.65	ns
RSDS_25 (point to point)	0.94	1.09	1.08	1.54	2.22	1.62	1.54	2.22	1.62	ns
HSTL_I	0.91	1.06	1.06	1.56	2.44	1.71	1.56	2.44	1.71	ns
HSTL_II	0.91	1.06	1.06	1.56	2.21	1.72	1.56	2.21	1.72	ns
HSTL_III	0.91	1.06	1.06	1.54	2.50	1.69	1.54	2.50	1.69	ns
HSTL_I_18	0.91	1.06	1.06	1.58	2.43	1.72	1.58	2.43	1.72	ns
HSTL_II_18	0.91	1.06	1.06	1.62	2.30	1.78	1.62	2.30	1.78	ns
HSTL_III_18	0.91	1.06	1.06	1.54	2.49	1.69	1.54	2.49	1.69	ns
SSTL2_I	0.91	1.06	1.06	1.60	2.50	1.74	1.60	2.50	1.74	ns
SSTL2_II	0.91	1.06	1.06	1.54	2.49	1.71	1.54	2.49	1.71	ns
SSTL15	0.91	1.06	1.06	1.54	2.07	1.69	1.54	2.07	1.69	ns
LVC MOS25, Slow, 2 mA	0.57	0.66	0.70	5.46	6.01	5.63	5.46	6.01	5.63	ns
LVC MOS25, Slow, 4 mA	0.57	0.66	0.70	3.49	3.79	3.65	3.49	3.79	3.65	ns
LVC MOS25, Slow, 6 mA	0.57	0.66	0.70	2.81	3.08	2.95	2.81	3.08	2.95	ns
LVC MOS25, Slow, 8 mA	0.57	0.66	0.70	2.41	2.72	2.59	2.41	2.72	2.59	ns
LVC MOS25, Slow, 12 mA	0.57	0.66	0.70	1.95	2.23	2.10	1.95	2.23	2.10	ns
LVC MOS25, Slow, 16 mA	0.57	0.66	0.70	2.05	2.29	2.21	2.05	2.29	2.21	ns
LVC MOS25, Slow, 24 mA	0.57	0.66	0.70	1.82	2.24	1.98	1.82	2.24	1.98	ns
LVC MOS25, Fast, 2 mA	0.57	0.66	0.70	5.49	6.04	5.62	5.49	6.04	5.62	ns
LVC MOS25, Fast, 4 mA	0.57	0.66	0.70	3.50	3.82	3.65	3.50	3.82	3.65	ns
LVC MOS25, Fast, 6 mA	0.57	0.66	0.70	2.73	2.99	2.88	2.73	2.99	2.88	ns
LVC MOS25, Fast, 8 mA	0.57	0.66	0.70	2.33	2.65	2.53	2.33	2.65	2.53	ns
LVC MOS25, Fast, 12 mA	0.57	0.66	0.70	1.88	2.08	2.03	1.88	2.08	2.03	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVC MOS25, Fast, 16 mA	0.57	0.66	0.70	1.92	2.15	2.08	1.92	2.15	2.08	ns
LVC MOS25, Fast, 24 mA	0.57	0.66	0.70	1.79	2.15	1.96	1.79	2.15	1.96	ns
LVC MOS18, Slow, 2 mA	0.61	0.71	0.73	4.47	4.87	4.30	4.47	4.87	4.30	ns
LVC MOS18, Slow, 4 mA	0.61	0.71	0.73	2.96	3.21	2.94	2.96	3.21	2.94	ns
LVC MOS18, Slow, 6 mA	0.61	0.71	0.73	2.43	2.64	2.47	2.43	2.64	2.47	ns
LVC MOS18, Slow, 8 mA	0.61	0.71	0.73	2.11	2.41	2.24	2.11	2.41	2.24	ns
LVC MOS18, Slow, 12 mA	0.61	0.71	0.73	1.99	2.30	2.10	1.99	2.30	2.10	ns
LVC MOS18, Slow, 16 mA	0.61	0.71	0.73	1.95	2.30	2.04	1.95	2.30	2.04	ns
LVC MOS18, Fast, 2 mA	0.61	0.71	0.73	4.23	4.57	4.08	4.23	4.57	4.08	ns
LVC MOS18, Fast, 4 mA	0.61	0.71	0.73	2.76	2.97	2.74	2.76	2.97	2.74	ns
LVC MOS18, Fast, 6 mA	0.61	0.71	0.73	2.28	2.46	2.32	2.28	2.46	2.32	ns
LVC MOS18, Fast, 8 mA	0.61	0.71	0.73	1.99	2.34	2.14	1.99	2.34	2.14	ns
LVC MOS18, Fast, 12 mA	0.61	0.71	0.73	1.80	2.19	1.88	1.80	2.19	1.88	ns
LVC MOS18, Fast, 16 mA	0.61	0.71	0.73	1.74	2.18	1.88	1.74	2.18	1.88	ns
LVC MOS15, Slow, 2 mA	0.73	0.85	0.85	3.77	4.29	3.91	3.77	4.29	3.91	ns
LVC MOS15, Slow, 4 mA	0.73	0.85	0.85	2.79	3.10	2.93	2.79	3.10	2.93	ns
LVC MOS15, Slow, 6 mA	0.73	0.85	0.85	2.32	2.68	2.50	2.32	2.68	2.50	ns
LVC MOS15, Slow, 8 mA	0.73	0.85	0.85	1.98	2.29	2.24	1.98	2.29	2.24	ns
LVC MOS15, Slow, 12 mA	0.73	0.85	0.85	1.91	2.23	2.07	1.91	2.23	2.07	ns
LVC MOS15, Slow, 16 mA	0.73	0.85	0.85	1.83	2.23	1.98	1.83	2.23	1.98	ns
LVC MOS15, Fast, 2 mA	0.73	0.85	0.85	3.77	4.28	3.91	3.77	4.28	3.91	ns
LVC MOS15, Fast, 4 mA	0.73	0.85	0.85	2.53	2.78	2.66	2.53	2.78	2.66	ns
LVC MOS15, Fast, 6 mA	0.73	0.85	0.85	2.05	2.42	2.16	2.05	2.42	2.16	ns
LVC MOS15, Fast, 8 mA	0.73	0.85	0.85	1.90	2.20	2.04	1.90	2.20	2.04	ns
LVC MOS15, Fast, 12 mA	0.73	0.85	0.85	1.77	2.11	1.90	1.77	2.11	1.90	ns
LVC MOS15, Fast, 16 mA	0.73	0.85	0.85	1.76	2.11	1.92	1.76	2.11	1.92	ns
LVC MOS12, Slow, 2 mA	0.81	0.93	0.95	3.39	3.75	3.54	3.39	3.75	3.54	ns
LVC MOS12, Slow, 4 mA	0.81	0.93	0.95	2.63	2.93	2.79	2.63	2.93	2.79	ns
LVC MOS12, Slow, 6 mA	0.81	0.93	0.95	2.11	2.67	2.26	2.11	2.67	2.26	ns
LVC MOS12, Slow, 8 mA	0.81	0.93	0.95	2.02	2.25	2.17	2.02	2.25	2.17	ns
LVC MOS12, Fast, 2 mA	0.81	0.93	0.95	2.98	3.39	3.11	2.98	3.39	3.11	ns
LVC MOS12, Fast, 4 mA	0.81	0.93	0.95	2.16	2.70	2.31	2.16	2.70	2.31	ns
LVC MOS12, Fast, 6 mA	0.81	0.93	0.95	1.89	2.34	2.05	1.89	2.34	2.05	ns
LVC MOS12, Fast, 8 mA	0.81	0.93	0.95	1.82	2.10	1.98	1.82	2.10	1.98	ns
LVDCI_25	0.57	0.70	0.70	2.14	2.82	2.26	2.14	2.82	2.26	ns
LVDCI_18	0.61	0.71	0.73	2.23	2.78	2.38	2.23	2.78	2.38	ns
LVDCI_15	0.73	0.85	0.85	2.01	2.75	2.18	2.01	2.75	2.18	ns
LVDCI_DV2_25	0.57	0.70	0.70	1.83	2.37	2.00	1.83	2.37	2.00	ns

Table 50: OLOGIC Switching Characteristics

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup/Hold							
T _{ODCK} /T _{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.45/ −0.08	0.50/ −0.08	0.54/ −0.08	0.54/ −0.08	0.69/ −0.11	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.17/ −0.03	0.20/ −0.03	0.22/ −0.03	0.27/ −0.05	0.27/ −0.04	ns
T _{OSRCK} /T _{OCKSR}	SR pin Setup/Hold with respect to CLK	0.59/ −0.24	0.62/ −0.24	0.54/ −0.08	0.54/ −0.08	0.79/ −0.35	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.44/ −0.07	0.51/ −0.07	0.56/ −0.07	0.60/ −0.10	0.68/ −0.13	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.15/ −0.04	0.19/ −0.04	0.21/ −0.04	0.27/ −0.05	0.29/ −0.05	ns
Combinatorial							
T _{DOQ}	D1 to OQ out or T1 to TQ out	0.78	0.87	1.01	1.01	1.15	ns
Sequential Delays							
T _{OCKQ}	CLK to OQ/TQ out	0.54	0.61	0.71	0.71	0.80	ns
T _{RQ}	SR pin to OQ/TQ out	0.80	0.90	1.05	1.05	1.19	ns
T _{GSRQ}	Global Set/Reset to Q outputs	7.60	7.60	10.51	10.51	10.51	ns
Set/Reset							
T _{RPW}	Minimum Pulse Width, SR inputs	0.78	0.95	1.20	1.20	1.30	ns, Min

Input/Output Delay Switching Characteristics

Table 53: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
IDELAYCTRL						
T _{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3.00	3.00	3.00	3.25	μs
F _{IDELAYCTRL_REF}	REFCLK frequency = 200.0 ⁽¹⁾	200	200	200	200	MHz
	REFCLK frequency = 300.0 ⁽¹⁾	300	300	–	–	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
T _{IDELAYCTRL_RPW}	Minimum Reset pulse width	50.00	50.00	50.00	52.50	ns
IODELAY						
T _{IDELAYRESOLUTION}	IODELAY Chain Delay Resolution	1/(32 x 2 x F _{REF})				ps
T _{IDELAYPAT_JIT}	Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾	0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). ⁽³⁾	±5	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). ⁽⁴⁾	±9	±9	±9	±9	ps per tap
T _{IODELAY_CLK_MAX}	Maximum frequency of CLK input to IODELAY	500.00	420.00	300.00	300.00	MHz
T _{IODCCK_CE} / T _{IODCKC_CE}	CE pin Setup/Hold with respect to CK	0.45/ –0.09	0.53/ –0.09	0.65/ –0.09	0.84/ –0.14	ns
T _{IODCK_INC} / T _{IODCKC_INC}	INC pin Setup/Hold with respect to CK	0.23/ –0.02	0.27/ –0.01	0.31/ 0.00	0.27/ –0.04	ns
T _{IODCCK_RST} / T _{IODCKC_RST}	RST pin Setup/Hold with respect to CK	0.57/ –0.08	0.62/ –0.08	0.69/ –0.08	0.74/ –0.13	ns
T _{IODDO_T}	TSCONTROL delay to MUXE/MUXF switching and through IODELAY	Note 5	Note 5	Note 5	Note 5	ps
T _{IODDO_IDATAIN}	Propagation delay through IODELAY	Note 5	Note 5	Note 5	Note 5	ps
T _{IODDO_ODATAIN}	Propagation delay through IODELAY	Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See TRACE report for actual values.

CLB Switching Characteristics

Table 54: CLB Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Combinatorial Delays						
T _{ILO}	An – Dn LUT address to A	0.06	0.07	0.07	0.09	ns, Max
	An – Dn LUT address to AMUX/CMUX	0.18	0.20	0.22	0.25	ns, Max
	An – Dn LUT address to BMUX_A	0.28	0.31	0.36	0.40	ns, Max

Table 54: CLB Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T _{ITO}	An – Dn inputs to A – D Q outputs	0.59	0.67	0.79	0.85	ns, Max
T _{AXA}	AX inputs to AMUX output	0.31	0.35	0.42	0.44	ns, Max
T _{AXB}	AX inputs to BMUX output	0.35	0.39	0.47	0.50	ns, Max
T _{AXC}	AX inputs to CMUX output	0.39	0.44	0.52	0.56	ns, Max
T _{AXD}	AX inputs to DMUX output	0.42	0.47	0.55	0.60	ns, Max
T _{BXB}	BX inputs to BMUX output	0.30	0.34	0.39	0.44	ns, Max
T _{BXD}	BX inputs to DMUX output	0.38	0.43	0.50	0.55	ns, Max
T _{CXC}	CX inputs to CMUX output	0.26	0.29	0.34	0.37	ns, Max
T _{CXD}	CX inputs to DMUX output	0.30	0.34	0.40	0.44	ns, Max
T _{DXD}	DX inputs to DMUX output	0.30	0.33	0.38	0.43	ns, Max
T _{OPCYA}	An input to COUT output	0.32	0.36	0.41	0.47	ns, Max
T _{OPCYB}	Bn input to COUT output	0.32	0.36	0.41	0.47	ns, Max
T _{OPCYC}	Cn input to COUT output	0.27	0.30	0.34	0.40	ns, Max
T _{OPCYD}	Dn input to COUT output	0.25	0.28	0.32	0.37	ns, Max
T _{AXCY}	AX input to COUT output	0.25	0.28	0.33	0.36	ns, Max
T _{BXCY}	BX input to COUT output	0.22	0.24	0.28	0.31	ns, Max
T _{CXCY}	CX input to COUT output	0.15	0.17	0.20	0.22	ns, Max
T _{DXCY}	DX input to COUT output	0.14	0.16	0.19	0.21	ns, Max
T _{BYP}	CIN input to COUT output	0.06	0.07	0.08	0.09	ns, Max
T _{CINA}	CIN input to AMUX output	0.21	0.24	0.28	0.30	ns, Max
T _{CINB}	CIN input to BMUX output	0.23	0.25	0.29	0.31	ns, Max
T _{CINC}	CIN input to CMUX output	0.23	0.26	0.30	0.33	ns, Max
T _{CIND}	CIN input to DMUX output	0.25	0.29	0.33	0.36	ns, Max
Sequential Delays						
T _{CKO}	Clock to AQ – DQ outputs	0.29	0.33	0.39	0.44	ns, Max
T _{SHCKO}	Clock to AMUX – DMUX outputs	0.36	0.40	0.47	0.53	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T _{DICK} /T _{CKDI}	A – D input to CLK on A – D Flip Flops	0.30/0.17	0.36/0.18	0.43/0.20	0.44/0.25	ns, Min
T _{CECK_CLB} / T _{CKCE_CLB}	CE input to CLK on A – D Flip Flops	0.20/0.00	0.25/0.00	0.32/0.00	0.32/0.01	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D Flip Flops	0.39/–0.07	0.44/–0.07	0.52/–0.07	0.58/–0.08	ns, Min
T _{CINCK} /T _{CKCIN}	CIN input to CLK on A – D Flip Flops	0.16/0.12	0.19/0.14	0.24/0.16	0.23/0.22	ns, Min
Set/Reset						
T _{SRMIN}	SR input minimum pulse width	0.90	0.90	0.97	0.80	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops	0.52	0.58	0.68	0.77	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops	0.41	0.48	0.59	0.61	ns, Max
F _{TOG}	Toggle frequency (for export control)	1412.00	1286.40	1098.00	1098.00	MHz

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

Table 58: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Maximum Frequency							
F _{MAX}	With all registers used	600	540	450	450	410	MHz
F _{MAX_PATDET}	With pattern detector	551	483	408	408	356	MHz
F _{MAX_MULT_NOMREG}	Two register multiply without MREG	356	311	262	262	224	MHz
F _{MAX_MULT_NOMREG_PATDET}	Two register multiply without MREG with pattern detect	327	286	241	241	211	MHz
F _{MAX_PREADD_MULT_NOADREG}	Without ADREG	398	347	292	292	254	MHz
F _{MAX_PREADD_MULT_NOADREG_PATDET}	Without ADREG with pattern detect	398	347	292	292	254	MHz
F _{MAX_NOPIPELINEREG}	Without pipeline registers (MREG, ADREG)	266	233	196	196	171	MHz
F _{MAX_NOPIPELINEREG_PATDET}	Without pipeline registers (MREG, ADREG) with pattern detect	250	219	184	184	160	MHz

Configuration Switching Characteristics

Table 59: Configuration Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Power-up Timing Characteristics						
T _{PL} ⁽¹⁾	Program Latency	5	5	5	5	ms, Max
T _{POR} ⁽¹⁾	Power-on-Reset	15/55	15/55	15/55	15/60	ms, Min/Max
T _{ICCK}	CCLK (output) delay	400	400	400	400	ns, Min
T _{PROGRAM}	Program Pulse Width	250	250	250	250	ns, Min
Master/Slave Serial Mode Programming Switching						
T _{DCCK} /T _{CCKD}	DIN Setup/Hold, slave mode	4.0/0.0	4.0/0.0	4.0/0.0	4.5/0.0	ns, Min
T _{DSCCK} /T _{SCCKD}	DIN Setup/Hold, master mode	4.0/0.0	4.0/0.0	4.0/0.0	5.0/0.0	ns, Min
T _{CCO}	DOUT at 2.5V	6	6	6	7	ns, Max
	DOUT at 1.8V	6	6	6	7	ns, Max
F _{MCCK}	Maximum CCLK frequency, serial modes	105	105	105	70	MHz, Max
F _{MCCKTOL}	Frequency Tolerance, master mode with respect to nominal CCLK.	55	55	55	60	%
F _{MSCCK}	Slave mode external CCLK	100	100	100	100	MHz
SelectMAP Mode Programming Switching						
T _{SMDCK} /T _{SMCKD}	SelectMAP Data Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	5.5/0.0	ns, Min
T _{SMCSCCK} /T _{SMCKCS}	CSI_B Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	5.5/0.0	ns, Min
T _{SMCCKW} /T _{SMWCCK}	RDWR_B Setup/Hold	10.0/0.0	10.0/0.0	10.0/0.0	16.0/0.0	ns, Min
T _{SMCKCSO}	CSO_B clock to out (330 Ω pull-up resistor required)	6	6	6	7	ns, Max
T _{SMCO}	CCLK to DATA out in readback at 2.5V	6	6	6	7	ns, Max
	CCLK to DATA out in readback at 1.8V	6	6	6	7	ns, Max

Table 67: Clock-Capable Clock Input to Output Delay With MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Clock-capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> MMCM.							
T _{ICKOFMMCMCC}	Clock-capable Clock Input and OUTFF <i>with</i> MMCM	XC6VLX75T	2.22	2.38	2.63	2.72	ns
		XC6VLX130T	2.24	2.39	2.65	2.74	ns
		XC6VLX195T	2.24	2.40	2.65	2.75	ns
		XC6VLX240T	2.24	2.40	2.65	2.75	ns
		XC6VLX365T	2.25	2.42	2.65	2.76	ns
		XC6VLX550T	N/A	2.43	2.68	2.80	ns
		XC6VLX760	N/A	2.42	2.69	2.79	ns
		XC6VSX315T	2.23	2.38	2.65	2.73	ns
		XC6VSX475T	N/A	2.30	2.57	2.66	ns
		XC6VHX250T	2.25	2.41	2.67	N/A	ns
		XC6VHX255T	2.35	2.51	2.78	N/A	ns
		XC6VHX380T	2.27	2.43	2.69	N/A	ns
		XC6VHX565T	N/A	2.41	2.68	N/A	ns
		XQ6VLX130T	N/A	2.39	2.65	2.74	ns
		XQ6VLX240T	N/A	2.40	2.65	2.75	ns
		XQ6VLX550T	N/A	N/A	2.68	2.80	ns
		XQ6VSX315T	N/A	2.38	2.65	2.73	ns
		XQ6VSX475T	N/A	N/A	2.57	2.66	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Virtex-6 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 68. Values are expressed in nanoseconds unless otherwise noted.

Table 68: Global Clock Input Setup and Hold Without MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. ⁽¹⁾							
T _{PSFD} / T _{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF ⁽²⁾ without MMCM	XC6VLX75T	1.33/ 0.03	1.44/ 0.03	1.75/ 0.03	2.18/ −0.22	ns
		XC6VLX130T	1.31/ −0.08	1.54/ −0.08	1.88/ −0.08	2.31/ −0.12	ns
		XC6VLX195T	1.36/ −0.11	1.60/ −0.11	1.97/ −0.11	2.40/ −0.25	ns
		XC6VLX240T	1.36/ −0.11	1.60/ −0.11	1.97/ −0.11	2.40/ −0.25	ns
		XC6VLX365T	1.79/ −0.28	1.87/ −0.28	2.17/ −0.28	2.48/ −0.24	ns
		XC6VLX550T	N/A	2.22/ −0.12	2.36/ −0.12	2.77/ −0.26	ns
		XC6VLX760	N/A	2.19/ −0.24	2.35/ −0.24	2.71/ −0.21	ns
		XC6VSX315T	1.75/ −0.09	1.85/ −0.09	2.06/ −0.09	2.47/ −0.24	ns
		XC6VSX475T	N/A	2.14/ −0.14	2.31/ −0.14	2.71/ −0.30	ns
		XC6VHX250T	1.93/ −0.22	2.04/ −0.22	2.25/ −0.22	N/A	ns
		XC6VHX255T	1.81/ −0.33	2.11/ −0.33	2.56/ −0.33	N/A	ns
		XC6VHX380T	1.93/ −0.11	2.04/ −0.11	2.25/ −0.11	N/A	ns
		XC6VHX565T	N/A	2.20/ −0.12	2.39/ −0.12	N/A	ns
		XQ6VLX130T	N/A	1.54/ −0.08	1.88/ −0.08	2.31/ −0.12	ns
		XQ6VLX240T	N/A	1.60/ −0.11	1.97/ −0.11	2.40/ −0.25	ns
		XQ6VLX550T	N/A	N/A	2.36/ −0.12	2.77/ −0.26	ns
		XQ6VSX315T	N/A	1.85/ −0.09	2.06/ −0.09	2.47/ −0.24	ns
		XQ6VSX475T	N/A	N/A	2.31/ −0.14	2.71/ −0.30	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch
- A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 69: Global Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T _{PSMMCMGC} / T _{PHMMCMGC}	No Delay Global Clock Input and IFF(2) with MMCM	XC6VLX75T	1.45/ −0.18	1.57/ −0.18	1.72/ −0.18	1.78/ −0.08	ns
		XC6VLX130T	1.53/ −0.18	1.65/ −0.18	1.81/ −0.18	1.87/ −0.07	ns
		XC6VLX195T	1.54/ −0.17	1.66/ −0.17	1.82/ −0.17	1.87/ −0.08	ns
		XC6VLX240T	1.54/ −0.17	1.66/ −0.17	1.82/ −0.17	1.87/ −0.08	ns
		XC6VLX365T	1.55/ −0.18	1.67/ −0.18	1.83/ −0.18	1.87/ −0.07	ns
		XC6VLX550T	N/A	1.84/ −0.17	2.02/ −0.17	2.06/ −0.06	ns
		XC6VLX760	N/A	2.26/ −0.13	2.49/ −0.13	2.06/ −0.03	ns
		XC6VSX315T	1.56/ −0.18	1.68/ −0.18	1.84/ −0.18	1.89/ −0.08	ns
		XC6VSX475T	N/A	1.85/ −0.23	2.03/ −0.23	2.07/ −0.13	ns
		XC6VHX250T	1.52/ −0.17	1.64/ −0.17	1.80/ −0.17	N/A	ns
		XC6VHX255T	1.52/ −0.12	1.64/ −0.12	1.85/ −0.12	N/A	ns
		XC6VHX380T	1.68/ −0.16	1.81/ −0.16	1.99/ −0.16	N/A	ns
		XC6VHX565T	N/A	1.81/ −0.01	1.99/ −0.01	N/A	ns
		XQ6VLX130T	N/A	1.65/ −0.18	1.81/ −0.18	1.87/ −0.07	ns
		XQ6VLX240T	N/A	1.66/ −0.17	1.82/ −0.17	1.87/ −0.08	ns
		XQ6VLX550T	N/A	N/A	2.02/ −0.17	2.06/ −0.06	ns
		XQ6VSX315T	N/A	1.68/ −0.18	1.84/ −0.18	1.89/ −0.08	ns
		XQ6VSX475T	N/A	N/A	2.03/ −0.23	2.07/ −0.13	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 70: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard. ⁽¹⁾							
T _{PSMMCMCC} / T _{PHMMCMCC}	No Delay Clock-capable Clock Input and IFF ⁽²⁾ with MMCM	XC6VLX75T	1.56/ −0.25	1.69/ −0.25	1.86/ −0.25	1.91/ −0.15	ns
		XC6VLX130T	1.64/ −0.25	1.78/ −0.25	1.95/ −0.25	2.00/ −0.14	ns
		XC6VLX195T	1.65/ −0.24	1.79/ −0.24	1.96/ −0.24	2.01/ −0.15	ns
		XC6VLX240T	1.65/ −0.24	1.79/ −0.24	1.96/ −0.24	2.01/ −0.15	ns
		XC6VLX365T	1.66/ −0.25	1.79/ −0.25	1.97/ −0.25	2.02/ −0.15	ns
		XC6VLX550T	N/A	1.97/ −0.24	2.16/ −0.24	2.19/ −0.14	ns
		XC6VLX760	N/A	2.39/ −0.20	2.63/ −0.20	2.21/ −0.10	ns
		XC6VSX315T	1.67/ −0.25	1.80/ −0.25	1.98/ −0.25	2.03/ −0.16	ns
		XC6VSX475T	N/A	1.98/ −0.29	2.17/ −0.29	2.21/ −0.20	ns
		XC6VHX250T	1.63/ −0.24	1.76/ −0.24	1.94/ −0.24	N/A	ns
		XC6VHX255T	1.63/ −0.19	1.76/ −0.19	1.99/ −0.19	N/A	ns
		XC6VHX380T	1.80/ −0.23	1.94/ −0.23	2.13/ −0.23	N/A	ns
		XC6VHX565T	N/A	1.94/ −0.08	2.13/ −0.08	N/A	ns
		XQ6VLX130T	N/A	1.78/ −0.25	1.95/ −0.25	2.00/ −0.14	ns
		XQ6VLX240T	N/A	1.79/ −0.24	1.96/ −0.24	2.01/ −0.15	ns
		XQ6VLX550T	N/A	N/A	2.16/ −0.24	2.19/ −0.14	ns
		XQ6VSX315T	N/A	1.80/ −0.25	1.98/ −0.25	2.03/ −0.16	ns
		XQ6VSX475T	N/A	N/A	2.17/ −0.29	2.21/ −0.20	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 73: Sample Window

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{SAMP}	Sampling Error at Receiver Pins ⁽¹⁾	All	510	560	610	670	ps
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO ⁽²⁾	All	300	350	400	440	ps

Notes:

1. This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 MMCM jitter
 - MMCM accuracy (phase offset)
 - MMCM phase shift resolution
These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 74: Pin-to-Pin Setup/Hold and Clock-to-Out

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO						
T _{PSCS} /T _{PHCS}	Setup/Hold of I/O clock	−0.28/1.09	−0.28/1.16	−0.28/1.33	−0.18/1.79	ns
Pin-to-Pin Clock-to-Out Using BUFIO						
T _{ICKOFC}	Clock-to-Out of I/O clock	4.22	4.59	5.22	5.63	ns

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
07/16/09	1.1	Revised the maximum V_{CCAUX} and V_{IN} numbers in Table 2, page 2 . Removed empty column from Table 3, page 3 . Revised specifications on Table 20, page 13 . Updated Table 38, page 22 and added notes 1 and 2. Revised T_{DLYCCO_RDY} , $T_{IDELAYCTRL_RPW}$, and $T_{IDELAYPAT_JIT}$ in Table 53, page 41 . Updated Table 58, page 46 to more closely match the DSP48E1 speed specifications. Updated T_{TAPTCK}/T_{TCKTAP} in Table 59, page 49 . Updated XC6VLX130T parameters in Table 68 through Table 70, page 59 .
08/19/09	1.2	Added values for -1L voltages and speed grade in all pertinent tables. Added V_{FS} and notes to Table 1 and Table 2 . Removed DV_{PPIN} from the example in Figure 2 . Added networking applications to Table 41, page 25 . Changed and added to the block RAM F_{MAX} section in Table 57, page 44 including removing Note 12. Changed F_{PFDMAX} values and corrected units for $T_{STATPHAOFFSET}$ and $T_{OUTDUTY}$ in Table 64, page 52 . Updated Table 71, page 60 .
09/16/09	2.0	Added Virtex-6 HXT devices to entire document including GTH Transceiver Specifications . Updated speed specifications as described in Switching Characteristics , includes changes in Table 51 , Table 57 , Table 58 , and Table 66 through Table 70 . Comprehensive changes to Table 14 , Table 15 , and Table 16 . Added conditions to DV_{PPOUT} and revised description of T_{OSKEW} in Table 17 . Removed V_{ISE} specification and note from Table 18 . Added note 3 to Table 23 . Updated note 3 in Table 24 . Updated LVCMOS25 delays in Table 44 . Updated specification for T_{IOTPHZ} in Table 46 . Removed $T_{BUFHSKEW}$ from Table 71, page 60 and added values for $T_{BUFIOSKEW}$. Added values in Table 74 .