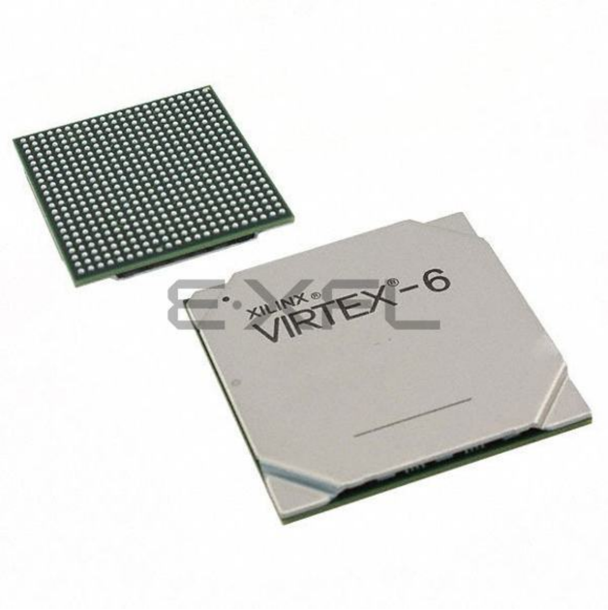
AMD Xilinx - XC6VLX240T-L1FFG1759I Datasheet



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Details	
Product Status	Active
Number of LABs/CLBs	18840
Number of Logic Elements/Cells	241152
Total RAM Bits	15335424
Number of I/O	720
Number of Gates	-
Voltage - Supply	0.91V ~ 0.97V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1759-BBGA, FCBGA
Supplier Device Package	1759-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vlx240t-l1ffg1759i

Important Note

Typical values for quiescent supply current are specified at nominal voltage, 85°C junction temperatures (T_j). Xilinx recommends analyzing static power consumption at T_j = 85°C because the majority of designs operate near the high end of the commercial temperature range. Quiescent supply current is specified by speed grade for Virtex-6 devices. Use the XPower™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified in Table 4.

Table 4: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed and Temperature Grade						Units
			-3 (C)	-2 (C, E, & I)	-1 (C & I)	-1 (I & M)(2)	-1L (C)	-1L (I)(1)	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC6VLX75T	927	927	927	N/A	656	741	mA
		XC6VLX130T	1563	1563	1563	N/A	1102	1245	mA
		XC6VLX195T	2059	2059	2059	N/A	1441	1628	mA
		XC6VLX240T	2478	2478	2478	N/A	1733	1957	mA
		XC6VLX365T	3001	3001	3001	N/A	2092	2363	mA
		XC6VLX550T(3)	N/A	4515	4515	N/A	3147	3555	mA
		XC6VLX760(3)	N/A	5094	5094	N/A	3471	3921	mA
		XC6VSX315T	3476	3476	3476	N/A	2409	2721	mA
		XC6VSX475T(3)	N/A	5227	5227	N/A	3622	4091	mA
		XC6VHX250T	2906	2906	2906	N/A	N/A	N/A	mA
		XC6VHX255T	2746	2746	2746	N/A	N/A	N/A	mA
		XC6VHX380T(4)	4160	4160	4160	N/A	N/A	N/A	mA
		XC6VHX565T(5)	N/A	5207	5207	N/A	N/A	N/A	mA
		XQ6VLX130T	N/A	1563	N/A	1563	N/A	1245	mA
		XQ6VLX240T	N/A	2478	N/A	2478	N/A	1957	mA
		XQ6VLX550T(7)	N/A	N/A	N/A	4515	N/A	3555	mA
		XQ6VSX315T	N/A	3476	N/A	3476	N/A	2721	mA
		XQ6VSX475T(7)	N/A	N/A	N/A	5227	N/A	4091	mA

Table 4: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed and Temperature Grade						Units
			-3 (C)	-2 (C, E, & I)	-1 (C & I)	-1 (I & M)(2)	-1L (C)	-1L (I)(1)	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC6VLX75T	45	45	45	N/A	45	45	mA
		XC6VLX130T	75	75	75	N/A	75	75	mA
		XC6VLX195T	113	113	113	N/A	113	113	mA
		XC6VLX240T	135	135	135	N/A	135	135	mA
		XC6VLX365T	191	191	191	N/A	191	191	mA
		XC6VLX550T(3)	N/A	286	286	N/A	286	286	mA
		XC6VLX760(3)	N/A	387	387	N/A	387	387	mA
		XC6VSX315T	186	186	186	N/A	186	186	mA
		XC6VSX475T(3)	N/A	279	279	N/A	279	279	mA
		XC6VHX250T	152	152	152	N/A	N/A	N/A	mA
		XC6VHX255T	152	152	152	N/A	N/A	N/A	mA
		XC6VHX380T(4)	227	227	227	N/A	N/A	N/A	mA
		XC6VHX565T(5)	N/A	315	315	N/A	N/A	N/A	mA
		XQ6VLX130T(6)	N/A	75	N/A	75	N/A	75	mA
		XQ6VLX240T(6)	N/A	135	N/A	135	N/A	135	mA
		XQ6VLX550T(7)	N/A	N/A	N/A	286	N/A	286	mA
		XQ6VSX315T(6)	N/A	186	N/A	186	N/A	186	mA
		XQ6VSX475T(7)	N/A	N/A	N/A	279	N/A	279	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j). -1 and -2 industrial (I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. -1L industrial temperature range devices have the values specified in this column.
2. Use the XPE tool to calculate 125°C values for -1M temperature range devices.
3. The -2E extended temperature range (T_j = 0°C to +100°C) is only available in these devices. The -2I temperature range (T_j = –40°C to +100°C) is available for all other devices except the XC6VHX565T.
4. The XC6VHX380T is available with both -2E and -2I temperature ranges.
5. The XC6VHX565T is only available in the following temperature ranges: -1C, -1I, -2C, and -2E.
6. The XQ6VLX130T, XQ6VLX240T, and XQ6VSX315T are available in -2I, -1I, -1M, and -1LI temperature ranges.
7. The XQ6VLX550T and the XQ6VSX475T are only available in -1I and -1LI temperature ranges.
8. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
9. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPE or XPower Analyzer (XPA) tools.

HT DC Specifications (HT_25)

Table 8: **HT DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage for XC devices	R_T = 100 Ω across Q and $\overline{Q}$ signals	480	600	885	mV
	Differential Output Voltage for XQ devices		480	600	930	mV
ΔV_{OD}	Change in V_{OD} Magnitude		–15	–	15	mV
V_{OCM}	Output Common Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	440	600	760	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		–15	–	15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		–15	–	15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		–15	–	15	mV

LVDS DC Specifications (LVDS_25)

Table 9: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage for XC devices	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
	Output Common-Mode Voltage for XQ devices		1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 10: **Extended LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.715	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High for XC devices	R_T = 100 Ω across Q and $\overline{Q}$ signals	350	–	840	mV
	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High for XQ devices		350	–	850	mV
V_{OCM}	Output Common-Mode Voltage for XC devices	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
	Output Common-Mode Voltage for XQ devices		1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	–	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

Table 23: **GTX Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.480	–	F_{GTXMAX}	Gb/s
T_{RTX}	TX Rise time	20%–80%	–	120	–	ps
T_{FTX}	TX Fall time	80%–20%	–	120	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	350	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	75	ns
$TJ_{6.5}$	Total Jitter(2)(3)	6.5 Gb/s	–	–	0.33	UI
$DJ_{6.5}$	Deterministic Jitter(2)(3)		–	–	0.17	UI
$TJ_{5.0}$	Total Jitter(2)(3)	5.0 Gb/s	–	–	0.33	UI
$DJ_{5.0}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{4.25}$	Total Jitter(2)(3)	4.25 Gb/s	–	–	0.33	UI
$DJ_{4.25}$	Deterministic Jitter(2)(3)		–	–	0.14	UI
$TJ_{3.75}$	Total Jitter(2)(3)	3.75 Gb/s	–	–	0.34	UI
$DJ_{3.75}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$TJ_{3.125}$	Total Jitter(2)(3)	3.125 Gb/s	–	–	0.2	UI
$DJ_{3.125}$	Deterministic Jitter(2)(3)		–	–	0.1	UI
$TJ_{3.125L}$	Total Jitter(2)(3)	3.125 Gb/s(4)	–	–	0.35	UI
$DJ_{3.125L}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$TJ_{2.5}$	Total Jitter(2)(3)	2.5 Gb/s(5)	–	–	0.20	UI
$DJ_{2.5}$	Deterministic Jitter(2)(3)		–	–	0.08	UI
$TJ_{1.25}$	Total Jitter(2)(3)	1.25 Gb/s(6)	–	–	0.15	UI
$DJ_{1.25}$	Deterministic Jitter(2)(3)		–	–	0.06	UI
TJ_{600}	Total Jitter(2)(3)	600 Mb/s	–	–	0.1	UI
DJ_{600}	Deterministic Jitter(2)(3)		–	–	0.03	UI
TJ_{480}	Total Jitter(2)(3)	480 Mb/s	–	–	0.1	UI
DJ_{480}	Deterministic Jitter(2)(3)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
2. Using PLL_DIVSEL_FB = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 1.5625 GHz and OUTDIV = 1.
5. PLL frequency at 2.5 GHz and OUTDIV = 2.
6. PLL frequency at 2.5 GHz and OUTDIV = 4.

Table 24: **GTX Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTXRX}	Serial data rate	RX oversampler not enabled	0.600	–	F_{GTXMAX}	Gb/s
		RX oversampler enabled	0.480	–	0.600	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–	75	–	ns
$RX_{OOBVDPP}$	OOB detect threshold peak-to-peak		60	–	150	mV
RX_{SST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000	–	0	ppm
RX_{RL}	Run length (CID)	Internal AC capacitor bypassed	–	–	512	UI
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance	CDR 2^{nd}-order loop disabled	–200	–	200	ppm
		CDR 2^{nd}-order loop enabled	–2000	–	2000	ppm
SJ Jitter Tolerance(2)						
$JT\_SJ_{6.5}$	Sinusoidal Jitter(3)	6.5 Gb/s	0.44	–	–	UI
$JT\_SJ_{5.0}$	Sinusoidal Jitter(3)	5.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{4.25}$	Sinusoidal Jitter(3)	4.25 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.75}$	Sinusoidal Jitter(3)	3.75 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.125}$	Sinusoidal Jitter(3)	3.125 Gb/s	0.45	–	–	UI
$JT\_SJ_{3.125L}$	Sinusoidal Jitter(3)	3.125 Gb/s(4)	0.45	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter(3)	2.5 Gb/s(5)	0.5	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter(3)	1.25 Gb/s(6)	0.5	–	–	UI
JT_SJ_{600}	Sinusoidal Jitter(3)	600 Mb/s	0.4	–	–	UI
JT_SJ_{480}	Sinusoidal Jitter(3)	480 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$JT\_TJSE_{3.125}$	Total Jitter with Stressed Eye(7)	3.125 Gb/s	0.70	–	–	UI
		5.0 Gb/s	0.70	–	–	UI
$JT\_SJSE_{3.125}$	Sinusoidal Jitter with Stressed Eye(7)	3.125 Gb/s	0.1	–	–	UI
		5.0 Gb/s	0.1	–	–	UI

Notes:

1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. PLL frequency at 1.5625 GHz and OUTDIV = 1.
5. PLL frequency at 2.5 GHz and OUTDIV = 2.
6. PLL frequency at 2.5 GHz and OUTDIV = 4.
7. Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Specifications

GTH Transceiver DC Characteristics

Table 25: **Absolute Maximum Ratings for GTH Transceivers(1)**

Symbol	Description	Min	Max	Units
MGTHAVCC	Analog supply voltage for the GTH transmitter, receiver, and common analog circuits	–0.5	1.125	V
MGTHAVCCRX	Analog supply voltage for the GTH receiver circuits and common analog circuits	–0.5	1.125	V
MGTHAVTT	Analog supply voltage for the GTH transmitter termination circuits	–0.5	1.32	V
MGTHAVCCPLL	Analog supply voltage for the GTH receiver and PLL circuits	–0.5	1.935	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.125	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.935	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 26: **Recommended Operating Conditions for GTH Transceivers (1)(2)**

Symbol	Description	Min	Typ	Max	Units
MGTHAVCC	Analog supply voltage for the GTH transmitter, receiver, and common analog circuits	1.075	1.1	1.125	V
MGTHAVCCRX	Analog supply voltage for the GTH receiver circuits and common analog circuits	1.075	1.1	1.125	V
MGTHAVTT	Analog supply voltage for the GTH transmitter termination circuits	1.140	1.2	1.26	V
MGTHAVCCPLL	Analog supply voltage for the GTH receiver and PLL circuit	1.710	1.8	1.89	V

Notes:

1. Each voltage listed requires the filter circuit described in UG371: *Virtex-6 FPGA GTH Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +100°C.

Table 27: **GTH Transceiver Power Supply Sequencing (1)(2)(3)**

Symbol	Description	Min	Max	Units
$T_{HAVCC2HAVCCRX}$	Maximum time between powering MGTHAVCC to when MGTHAVCCRX must be powered.	0	5	ms
$T_{HAVCCRX2HAVCCPLL}$	Minimum time between powering MGTHAVCCRX to when MGTHAVCCPLL can be powered.	10	–	µs
$T_{HAVCCRX2HAVTT}$	Minimum time between powering MGTHAVCCRX to when MGTHAVTT can be powered.	10	–	µs

Notes:

1. MGTHAVCCRX must be powered simultaneously or within $T_{HAVCC2HAVCCRX}$ of MGTHAVCC, but it must not precede MGTHAVCC.
2. MGTHAVCC and MGTHAVCCRX must be powered before MGTHAVCCPLL and MGTHAVTT. This minimum time is defined by $T_{HAVCCRX2HAVCCPLL}$ and $T_{HAVCCRX2HAVTT}$.
3. At any time, the condition of MGTHAVCC being present and MGTHAVCCRX not being present should not occur for more than the maximum $T_{HAVCC2HAVCCRX}$.

Figure 4 shows the timing parameters in Table 27.

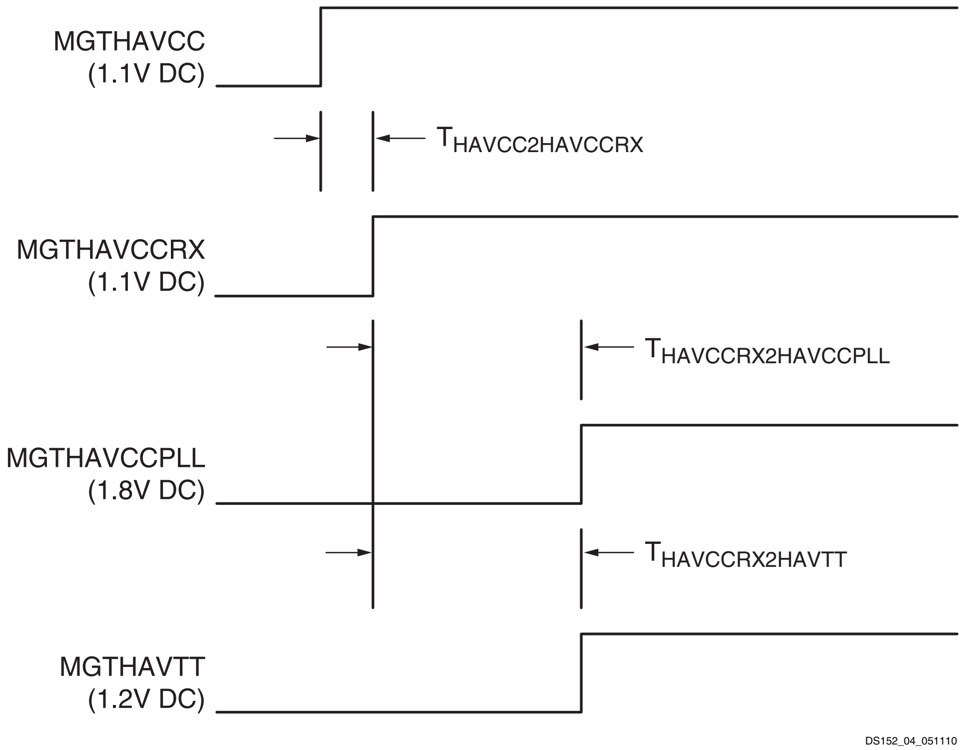

Figure 4: **GTH Transceiver Power Supply Power-On Sequencing**

Table 28: **GTH Transceiver Supply Current**

Symbol	Description	Typ[(1)]	Max	Units
$I_{MGTHAVCC}$	MGTHAVCC supply current for one GTH Quad (4 lanes)	571	Note 2	mA
$I_{MGTHAVCCRX}$	MGTHAVCCRX supply current for a GTH Quad (4 lanes)	254	Note 2	mA
$I_{MGTHAVTT}$	MGTHAVTT supply current for one GTH Quad (4 lanes)	93	Note 2	mA
$I_{MGTHAVCCPLL}$	MGTHAVCCPLL supply current for one GTH Quad (4 lanes)	219	Note 2	mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	1000.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 10.3125 Gb/s line rate.
2. Values for currents other than the values specified in this table can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

Table 29: **GTH Transceiver Quiescent Supply Current(1)(2)**

Symbol	Description	Typ(3)	Max	Units
$I_{MGTHAVCCQ}$	Quiescent MGTHAVCC Supply Current for one GTH Quad (4 lanes)	65	Note 4	mA
$I_{MGTHAVCCRXQ}$	Quiescent MGTHAVCCRX Supply Current for one GTH Quad (4 lanes)	17	Note 4	mA
$I_{MGTHAVTTQ}$	Quiescent MGTHAVTT Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA
$I_{MGTHAVCCPLLQ}$	Quiescent MGTHAVCCPLL Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA

Notes:

1. Device powered and unconfigured.
2. GTH transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTH transceivers.
3. Typical values are specified at nominal voltage, 25°C.
4. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at: http://www.xilinx.com/technology/protocols/pciexpress.htm

Table 39: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$F_{PIPECLK}$	Pipe clock maximum frequency	250	250	250	250	MHz
$F_{USERCLK}$	User clock maximum frequency	500	500	250	250	MHz
F_{DRPCLK}	DRP clock maximum frequency	250	250	250	250	MHz

System Monitor Analog-to-Digital Converter Specification

Table 40: **Analog-to-Digital Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
AV_{DD} = 2.5V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_j = –55°C to 125°C M-Grade, Typical values at T_j=+35°C						
DC Accuracy: All external input channels. Both unipolar and bipolar modes.						
Resolution			10	–	–	Bits
Integral Nonlinearity	INL		–	–	±1	LSBs
Differential Nonlinearity	DNL	No missing codes (T_{MIN} to T_{MAX}) Guaranteed Monotonic	–	–	±0.9	LSBs
Unipolar Offset Error (1)		Uncalibrated	–	±2	±30	LSBs
Bipolar Offset Error (1)		Uncalibrated measured in bipolar mode	–	±2	±30	LSBs
Gain Error		Uncalibrated - External Reference	–	±0.2	±2	%
		Uncalibrated - Internal Reference	–	±2	–	%
Bipolar Gain Error (1)		Uncalibrated - External Reference	–	±0.2	±2	%
		Uncalibrated - Internal Reference	–	±2	–	%
Total Unadjusted Error (Uncalibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	–	±10	–	LSBs
		Deviation from ideal transfer function. Internal reference	–	±20	–	LSBs
Total Unadjusted Error (Calibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	–	±1	±2	LSBs
Calibrated Gain Temperature Coefficient		Variation of FS code with temperature	–	±0.01	–	LSB/°C
DC Common-Mode Reject	$CMRR_{DC}$	$V_N = V_{CM}$ = 0.5V ± 0.5V, $V_P – V_N$ = 100mV	–	70	–	dB
Conversion Rate(2)						
Conversion Time - Continuous	t_{CONV}	Number of CLK cycles	26	–	32	
Conversion Time - Event	t_{CONV}	Number of CLK cycles	–	–	21	
T/H Acquisition Time	t_{ACQ}	Number of CLK cycles	4	–	–	
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	80	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
CLK Duty cycle			40	–	60	%

Table 40: **Analog-to-Digital Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Analog Inputs[3]						
Dedicated Analog Inputs Input Voltage Range V_P - V_N		Unipolar Operation	0	–	1	Volts
		Bipolar Operation	–0.5	–	+0.5	
		Unipolar Common Mode Range (FS input)	0	–	+0.5	
		Bipolar Common Mode Range (FS input)	+0.5	–	+0.6	
		Bandwidth	–	20	–	MHz
Auxiliary Analog Inputs Input Voltage Range $V_{AUXP[0]}$ /$V_{AUXN[0]}$ to $V_{AUXP[15]}$ /$V_{AUXN[15]}$ T_j = –55°C to 125°C		Unipolar Operation	0	–	1	Volts
		Bipolar Operation	–0.5	–	+0.5	
		Unipolar Common Mode Range (FS input)	0	–	+0.5	
		Bipolar Common Mode Range (FS input)	+0.5	–	+0.6	
		Bandwidth	–	10	–	kHz
Input Leakage Current		A/D not converting, ADCCLK stopped	–	±1.0	–	µA
Input Capacitance			–	10	–	pF
On-chip Supply Monitor Error		V_{CCINT} and V_{CCAUX} with calibration enabled. External 1.25V reference T_j = –55°C to 125°C.	–	–	±1.0	% Reading
		V_{CCINT} and V_{CCAUX} with calibration enabled. Internal reference T_j = –40°C to 100°C.[4]	–	±2	–	% Reading
On-chip Temperature Monitor Error		T_j = –55°C to +125°C with calibration enabled. External 1.25V reference.	–	–	±4	°C
		T_j = –40°C to +100°C with calibration enabled. Internal reference.[4]	–	±5	–	°C
External Reference Inputs[5]						
Positive Reference Input Voltage Range	V_{REFP}	Measured Relative to V_{REFN}	1.20	1.25	1.30	Volts
Negative Reference Input Voltage Range	V_{REFN}	Measured Relative to AGND	–50	0	100	mV
Input current	I_{REF}	ADCCLK = 5.2 MHz	–	–	100	µA
Power Requirements						
Analog Power Supply	AV_{DD}	Measured Relative to AV_{SS}	2.375	2.5	2.625	Volts
Analog Supply Current	AI_{DD}	ADCCLK = 5.2 MHz	–	–	12	mA

Notes:

1. Offset errors are removed by enabling the System Monitor automatic gain calibration feature.
2. See "System Monitor Timing" in UG370: *Virtex-6 FPGA System Monitor User Guide*
3. See "Analog Inputs" in UG370: *Virtex-6 FPGA System Monitor User Guide* for a detailed description.
4. These internal references are not specified over the junction temperature operating range for military (M) temperature devices.
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function.This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

Table 44: **IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDCI_DV2_25	0.51	0.57	0.66	0.70	1.71	1.83	2.01	2.00	1.71	1.83	2.01	2.00	ns
LVDCI_DV2_18	0.55	0.61	0.71	0.73	1.69	1.81	2.00	1.98	1.69	1.81	2.00	1.98	ns
LVDCI_DV2_15	0.64	0.73	0.85	0.85	1.68	1.77	1.91	1.98	1.68	1.77	1.91	1.98	ns
LVPECL_25	0.85	0.94	1.09	1.08	1.38	1.49	1.65	1.64	1.38	1.49	1.65	1.64	ns
HSTL_I_12	0.81	0.91	1.06	1.06	1.48	1.60	1.78	1.74	1.48	1.60	1.78	1.74	ns
HSTL_I_DCI	0.81	0.91	1.06	1.06	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
HSTL_II_DCI	0.81	0.91	1.06	1.06	1.37	1.49	1.68	1.66	1.37	1.49	1.68	1.66	ns
HSTL_II_T_DCI	0.81	0.91	1.06	1.06	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
HSTL_III_DCI	0.81	0.91	1.06	1.06	1.34	1.45	1.62	1.61	1.34	1.45	1.62	1.61	ns
HSTL_I_DCI_18	0.81	0.91	1.06	1.06	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
HSTL_II_DCI_18	0.81	0.91	1.06	1.06	1.36	1.46	1.62	1.59	1.36	1.46	1.62	1.59	ns
HSTL_II _T_DCI_18	0.81	0.91	1.06	1.06	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
HSTL_III_DCI_18	0.81	0.91	1.06	1.06	1.43	1.54	1.69	1.67	1.43	1.54	1.69	1.67	ns
DIFF_HSTL_I_18	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
DIFF_HSTL_I_DCI_18	0.85	0.94	1.09	1.08	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
DIFF_HSTL_I	0.85	0.94	1.09	1.08	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns
DIFF_HSTL_I_DCI	0.85	0.94	1.09	1.08	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
DIFF_HSTL_II_18	0.85	0.94	1.09	1.08	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
DIFF_HSTL_II_DCI_18	0.85	0.94	1.09	1.08	1.36	1.46	1.62	1.59	1.36	1.46	1.62	1.59	ns
DIFF_HSTL_II _T_DCI_18	0.85	0.94	1.09	1.08	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
DIFF_HSTL_II	0.85	0.94	1.09	1.08	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
DIFF_HSTL_II_DCI	0.85	0.94	1.09	1.08	1.37	1.49	1.68	1.66	1.37	1.49	1.68	1.66	ns
SSTL2_I_DCI	0.81	0.91	1.06	1.06	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
SSTL2_II_DCI	0.81	0.91	1.06	1.06	1.39	1.50	1.67	1.69	1.39	1.50	1.67	1.69	ns
SSTL2_II_T_DCI	0.81	0.91	1.06	1.06	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
SSTL18_I	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
SSTL18_II	0.81	0.91	1.06	1.06	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
SSTL18_I_DCI	0.81	0.91	1.06	1.06	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
SSTL18_II_DCI	0.81	0.91	1.06	1.06	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
SSTL18_II_T_DCI	0.81	0.91	1.06	1.06	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL2_I	0.85	0.94	1.09	1.08	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
DIFF_SSTL2_I_DCI	0.85	0.94	1.09	1.08	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
DIFF_SSTL2_II	0.85	0.94	1.09	1.08	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
DIFF_SSTL2_II_DCI	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.69	1.39	1.50	1.67	1.69	ns
DIFF_SSTL2_II_T_DCI	0.85	0.94	1.09	1.08	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns

Table 44: **IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices** ***(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
DIFF_SSTL18_I	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
DIFF_SSTL18_I_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL18_II	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
DIFF_SSTL18_II_DCI	0.85	0.94	1.09	1.08	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
DIFF_SSTL18_II_T_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
DIFF_SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns

Table 45: **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices**

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVDS_25	0.94	1.09	1.08	1.54	2.16	1.62	1.54	2.16	1.62	ns
LVDSEXT_25	0.94	1.09	1.08	1.65	2.20	1.73	1.65	2.20	1.73	ns
HT_25	0.94	1.09	1.08	1.62	2.20	1.69	1.62	2.20	1.69	ns
BLVDS_25	0.94	1.09	1.08	1.50	3.18	1.65	1.50	3.18	1.65	ns
RSDS_25 (point to point)	0.94	1.09	1.08	1.54	2.22	1.62	1.54	2.22	1.62	ns
HSTL_I	0.91	1.06	1.06	1.56	2.44	1.71	1.56	2.44	1.71	ns
HSTL_II	0.91	1.06	1.06	1.56	2.21	1.72	1.56	2.21	1.72	ns
HSTL_III	0.91	1.06	1.06	1.54	2.50	1.69	1.54	2.50	1.69	ns
HSTL_I_18	0.91	1.06	1.06	1.58	2.43	1.72	1.58	2.43	1.72	ns
HSTL_II_18	0.91	1.06	1.06	1.62	2.30	1.78	1.62	2.30	1.78	ns
HSTL_III_18	0.91	1.06	1.06	1.54	2.49	1.69	1.54	2.49	1.69	ns
SSTL2_I	0.91	1.06	1.06	1.60	2.50	1.74	1.60	2.50	1.74	ns
SSTL2_II	0.91	1.06	1.06	1.54	2.49	1.71	1.54	2.49	1.71	ns
SSTL15	0.91	1.06	1.06	1.54	2.07	1.69	1.54	2.07	1.69	ns
LVCMOS25, Slow, 2 mA	0.57	0.66	0.70	5.46	6.01	5.63	5.46	6.01	5.63	ns
LVCMOS25, Slow, 4 mA	0.57	0.66	0.70	3.49	3.79	3.65	3.49	3.79	3.65	ns
LVCMOS25, Slow, 6 mA	0.57	0.66	0.70	2.81	3.08	2.95	2.81	3.08	2.95	ns
LVCMOS25, Slow, 8 mA	0.57	0.66	0.70	2.41	2.72	2.59	2.41	2.72	2.59	ns
LVCMOS25, Slow, 12 mA	0.57	0.66	0.70	1.95	2.23	2.10	1.95	2.23	2.10	ns
LVCMOS25, Slow, 16 mA	0.57	0.66	0.70	2.05	2.29	2.21	2.05	2.29	2.21	ns
LVCMOS25, Slow, 24 mA	0.57	0.66	0.70	1.82	2.24	1.98	1.82	2.24	1.98	ns
LVCMOS25, Fast, 2 mA	0.57	0.66	0.70	5.49	6.04	5.62	5.49	6.04	5.62	ns
LVCMOS25, Fast, 4 mA	0.57	0.66	0.70	3.50	3.82	3.65	3.50	3.82	3.65	ns
LVCMOS25, Fast, 6 mA	0.57	0.66	0.70	2.73	2.99	2.88	2.73	2.99	2.88	ns
LVCMOS25, Fast, 8 mA	0.57	0.66	0.70	2.33	2.65	2.53	2.33	2.65	2.53	ns
LVCMOS25, Fast, 12 mA	0.57	0.66	0.70	1.88	2.08	2.03	1.88	2.08	2.03	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 47 shows the test setup parameters used for measuring input delay.

Table 47: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(5)	V_{REF} (1)(3)(5)
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	$V_{REF} – 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL, Class III	HSTL_III	$V_{REF} – 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} – 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	$V_{REF} – 0.5$	$V_{REF} + 0.5$	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	$V_{REF} – 1.00$	$V_{REF} + 1.00$	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	$V_{REF} – 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} – 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
HT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 6.
6. The value given is the differential input voltage.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 55: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Sequential Delays						
T_{SHCKO}	Clock to A – B outputs	0.92	1.10	1.36	1.49	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	1.19	1.40	1.71	1.87	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{DS}/T_{DH}	A – D inputs to CLK	0.62/0.18	0.72/0.20	0.88/0.22	0.98/0.23	ns, Min
T_{AS}/T_{AH}	Address An inputs to clock	0.19/0.52	0.22/0.59	0.27/0.66	0.30/0.75	ns, Min
T_{WS}/T_{WH}	WE input to clock	0.27/0.00	0.32/0.00	0.40/0.00	0.47/–0.03	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.28/–0.01	0.34/–0.01	0.41/–0.01	0.48/–0.05	ns, Min
Clock CLK						
T_{MPW}	Minimum pulse width	0.70	0.82	1.00	1.04	ns, Min
T_{MCP}	Minimum clock period	1.40	1.64	2.00	2.08	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 56: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Sequential Delays						
T_{REG}	Clock to A – D outputs	1.11	1.30	1.58	1.74	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.37	1.60	1.93	2.12	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	1.08	1.27	1.55	1.74	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{WS}/T_{WH}	WE input	0.05/0.00	0.07/0.00	0.09/0.00	0.11/0.03	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.06/–0.01	0.08/–0.01	0.10/–0.01	0.12/0.02	ns, Min
T_{DS}/T_{DH}	A – D inputs to CLK	0.64/0.18	0.76/0.21	0.94/0.24	1.07/0.23	ns, Min
Clock CLK						
T_{MPW}	Minimum pulse width	0.60	0.70	0.85	0.89	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Table 58: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Maximum Frequency							
F_{MAX}	With all registers used	600	540	450	450	410	MHz
F_{MAX_PATDET}	With pattern detector	551	483	408	408	356	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	356	311	262	262	224	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	327	286	241	241	211	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	398	347	292	292	254	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	398	347	292	292	254	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	266	233	196	196	171	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	250	219	184	184	160	MHz

Configuration Switching Characteristics

Table 59: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Power-up Timing Characteristics						
T_{PL}(1)	Program Latency	5	5	5	5	ms, Max
T_{POR}(1)	Power-on-Reset	15/55	15/55	15/55	15/60	ms, Min/Max
T_{ICCK}	CCLK (output) delay	400	400	400	400	ns, Min
$T_{PROGRAM}$	Program Pulse Width	250	250	250	250	ns, Min
Master/Slave Serial Mode Programming Switching						
T_{DCCK}/T_{CCKD}	DIN Setup/Hold, slave mode	4.0/0.0	4.0/0.0	4.0/0.0	4.5/0.0	ns, Min
T_{DSCCK}/T_{SCCKD}	DIN Setup/Hold, master mode	4.0/0.0	4.0/0.0	4.0/0.0	5.0/0.0	ns, Min
T_{CCO}	DOUT at 2.5V	6	6	6	7	ns, Max
	DOUT at 1.8V	6	6	6	7	ns, Max
F_{MCCK}	Maximum CCLK frequency, serial modes	105	105	105	70	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance, master mode with respect to nominal CCLK.	55	55	55	60	%
F_{MSCCK}	Slave mode external CCLK	100	100	100	100	MHz
SelectMAP Mode Programming Switching						
T_{SMDCCK}/T_{SMCCKD}	SelectMAP Data Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	5.5/0.0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	5.5/0.0	ns, Min
T_{SMCCKW}/T_{SMWCCK}	RDWR_B Setup/Hold	10.0/0.0	10.0/0.0	10.0/0.0	16.0/0.0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)	6	6	6	7	ns, Max
T_{SMCO}	CCLK to DATA out in readback at 2.5V	6	6	6	7	ns, Max
	CCLK to DATA out in readback at 1.8V	6	6	6	7	ns, Max

Table 59: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$	DI Setup/Hold	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$	DEN Setup/Hold time	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$	DWE Setup/Hold time	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{MMCMCKO\_DO}$	CLK to out of DO(3)	2.60	3.02	3.64	3.68	ns
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY	0.32	0.34	0.38	0.38	ns

Notes:

1. To support longer delays in configuration, use the design solutions described in UG360: *Virtex-6 FPGA Configuration User Guide*.
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
3. DO will hold until next DRP operation.

Clock Buffers and Networks

Table 60: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-2	-1	-1L	
T_{BCCCK_CE}/T_{BCCKC_CE}(1)	CE pins Setup/Hold	All	0.11/ 0.00	0.13/ 0.00	0.16/ 0.00	0.13/ 0.00	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins Setup/Hold	All	0.11/ 0.00	0.13/ 0.00	0.16/ 0.00	0.13/ 0.00	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	All	0.07	0.08	0.10	0.10	ns
Maximum Frequency							
F_{MAX}	Global clock tree (BUFG)	All except LX760	800	750	700	667	MHz
		LX760	N/A	700	700	667	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 61: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BIOCKO_O}	Clock to out delay from I to O	0.14	0.16	0.18	0.21	ns
Maximum Frequency						
F_{MAX}	I/O clock tree (BUFIO)	800	800	710	710	MHz

Table 62: **Regional Clock Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BRCKO_O}	Clock to out delay from I to O	0.56	0.62	0.73	0.82	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.28	0.31	0.36	0.41	ns

Table 66: **Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM.							
$T_{ICKOFMMCMGC}$	Global Clock Input and OUTFF *with* MMCM	XC6VLX75T	2.34	2.50	2.77	2.85	ns
		XC6VLX130T	2.35	2.51	2.78	2.87	ns
		XC6VLX195T	2.36	2.52	2.79	2.88	ns
		XC6VLX240T	2.36	2.52	2.79	2.88	ns
		XC6VLX365T	2.37	2.53	2.79	2.89	ns
		XC6VLX550T	N/A	2.55	2.82	2.93	ns
		XC6VLX760	N/A	2.54	2.82	2.92	ns
		XC6VSX315T	2.35	2.51	2.79	2.87	ns
		XC6VSX475T	N/A	2.43	2.70	2.79	ns
		XC6VHX250T	2.36	2.53	2.80	N/A	ns
		XC6VHX255T	2.46	2.63	2.91	N/A	ns
		XC6VHX380T	2.39	2.59	2.83	N/A	ns
		XC6VHX565T	N/A	2.54	2.81	N/A	ns
		XQ6VLX130T	N/A	2.51	2.78	2.87	ns
		XQ6VLX240T	N/A	2.52	2.79	2.88	ns
		XQ6VLX550T	N/A	N/A	2.82	2.93	ns
		XQ6VSX315T	N/A	2.51	2.79	2.87	ns
		XQ6VSX475T	N/A	N/A	2.70	2.79	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Virtex-6 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 68. Values are expressed in nanoseconds unless otherwise noted.

Table 68: **Global Clock Input Setup and Hold Without MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSFD}/ T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF(2) without MMCM	XC6VLX75T	1.33/ 0.03	1.44/ 0.03	1.75/ 0.03	2.18/ –0.22	ns
		XC6VLX130T	1.31/ –0.08	1.54/ –0.08	1.88/ –0.08	2.31/ –0.12	ns
		XC6VLX195T	1.36/ –0.11	1.60/ –0.11	1.97/ –0.11	2.40/ –0.25	ns
		XC6VLX240T	1.36/ –0.11	1.60/ –0.11	1.97/ –0.11	2.40/ –0.25	ns
		XC6VLX365T	1.79/ –0.28	1.87/ –0.28	2.17/ –0.28	2.48/ –0.24	ns
		XC6VLX550T	N/A	2.22/ –0.12	2.36/ –0.12	2.77/ –0.26	ns
		XC6VLX760	N/A	2.19/ –0.24	2.35/ –0.24	2.71/ –0.21	ns
		XC6VSX315T	1.75/ –0.09	1.85/ –0.09	2.06/ –0.09	2.47/ –0.24	ns
		XC6VSX475T	N/A	2.14/ –0.14	2.31/ –0.14	2.71/ –0.30	ns
		XC6VHX250T	1.93/ –0.22	2.04/ –0.22	2.25/ –0.22	N/A	ns
		XC6VHX255T	1.81/ –0.33	2.11/ –0.33	2.56/ –0.33	N/A	ns
		XC6VHX380T	1.93/ –0.11	2.04/ –0.11	2.25/ –0.11	N/A	ns
		XC6VHX565T	N/A	2.20/ –0.12	2.39/ –0.12	N/A	ns
		XQ6VLX130T	N/A	1.54/ –0.08	1.88/ –0.08	2.31/ –0.12	ns
		XQ6VLX240T	N/A	1.60/ –0.11	1.97/ –0.11	2.40/ –0.25	ns
		XQ6VLX550T	N/A	N/A	2.36/ –0.12	2.77/ –0.26	ns
		XQ6VSX315T	N/A	1.85/ –0.09	2.06/ –0.09	2.47/ –0.24	ns
		XQ6VSX475T	N/A	N/A	2.31/ –0.14	2.71/ –0.30	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 70: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard.[1]							
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No Delay Clock-capable Clock Input and IFF[2] with MMCM	XC6VLX75T	1.56/ –0.25	1.69/ –0.25	1.86/ –0.25	1.91/ –0.15	ns
		XC6VLX130T	1.64/ –0.25	1.78/ –0.25	1.95/ –0.25	2.00/ –0.14	ns
		XC6VLX195T	1.65/ –0.24	1.79/ –0.24	1.96/ –0.24	2.01/ –0.15	ns
		XC6VLX240T	1.65/ –0.24	1.79/ –0.24	1.96/ –0.24	2.01/ –0.15	ns
		XC6VLX365T	1.66/ –0.25	1.79/ –0.25	1.97/ –0.25	2.02/ –0.15	ns
		XC6VLX550T	N/A	1.97/ –0.24	2.16/ –0.24	2.19/ –0.14	ns
		XC6VLX760	N/A	2.39/ –0.20	2.63/ –0.20	2.21/ –0.10	ns
		XC6VSX315T	1.67/ –0.25	1.80/ –0.25	1.98/ –0.25	2.03/ –0.16	ns
		XC6VSX475T	N/A	1.98/ –0.29	2.17/ –0.29	2.21/ –0.20	ns
		XC6VHX250T	1.63/ –0.24	1.76/ –0.24	1.94/ –0.24	N/A	ns
		XC6VHX255T	1.63/ –0.19	1.76/ –0.19	1.99/ –0.19	N/A	ns
		XC6VHX380T	1.80/ –0.23	1.94/ –0.23	2.13/ –0.23	N/A	ns
		XC6VHX565T	N/A	1.94/ –0.08	2.13/ –0.08	N/A	ns
		XQ6VLX130T	N/A	1.78/ –0.25	1.95/ –0.25	2.00/ –0.14	ns
		XQ6VLX240T	N/A	1.79/ –0.24	1.96/ –0.24	2.01/ –0.15	ns
		XQ6VLX550T	N/A	N/A	2.16/ –0.24	2.19/ –0.14	ns
		XQ6VSX315T	N/A	1.80/ –0.25	1.98/ –0.25	2.03/ –0.16	ns
		XQ6VSX475T	N/A	N/A	2.17/ –0.29	2.21/ –0.20	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 73: **Sample Window**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{SAMP}	Sampling Error at Receiver Pins(1)	All	510	560	610	670	ps
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO(2)	All	300	350	400	440	ps

Notes:

1. This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution
   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 74: **Pin-to-Pin Setup/Hold and Clock-to-Out**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO						
T_{PSCS}/T_{PHCS}	Setup/Hold of I/O clock	–0.28/1.09	–0.28/1.16	–0.28/1.33	–0.18/1.79	ns
Pin-to-Pin Clock-to-Out Using BUFIO						
$T_{ICKOFCS}$	Clock-to-Out of I/O clock	4.22	4.59	5.22	5.63	ns

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
07/16/09	1.1	Revised the maximum V_{CCAUX} and V_{IN} numbers in Table 2, page 2. Removed empty column from Table 3, page 3. Revised specifications on Table 20, page 13. Updated Table 38, page 22 and added notes 1 and 2. Revised T_{DLYCCO_RDY}, $T_{IDELAYCTRL\_RPW}$, and $T_{IDELAYPAT\_JIT}$ in Table 53, page 41. Updated Table 58, page 46 to more closely match the DSP48E1 speed specifications. Updated T_{TAPTCK}/T_{TCKTAP} in Table 59, page 49. Updated XC6VLX130T parameters in Table 68 through Table 70, page 59.
08/19/09	1.2	Added values for -1L voltages and speed grade in all pertinent tables. Added V_{FS} and notes to Table 1 and Table 2. Removed DV_{PPIN} from the example in Figure 2. Added networking applications to Table 41, page 25. Changed and added to the block RAM F_{MAX} section in Table 57, page 44 including removing Note 12. Changed F_{PFDMAX} values and corrected units for $T_{STATPHAOFFSET}$ and $T_{OUTDUTY}$ in Table 64, page 52. Updated Table 71, page 60.
09/16/09	2.0	Added Virtex-6 HXT devices to entire document including GTH Transceiver Specifications. Updated speed specifications as described in Switching Characteristics, includes changes in Table 51, Table 57, Table 58, and Table 66 through Table 70. Comprehensive changes to Table 14, Table 15, and Table 16. Added conditions to D_{VPPOUT} and revised description of T_{OSKEW} in Table 17. Removed V_{ISE} specification and note from Table 18. Added note 3 to Table 23. Updated note 3 in Table 24. Updated LVCMOS25 delays in Table 44. Updated specification for T_{IOTPHZ} in Table 46. Removed $T_{BUFHSKEW}$ from Table 71, page 60 and added values for $T_{BUFIOSKEW}$. Added values in Table 74.

Date	Version	Description of Revisions
02/08/11	2.12	Removed note 1 from Table 4 as the larger devices (XC6VLX550T, XC6VLX760, XC6VSX475T, and XC6VHX565T) are now offered in -2I. Updated Table 4 and Table 5 with data for the XC6VHX380T in the FF(G)1154 package. In Table 41, updated -1L specification for DDR3. Added Note 1 to Table 42. Moved the XC6VHX380Tdevices in the FF(G)1154 package to production release in Table 43 using ISE 12.4 software with current speed specifications. Updated description for F_{INDUTY} in Table 64.
02/25/11	3.0	Designated the data sheet as Preliminary for all devices not already labeled production in Table 42. Changed the XC6VHX380T devices in all packages to production status in Table 42 and Table 43. Removed note 1 from Table 42. Added maximum specifications to Table 25. Updated $T_{HAVCC2HAVCCRX}$ in Table 27. Updated the typical values and notes in Table 28 and Table 29. Added values to Table 30 and Table 31. In Table 34, added values for T_{LOCK} and T_{PHASE}. Updated the values in Table 36 and added note 3. Updated Table 37 and added note 4.
03/21/11	3.1	Updated Table 2 including Note 7. In Table 4, added Note 3 and -2E, extended temperature range to the XC6VLX550T, XC6VLX760, XC6VSX475T, and XC6VHX380T devices, and added Note 5 for the XC6VHX565T. Updated Table 28 typical values. Updated the description for $F_{IDELAYCTRL\_REF}$ in Table 53. Updated F_{MCCK} in Table 59.
04/01/11	3.2	Added Tj values for C, E, and I temperature ranges to Table 2. Updated the I_{CCQ} values in Table 4. Updated F_{GCLK} in Table 34. Designated the data sheet as Production for all devices not already labeled production in Table 42. Changed the XC6VHX255T and XC6VHX565T devices in all packages to production status in Table 42 and Table 43. This included updates to the Virtex-6 Device Pin-to-Pin Output Parameter Guidelines and Virtex-6 Device Pin-to-Pin Input Parameter Guidelines for these devices. Production speed specifications for these devices are available using the speed specification v1.14 in the ISE 13.1 software update. Updated and added package skew values to Table 72; these values are correct with regards to previous production released speed specifications in software. Updated copyright page 1 and Notice of Disclaimer.
12/08/11	3.3	Production release of the Defense-grade XQ devices in Table 42 and Table 43 using ISE v13.3 v1.17 Patch for -2 and -1 speed specifications; and v1.10 for -1L speed specifications. Added the XQ6VLX130T, XQ6VLX240T, XQ6VLX550T, XQ6VSX315T, and XQ6VSX475T to the data sheet which included adding Table 45. Updated T_j in Table 2. In Table 40, updated T_j for most specifications and added Note 4. Added Note 4 to Table 41. Added -1(XQ) speed specification columns only to Table 50, Table 51, Table 52, and Table 58. Updated V_{OD} in Table 8, V_{OCM} in Table 9, and V_{OCM} and V_{DIFF} in Table 10. Updated the Power-On Power Supply Requirements section. In Table 27, updated maximum specification for $T_{HAVCC2HAVCCRX}$ and added Note 3. Updated Tj in Table 40. In Table 41, increased the DDR LVDS receiver (SPI-4.2) -1 speed grade performance value from 1.0 Gb/s to 1.1 Gb/s. In Table 60, updated the F_{MAX} to add a separate row for the LX760 device values. The speed specifications in the software tools have always matched these values for the LX760, the data sheet is now correct. Updated the notes for $T_{OUTJITTER}$ in Table 64.
01/12/12	3.4	Added the temperature range -2E to Note 5 in Table 4.