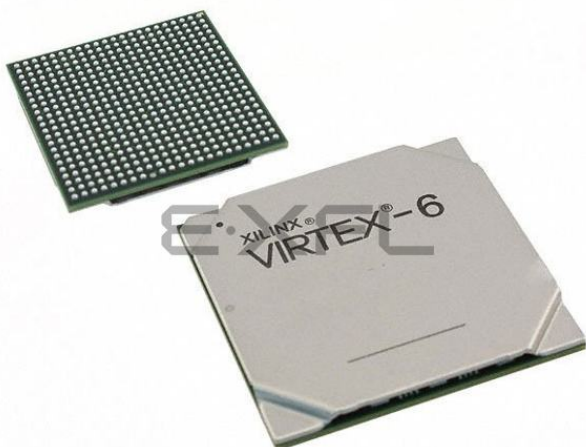




Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	28440
Number of Logic Elements/Cells	364032
Total RAM Bits	15335424
Number of I/O	720
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1759-BBGA, FCBGA
Supplier Device Package	1759-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vlx365t-2ffg1759i

Figure 4 shows the timing parameters in Table 27.

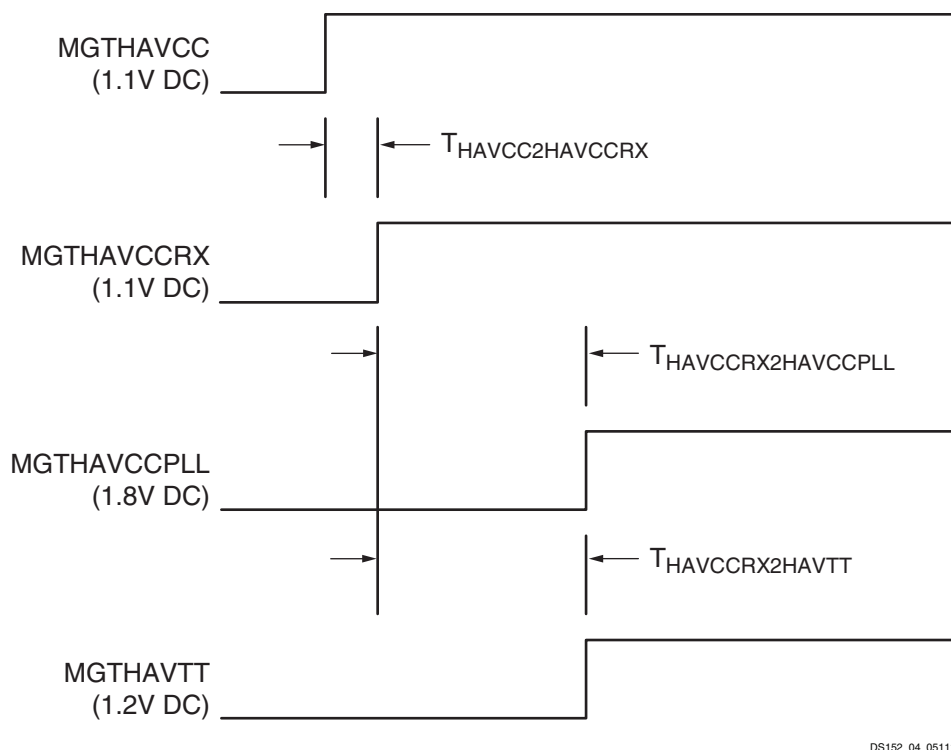


Figure 4: GTH Transceiver Power Supply Power-On Sequencing

Table 28: GTH Transceiver Supply Current

Symbol	Description	Typ ⁽¹⁾	Max	Units
$I_{MGTHAVCC}$	MGTHAVCC supply current for one GTH Quad (4 lanes)	571	Note 2	mA
$I_{MGTHAVCCR X}$	MGTHAVCCR X supply current for a GTH Quad (4 lanes)	254	Note 2	mA
$I_{MGTHAVTT}$	MGTHAVTT supply current for one GTH Quad (4 lanes)	93	Note 2	mA
$I_{MGTHAVCCPLL}$	MGTHAVCCPLL supply current for one GTH Quad (4 lanes)	219	Note 2	mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	1000.0 ± 1% tolerance		Ω

Notes:

- Typical values are specified at nominal voltage, 25°C, with a 10.3125 Gb/s line rate.
- Values for currents other than the values specified in this table can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

Table 29: GTH Transceiver Quiescent Supply Current⁽¹⁾⁽²⁾

Symbol	Description	Typ ⁽³⁾	Max	Units
$I_{MGTHAVCCQ}$	Quiescent MGTHAVCC Supply Current for one GTH Quad (4 lanes)	65	Note 4	mA
$I_{MGTHAVCCR XQ}$	Quiescent MGTHAVCCR X Supply Current for one GTH Quad (4 lanes)	17	Note 4	mA
$I_{MGTHAVTTQ}$	Quiescent MGTHAVTT Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA
$I_{MGTHAVCCPLLQ}$	Quiescent MGTHAVCCPLL Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA

Notes:

- Device powered and unconfigured.
- GTH transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTH transceivers.
- Typical values are specified at nominal voltage, 25°C.
- Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.

Table 35: GTH Transceiver User Clock Switching Characteristics ⁽¹⁾

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F _{TXOUT}	TXUSERCLKOUT maximum frequency		350	350	323	MHz
F _{RXOUT}	RXUSERCLKOUT maximum frequency		350	350	323	MHz
F _{TXIN}	TXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz
F _{RXIN}	RXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz

Notes:

1. Clocking must be implemented as described in [UG371](#): Virtex-6 FPGA GTH Transceivers User Guide.

Table 36: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
T _{RTX}	TX Rise time	20%–80%	–	50 ⁽³⁾	–	ps
T _{FTX}	TX Fall time	80%–20%	–	50 ⁽³⁾	–	ps
T _{LLSKEW}	TX lane-to-lane skew	within one GTH Quad	–	–	300	ps
Transmitter Output Jitter⁽¹⁾⁽²⁾						
TJ _{11.18}	Total Jitter	11.181 Gb/s	–	–	0.280	UI
DJ _{11.18}	Deterministic Jitter		–	–	0.170	UI
TJ _{10.3125}	Total Jitter	10.3125 Gb/s	–	–	0.280	UI
DJ _{10.3125}	Deterministic Jitter		–	–	0.170	UI
TJ _{9.953}	Total Jitter	9.953 Gb/s	–	–	0.280	UI
DJ _{9.953}	Deterministic Jitter		–	–	0.170	UI
TJ _{2.667}	Total Jitter	2.667 Gb/s	–	–	0.110	UI
DJ _{2.667}	Deterministic Jitter		–	–	0.060	UI
TJ _{2.488}	Total Jitter	2.488 Gb/s	–	–	0.110	UI
DJ _{2.488}	Deterministic Jitter		–	–	0.060	UI

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit-error ratio of 1e⁻¹².
3. Rise and fall times are specified at the transmitter package balls.

Table 37: GTH Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
R _{XRL}	Run length (CID)		8000	–	–	UI
R _{XPPMTOL}	Data/REFCLK PPM offset tolerance		–200	–	200	ppm
SJ Jitter Tolerance ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾						
JT_SJ _{11.18}	Sinusoidal Jitter	11.18 Gb/s	0.3	–	–	UI
JT_SJ _{10.32}	Sinusoidal Jitter	10.32 Gb/s	0.3	–	–	UI
JT_SJ _{9.95}	Sinusoidal Jitter	9.95 Gb/s	0.3	–	–	UI
JT_SJ _{2.667}	Sinusoidal Jitter	2.667 Gb/s	0.5	–	–	UI
JT_SJ _{2.48}	Sinusoidal Jitter	2.48 Gb/s	0.5	–	–	UI

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. High-frequency jitter tolerance including 6 db of channel loss at a high frequency of the data rate divided by two.

Ethernet MAC Switching Characteristics

Consult [UG368: Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide](#) for further information.

Table 38: Maximum Ethernet MAC Performance

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1	-1L	
F _{TEMACCLIENT}	Client interface maximum frequency	10 Mb/s – 8-bit width	2.5 ⁽¹⁾	2.5 ⁽¹⁾	2.5 ⁽¹⁾	2.5 ⁽¹⁾	MHz
		100 Mb/s – 8-bit width	25 ⁽²⁾	25 ⁽²⁾	25 ⁽²⁾	25 ⁽²⁾	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		1000 Mb/s – 16-bit width	62.5	62.5	62.5	62.5	MHz
		2000 Mb/s – 16-bit width	125	125	125	N/A	MHz
		2500 Mb/s – 16-bit width	156.25	156.25	156.25	N/A	MHz
F _{TEMACPHY}	Physical interface maximum frequency	10 Mb/s – 4-bit width	2.5	2.5	2.5	2.5	MHz
		100 Mb/s – 4-bit width	25	25	25	25	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		2000 Mb/s – 8-bit width	250	250	250	N/A	MHz
		2500 Mb/s – 8-bit width	312.5	312.5	312.5	N/A	MHz

Notes:

1. When not using clock enable, the F_{MAX} is lowered to 1.25 MHz.
2. When not using clock enable, the F_{MAX} is lowered to 12.5 MHz.

IOB Pad Input/Output/3-State Switching Characteristics

Table 44 (for commercial (XC) Virtex-6 devices) and **Table 45** (for the Defense-grade (XQ) Virtex-6 devices) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 46 summarizes the value of T_{IOTPHZ} . T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDS_25	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
LVDSEXT_25	0.85	0.94	1.09	1.08	1.53	1.65	1.84	1.73	1.53	1.65	1.84	1.73	ns
HT_25	0.85	0.94	1.09	1.08	1.51	1.62	1.78	1.69	1.51	1.62	1.78	1.69	ns
BLVDS_25	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.65	1.39	1.50	1.67	1.65	ns
RSDS_25 (point to point)	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
HSTL_I	0.81	0.91	1.06	1.06	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns
HSTL_II	0.81	0.91	1.06	1.06	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
HSTL_III	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
HSTL_I_18	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
HSTL_II_18	0.81	0.91	1.06	1.06	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
HSTL_III_18	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
SSTL2_I	0.81	0.91	1.06	1.06	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
SSTL2_II	0.81	0.91	1.06	1.06	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
LVC MOS25, Slow, 2 mA	0.51	0.57	0.66	0.70	5.09	5.46	6.01	5.63	5.09	5.46	6.01	5.63	ns
LVC MOS25, Slow, 4 mA	0.51	0.57	0.66	0.70	3.30	3.49	3.79	3.65	3.30	3.49	3.79	3.65	ns
LVC MOS25, Slow, 6 mA	0.51	0.57	0.66	0.70	2.62	2.81	3.08	2.95	2.62	2.81	3.08	2.95	ns
LVC MOS25, Slow, 8 mA	0.51	0.57	0.66	0.70	2.21	2.41	2.72	2.59	2.21	2.41	2.72	2.59	ns
LVC MOS25, Slow, 12 mA	0.51	0.57	0.66	0.70	1.80	1.95	2.17	2.10	1.80	1.95	2.17	2.10	ns
LVC MOS25, Slow, 16 mA	0.51	0.57	0.66	0.70	1.89	2.05	2.29	2.21	1.89	2.05	2.29	2.21	ns
LVC MOS25, Slow, 24 mA	0.51	0.57	0.66	0.70	1.68	1.82	2.02	1.98	1.68	1.82	2.02	1.98	ns
LVC MOS25, Fast, 2 mA	0.51	0.57	0.66	0.70	5.12	5.49	6.04	5.62	5.12	5.49	6.04	5.62	ns
LVC MOS25, Fast, 4 mA	0.51	0.57	0.66	0.70	3.28	3.50	3.82	3.65	3.28	3.50	3.82	3.65	ns
LVC MOS25, Fast, 6 mA	0.51	0.57	0.66	0.70	2.56	2.73	2.99	2.88	2.56	2.73	2.99	2.88	ns
LVC MOS25, Fast, 8 mA	0.51	0.57	0.66	0.70	2.11	2.33	2.65	2.53	2.11	2.33	2.65	2.53	ns
LVC MOS25, Fast, 12 mA	0.51	0.57	0.66	0.70	1.74	1.88	2.08	2.03	1.74	1.88	2.08	2.03	ns
LVC MOS25, Fast, 16 mA	0.51	0.57	0.66	0.70	1.77	1.92	2.13	2.08	1.77	1.92	2.13	2.08	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVC MOS25, Fast, 16 mA	0.57	0.66	0.70	1.92	2.15	2.08	1.92	2.15	2.08	ns
LVC MOS25, Fast, 24 mA	0.57	0.66	0.70	1.79	2.15	1.96	1.79	2.15	1.96	ns
LVC MOS18, Slow, 2 mA	0.61	0.71	0.73	4.47	4.87	4.30	4.47	4.87	4.30	ns
LVC MOS18, Slow, 4 mA	0.61	0.71	0.73	2.96	3.21	2.94	2.96	3.21	2.94	ns
LVC MOS18, Slow, 6 mA	0.61	0.71	0.73	2.43	2.64	2.47	2.43	2.64	2.47	ns
LVC MOS18, Slow, 8 mA	0.61	0.71	0.73	2.11	2.41	2.24	2.11	2.41	2.24	ns
LVC MOS18, Slow, 12 mA	0.61	0.71	0.73	1.99	2.30	2.10	1.99	2.30	2.10	ns
LVC MOS18, Slow, 16 mA	0.61	0.71	0.73	1.95	2.30	2.04	1.95	2.30	2.04	ns
LVC MOS18, Fast, 2 mA	0.61	0.71	0.73	4.23	4.57	4.08	4.23	4.57	4.08	ns
LVC MOS18, Fast, 4 mA	0.61	0.71	0.73	2.76	2.97	2.74	2.76	2.97	2.74	ns
LVC MOS18, Fast, 6 mA	0.61	0.71	0.73	2.28	2.46	2.32	2.28	2.46	2.32	ns
LVC MOS18, Fast, 8 mA	0.61	0.71	0.73	1.99	2.34	2.14	1.99	2.34	2.14	ns
LVC MOS18, Fast, 12 mA	0.61	0.71	0.73	1.80	2.19	1.88	1.80	2.19	1.88	ns
LVC MOS18, Fast, 16 mA	0.61	0.71	0.73	1.74	2.18	1.88	1.74	2.18	1.88	ns
LVC MOS15, Slow, 2 mA	0.73	0.85	0.85	3.77	4.29	3.91	3.77	4.29	3.91	ns
LVC MOS15, Slow, 4 mA	0.73	0.85	0.85	2.79	3.10	2.93	2.79	3.10	2.93	ns
LVC MOS15, Slow, 6 mA	0.73	0.85	0.85	2.32	2.68	2.50	2.32	2.68	2.50	ns
LVC MOS15, Slow, 8 mA	0.73	0.85	0.85	1.98	2.29	2.24	1.98	2.29	2.24	ns
LVC MOS15, Slow, 12 mA	0.73	0.85	0.85	1.91	2.23	2.07	1.91	2.23	2.07	ns
LVC MOS15, Slow, 16 mA	0.73	0.85	0.85	1.83	2.23	1.98	1.83	2.23	1.98	ns
LVC MOS15, Fast, 2 mA	0.73	0.85	0.85	3.77	4.28	3.91	3.77	4.28	3.91	ns
LVC MOS15, Fast, 4 mA	0.73	0.85	0.85	2.53	2.78	2.66	2.53	2.78	2.66	ns
LVC MOS15, Fast, 6 mA	0.73	0.85	0.85	2.05	2.42	2.16	2.05	2.42	2.16	ns
LVC MOS15, Fast, 8 mA	0.73	0.85	0.85	1.90	2.20	2.04	1.90	2.20	2.04	ns
LVC MOS15, Fast, 12 mA	0.73	0.85	0.85	1.77	2.11	1.90	1.77	2.11	1.90	ns
LVC MOS15, Fast, 16 mA	0.73	0.85	0.85	1.76	2.11	1.92	1.76	2.11	1.92	ns
LVC MOS12, Slow, 2 mA	0.81	0.93	0.95	3.39	3.75	3.54	3.39	3.75	3.54	ns
LVC MOS12, Slow, 4 mA	0.81	0.93	0.95	2.63	2.93	2.79	2.63	2.93	2.79	ns
LVC MOS12, Slow, 6 mA	0.81	0.93	0.95	2.11	2.67	2.26	2.11	2.67	2.26	ns
LVC MOS12, Slow, 8 mA	0.81	0.93	0.95	2.02	2.25	2.17	2.02	2.25	2.17	ns
LVC MOS12, Fast, 2 mA	0.81	0.93	0.95	2.98	3.39	3.11	2.98	3.39	3.11	ns
LVC MOS12, Fast, 4 mA	0.81	0.93	0.95	2.16	2.70	2.31	2.16	2.70	2.31	ns
LVC MOS12, Fast, 6 mA	0.81	0.93	0.95	1.89	2.34	2.05	1.89	2.34	2.05	ns
LVC MOS12, Fast, 8 mA	0.81	0.93	0.95	1.82	2.10	1.98	1.82	2.10	1.98	ns
LVDCI_25	0.57	0.70	0.70	2.14	2.82	2.26	2.14	2.82	2.26	ns
LVDCI_18	0.61	0.71	0.73	2.23	2.78	2.38	2.23	2.78	2.38	ns
LVDCI_15	0.73	0.85	0.85	2.01	2.75	2.18	2.01	2.75	2.18	ns
LVDCI_DV2_25	0.57	0.70	0.70	1.83	2.37	2.00	1.83	2.37	2.00	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPi}			T _{IOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
DIFF_SSTL18_II	0.94	1.09	1.08	1.50	2.27	1.66	1.50	2.27	1.66	ns
DIFF_SSTL18_II_DCI	0.94	1.09	1.08	1.47	2.20	1.62	1.47	2.20	1.62	ns
DIFF_SSTL18_II_T_DCI	0.94	1.09	1.08	1.51	2.30	1.65	1.51	2.30	1.65	ns
DIFF_SSTL15	0.91	1.06	1.06	1.54	2.25	1.69	1.54	2.25	1.69	ns
DIFF_SSTL15_DCI	0.91	1.06	1.06	1.52	2.25	1.66	1.52	2.25	1.66	ns
DIFF_SSTL15_T_DCI	0.91	1.06	1.06	1.52	2.25	1.66	1.52	2.25	1.66	ns

Table 46: IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T _{IOTPHZ}	T input to Pad high-impedance	0.86	0.92	0.99	0.99	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 47 shows the test setup parameters used for measuring input delay.

Table 47: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)(2)}$	$V_H^{(1)(2)}$	$V_{MEAS}^{(1)(4)(5)}$	$V_{REF}^{(1)(3)(5)}$
LVC MOS, 2.5V	LVC MOS25	0	2.5	1.25	—
LVC MOS, 1.8V	LVC MOS18	0	1.8	0.9	—
LVC MOS, 1.5V	LVC MOS15	0	1.5	0.75	—
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL, Class III	HSTL_III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	$V_{REF} - 1.00$	$V_{REF} + 1.00$	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	$1.2 - 0.125$	$1.2 + 0.125$	$0^{(6)}$	—
LVDS EXT (LVDS Extended Mode), 2.5V	LVDS EXT_25	$1.2 - 0.125$	$1.2 + 0.125$	$0^{(6)}$	—
HT (HyperTransport), 2.5V	LDT_25	$0.6 - 0.125$	$0.6 + 0.125$	$0^{(6)}$	—

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVC MOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H .
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 6.
6. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 6 and Figure 7.

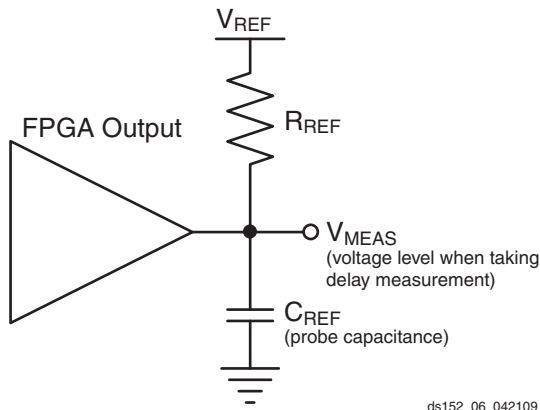
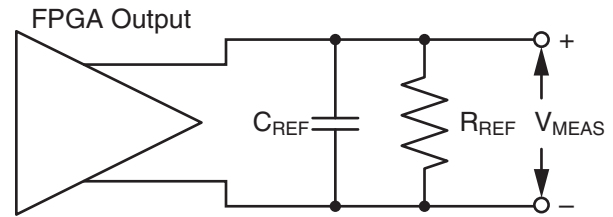


Figure 6: Single Ended Test Setup



ds152_07_042109

Figure 7: Differential Test Setup

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 48.
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 48: Output Delay Measurement Methodology

Description	I/O Standard Attribute	R_{REF} (Ω)	$C_{REF}^{(1)}$ (pF)	V_{MEAS} (V)	V_{REF} (V)
LVC MOS, 2.5V	LVC MOS25	1M	0	1.25	0
LVC MOS, 1.8V	LVC MOS18	1M	0	0.9	0
LVC MOS, 1.5V	LVC MOS15	1M	0	0.75	0
LVC MOS, 1.2V	LVC MOS12	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	100	0	0 ⁽²⁾	1.2
LVDS EXT (LVDS Extended Mode), 2.5V	LVDS_25	100	0	0 ⁽²⁾	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0 ⁽²⁾	0

Table 48: Output Delay Measurement Methodology (Cont'd)

Description	I/O Standard Attribute	R _{REF} (Ω)	C _{REF} ⁽¹⁾ (pF)	V _{MEAS} (V)	V _{REF} (V)
HT (HyperTransport), 2.5V	LDT_25	100	0	0 ⁽²⁾	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	100	0	0 ⁽²⁾	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V _{REF}	0.75
HSTL, Class III, with DCI	HSTL_III_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V _{REF}	0.9
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termination Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V _{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V _{REF}	1.25

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 49: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Setup/Hold						
T _{ICE1CK} /T _{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.21/ 0.03	0.25/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T _{ISRCK} /T _{ICKSR}	SR pin Setup/Hold with respect to CLK	0.66/ −0.08	0.78/ −0.08	0.96/ −0.08	1.09/ −0.11	ns
T _{IDOCK} /T _{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.07/ 0.41	0.08/ 0.46	0.10/ 0.54	0.11/ 0.64	ns
T _{IDOCKD} /T _{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.10/ 0.32	0.12/ 0.36	0.14/ 0.42	0.16/ 0.50	ns
Combinatorial						
T _{IDI}	D pin to O pin propagation delay, no Delay	0.15	0.17	0.20	0.23	ns
T _{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.19	0.22	0.25	0.28	ns
Sequential Delays						
T _{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.48	0.54	0.64	0.73	ns
T _{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.52	0.58	0.68	0.78	ns
T _{ICKQ}	CLK to Q outputs	0.54	0.61	0.70	0.93	ns
T _{RQ_ILOGIC}	SR pin to OQ/TQ out	0.85	0.97	1.15	1.32	ns
T _{GSRQ_ILOGIC}	Global Set/Reset to Q outputs	7.60	7.60	10.51	10.51	ns
Set/Reset						
T _{RPW_ILOGIC}	Minimum Pulse Width, SR inputs	0.78	0.95	1.20	1.30	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 51: ISERDES Switching Characteristics

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup/Hold for Control Lines							
T _{ISCKK_BITSIP} / T _{ISCKC_BITSIP}	BITSLIP pin Setup/Hold with respect to CLKDIV	0.07/ 0.15	0.08/ 0.16	0.09/ 0.17	0.09/ 0.17	0.14/ 0.17	ns
T _{ISCKK_CE} / T _{ISCKC_CE} ⁽²⁾	CE pin Setup/Hold with respect to CLK (for CE1)	0.20/ 0.03	0.25/ 0.04	0.27/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T _{ISCKK_CE2} / T _{ISCKC_CE2} ⁽²⁾	CE pin Setup/Hold with respect to CLKDIV (for CE2)	0.01/ 0.27	0.01 0.29	0.01/ 0.31	0.01/ 0.31	−0.05/ 0.35	ns
Setup/Hold for Data Lines							
T _{ISDCK_D} / T _{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.07/ 0.08	0.08/ 0.09	0.09/ 0.11	0.09/ 0.11	0.11/ 0.19	ns
T _{ISDCK_DDLY} / T _{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY) ⁽¹⁾	0.10/ 0.05	0.12/ 0.06	0.14/ 0.07	0.14/ 0.07	0.16/ 0.15	ns
T _{ISDCK_D_DDR} / T _{ISCKD_D_DDR}	D pin Setup/Hold with respect to CLK at DDR mode	0.07/ 0.08	0.08/ 0.09	0.09/ 0.11	0.09/ 0.11	0.11/ 0.19	ns
T _{ISDCK_DDLY_DDR} / T _{ISCKD_DDLY_DDR}	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY) ⁽¹⁾	0.10/ 0.05	0.12/ 0.06	0.14/ 0.07	0.14/ 0.07	0.16/ 0.15	ns
Sequential Delays							
T _{ISCKO_Q}	CLKDIV to out at Q pin	0.57	0.66	0.75	0.80	0.88	ns
Propagation Delays							
T _{ISDO_DO}	D input to DO output pin	0.19	0.22	0.25	0.25	0.28	ns

Notes:

- Recorded at 0 tap value.
- T_{ISCK_CE2} and T_{ISCK_CE2} are reported as $T_{ISCK_CE} / T_{ISCK_CE}$ in TRACE report.

Input/Output Delay Switching Characteristics

Table 53: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
IDELAYCTRL						
T _{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3.00	3.00	3.00	3.25	μs
F _{IDELAYCTRL_REF}	REFCLK frequency = 200.0 ⁽¹⁾	200	200	200	200	MHz
	REFCLK frequency = 300.0 ⁽¹⁾	300	300	–	–	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
T _{IDELAYCTRL_RPW}	Minimum Reset pulse width	50.00	50.00	50.00	52.50	ns
IODELAY						
T _{IDELAYRESOLUTION}	IODELAY Chain Delay Resolution	1/(32 x 2 x F _{REF})				ps
T _{IDELAYPAT_JIT}	Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾	0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). ⁽³⁾	±5	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). ⁽⁴⁾	±9	±9	±9	±9	ps per tap
T _{IODELAY_CLK_MAX}	Maximum frequency of CLK input to IDELAY	500.00	420.00	300.00	300.00	MHz
T _{IODCCK_CE} / T _{IODCKC_CE}	CE pin Setup/Hold with respect to CK	0.45/ –0.09	0.53/ –0.09	0.65/ –0.09	0.84/ –0.14	ns
T _{IODCK_INC} / T _{IODCKC_INC}	INC pin Setup/Hold with respect to CK	0.23/ –0.02	0.27/ –0.01	0.31/ 0.00	0.27/ –0.04	ns
T _{IODCCK_RST} / T _{IODCKC_RST}	RST pin Setup/Hold with respect to CK	0.57/ –0.08	0.62/ –0.08	0.69/ –0.08	0.74/ –0.13	ns
T _{IODDO_T}	TSCONTROL delay to MUXE/MUXF switching and through IDELAY	Note 5	Note 5	Note 5	Note 5	ps
T _{IODDO_IDATAIN}	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	ps
T _{IODDO_ODATAIN}	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See TRACE report for actual values.

CLB Switching Characteristics

Table 54: CLB Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Combinatorial Delays						
T _{ILO}	An – Dn LUT address to A	0.06	0.07	0.07	0.09	ns, Max
	An – Dn LUT address to AMUX/CMUX	0.18	0.20	0.22	0.25	ns, Max
	An – Dn LUT address to BMUX_A	0.28	0.31	0.36	0.40	ns, Max

Table 54: CLB Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T _{ITO}	An – Dn inputs to A – D Q outputs	0.59	0.67	0.79	0.85	ns, Max
T _{AXA}	AX inputs to AMUX output	0.31	0.35	0.42	0.44	ns, Max
T _{AXB}	AX inputs to BMUX output	0.35	0.39	0.47	0.50	ns, Max
T _{AXC}	AX inputs to CMUX output	0.39	0.44	0.52	0.56	ns, Max
T _{AXD}	AX inputs to DMUX output	0.42	0.47	0.55	0.60	ns, Max
T _{BXB}	BX inputs to BMUX output	0.30	0.34	0.39	0.44	ns, Max
T _{BXD}	BX inputs to DMUX output	0.38	0.43	0.50	0.55	ns, Max
T _{CXC}	CX inputs to CMUX output	0.26	0.29	0.34	0.37	ns, Max
T _{CXD}	CX inputs to DMUX output	0.30	0.34	0.40	0.44	ns, Max
T _{DXD}	DX inputs to DMUX output	0.30	0.33	0.38	0.43	ns, Max
T _{OPCYA}	An input to COUT output	0.32	0.36	0.41	0.47	ns, Max
T _{OPCYB}	Bn input to COUT output	0.32	0.36	0.41	0.47	ns, Max
T _{OPCYC}	Cn input to COUT output	0.27	0.30	0.34	0.40	ns, Max
T _{OPCYD}	Dn input to COUT output	0.25	0.28	0.32	0.37	ns, Max
T _{AXCY}	AX input to COUT output	0.25	0.28	0.33	0.36	ns, Max
T _{BXCY}	BX input to COUT output	0.22	0.24	0.28	0.31	ns, Max
T _{CXCY}	CX input to COUT output	0.15	0.17	0.20	0.22	ns, Max
T _{DXCY}	DX input to COUT output	0.14	0.16	0.19	0.21	ns, Max
T _{BYP}	CIN input to COUT output	0.06	0.07	0.08	0.09	ns, Max
T _{CINA}	CIN input to AMUX output	0.21	0.24	0.28	0.30	ns, Max
T _{CINB}	CIN input to BMUX output	0.23	0.25	0.29	0.31	ns, Max
T _{CINC}	CIN input to CMUX output	0.23	0.26	0.30	0.33	ns, Max
T _{CIND}	CIN input to DMUX output	0.25	0.29	0.33	0.36	ns, Max
Sequential Delays						
T _{CKO}	Clock to AQ – DQ outputs	0.29	0.33	0.39	0.44	ns, Max
T _{SHCKO}	Clock to AMUX – DMUX outputs	0.36	0.40	0.47	0.53	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T _{DICK} /T _{CKDI}	A – D input to CLK on A – D Flip Flops	0.30/0.17	0.36/0.18	0.43/0.20	0.44/0.25	ns, Min
T _{CECK_CLB} / T _{CKCE_CLB}	CE input to CLK on A – D Flip Flops	0.20/0.00	0.25/0.00	0.32/0.00	0.32/0.01	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D Flip Flops	0.39/–0.07	0.44/–0.07	0.52/–0.07	0.58/–0.08	ns, Min
T _{CINCK} /T _{CKCIN}	CIN input to CLK on A – D Flip Flops	0.16/0.12	0.19/0.14	0.24/0.16	0.23/0.22	ns, Min
Set/Reset						
T _{SRMIN}	SR input minimum pulse width	0.90	0.90	0.97	0.80	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops	0.52	0.58	0.68	0.77	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops	0.41	0.48	0.59	0.61	ns, Max
F _{TOG}	Toggle frequency (for export control)	1412.00	1286.40	1098.00	1098.00	MHz

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

Table 57: Block RAM and FIFO Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{RCKK_WE}/T_{RCKC_WE}	Write Enable (WE) input (Block RAM only)	0.44/ 0.19	0.47/ 0.25	0.52/ 0.35	0.67/ 0.24	ns, Min
$T_{RCKK_WREN}/T_{RCKC_WREN}$	WREN FIFO inputs	0.47/ 0.26	0.50/ 0.27	0.55/ 0.30	0.68/ 0.31	ns, Min
$T_{RCKK_RDEN}/T_{RCKC_RDEN}$	RDEN FIFO inputs	0.46/ 0.26	0.50/ 0.27	0.55/ 0.30	0.67/ 0.31	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers ⁽¹⁰⁾	0.90	0.98	1.10	1.23	ns, Max
$T_{RCKK_RSTREG}/T_{RCKC_RSTREG}$	FIFO reset timing ⁽¹¹⁾	0.22/ 0.23	0.24/ 0.24	0.28/ 0.26	0.31/ 0.27	ns, Min
Maximum Frequency						
F_{MAX}	Block RAM in TDP and SDP modes (Write First and No Change modes)	600	540	450	340	MHz
	Block RAM (Read First mode)	525	475	400	275	MHz
	Block RAM (SDP mode) ⁽¹²⁾	525	475	400	275	MHz
$F_{MAX_CASCADE}$	Block RAM Cascade (Write First and No Change modes)	550	490	400	300	MHz
	Block RAM Cascade (Read First mode)	475	425	350	235	MHz
F_{MAX_FIFO}	FIFO in all modes	600	540	450	340	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	450	400	325	250	MHz

Notes:

- TRACE will report all of these parameters as T_{RCKO_DO} .
- T_{RCKO_DOR} includes T_{RCKO_DOW} , T_{RCKO_DOPR} , and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
- These parameters also apply to synchronous FIFO with $DO_REG = 0$.
- T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
- These parameters also apply to multirate (asynchronous) and synchronous FIFO with $DO_REG = 1$.
- T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY} , T_{RCKO_AFULL} , T_{RCKO_EMPTY} , T_{RCKO_FULL} , T_{RCKO_RDERR} , T_{RCKO_WRERR} .
- $T_{RCKO_POINTERS}$ includes both $T_{RCKO_RDCOUNT}$ and $T_{RCKO_WRCOUNT}$.
- The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
- T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
- T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
- The FIFO reset must be asserted for at least three positive clock edges.
- When using ISE software v12.4 or later, if the RDADDR_COLLISION_HWCONFIG attribute is set to PERFORMANCE or the block RAM is in single-port operation, then the faster F_{MAX} for WRITE_FIRST/NO_CHANGE modes apply.

Table 58: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
$T_{DSPDO_PCIN, CARRYCASCIN, MULTSIGNIN_PCOUT, CARRYCASCOUT, MULTSIGNOUT}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.28	1.46	1.72	1.72	2.06	ns
Clock to Outs from Output Register Clock to Output Pins							
$T_{DSPCKO_P, CARRYOUT_PREG}$	CLK (PREG) to {P, CARRYOUT} output	0.38	0.43	0.50	0.50	0.57	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_PREG}$	CLK (PREG) to {CARRYCASCOUT, PCOUT, MULTSIGNOUT} output	0.50	0.56	0.66	0.66	0.76	ns
Clock to Outs from Pipeline Register Clock to Output Pins							
$T_{DSPCKO_P, CARRYOUT_MREG}$	CLK (MREG) to {P, CARRYOUT} output	1.72	1.96	2.30	2.30	2.69	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_MREG}$	CLK (MREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.81	2.06	2.43	2.43	2.88	ns
$T_{DSPCKO_P, CARRYOUT_ADREG_MULT}$	CLK (ADREG) to {P, CARRYOUT} output	2.79	3.16	3.72	3.72	4.32	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_ADREG_MULT}$	CLK (ADREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.87	3.26	3.84	3.84	4.51	ns
Clock to Outs from Input Register Clock to Output Pins							
$T_{DSPCKO_P, CARRYOUT_AREG, BREG_MULT}$	CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier	3.97	4.52	5.36	5.36	6.20	ns
$T_{DSPCKO_P, CARRYOUT_AREG, BREG}$	CLK (AREG, BREG) to {P, CARRYOUT} output not using multiplier	1.70	1.93	2.27	2.27	2.65	ns
$T_{DSPCKO_P, CARRYOUT_CREG}$	CLK (CREG) to {P, CARRYOUT} output	1.70	1.93	2.27	2.27	2.80	ns
$T_{DSPCKO_P, CARRYOUT_DREG_MULT}$	CLK (DREG) to {P, CARRYOUT} output	3.89	4.44	5.25	5.25	6.07	ns
Clock to Outs from Input Register Clock to Cascading Output Pins							
$T_{DSPCKO_ACOUT, BCOUT_AREG, BREG}$	CLK (AREG, BREG) to {P, CARRYOUT} output	0.66	0.76	0.89	0.89	1.01	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_AREG, BREG_MULT}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	4.05	4.63	5.49	5.49	6.39	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_AREG, BREG}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.79	2.03	2.40	2.40	2.84	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_DREG_MULT}$	CLK (DREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.98	4.54	5.38	5.38	6.26	ns
$T_{DSPCKO_PCOUT, CARRYCASCOUT, MULTSIGNOUT_CREG}$	CLK (CREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.78	2.03	2.40	2.40	2.99	ns

Table 58: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Maximum Frequency							
F _{MAX}	With all registers used	600	540	450	450	410	MHz
F _{MAX_PATDET}	With pattern detector	551	483	408	408	356	MHz
F _{MAX_MULT_NOMREG}	Two register multiply without MREG	356	311	262	262	224	MHz
F _{MAX_MULT_NOMREG_PATDET}	Two register multiply without MREG with pattern detect	327	286	241	241	211	MHz
F _{MAX_PREADD_MULT_NOADREG}	Without ADREG	398	347	292	292	254	MHz
F _{MAX_PREADD_MULT_NOADREG_PATDET}	Without ADREG with pattern detect	398	347	292	292	254	MHz
F _{MAX_NOPIPELINEREG}	Without pipeline registers (MREG, ADREG)	266	233	196	196	171	MHz
F _{MAX_NOPIPELINEREG_PATDET}	Without pipeline registers (MREG, ADREG) with pattern detect	250	219	184	184	160	MHz

Configuration Switching Characteristics

Table 59: Configuration Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Power-up Timing Characteristics						
T _{PL} ⁽¹⁾	Program Latency	5	5	5	5	ms, Max
T _{POR} ⁽¹⁾	Power-on-Reset	15/55	15/55	15/55	15/60	ms, Min/Max
T _{ICCK}	CCLK (output) delay	400	400	400	400	ns, Min
T _{PROGRAM}	Program Pulse Width	250	250	250	250	ns, Min
Master/Slave Serial Mode Programming Switching						
T _{DCCK} /T _{CCKD}	DIN Setup/Hold, slave mode	4.0/0.0	4.0/0.0	4.0/0.0	4.5/0.0	ns, Min
T _{DSCCK} /T _{SCCKD}	DIN Setup/Hold, master mode	4.0/0.0	4.0/0.0	4.0/0.0	5.0/0.0	ns, Min
T _{CCO}	DOUT at 2.5V	6	6	6	7	ns, Max
	DOUT at 1.8V	6	6	6	7	ns, Max
F _{MCCK}	Maximum CCLK frequency, serial modes	105	105	105	70	MHz, Max
F _{MCCKTOL}	Frequency Tolerance, master mode with respect to nominal CCLK.	55	55	55	60	%
F _{MSCCK}	Slave mode external CCLK	100	100	100	100	MHz
SelectMAP Mode Programming Switching						
T _{SMDCK} /T _{SMCKD}	SelectMAP Data Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	5.5/0.0	ns, Min
T _{SMCSCCK} /T _{SMCKCS}	CSI_B Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	5.5/0.0	ns, Min
T _{SMCKW} /T _{SMWCK}	RDWR_B Setup/Hold	10.0/0.0	10.0/0.0	10.0/0.0	16.0/0.0	ns, Min
T _{SMCKCSO}	CSO_B clock to out (330 Ω pull-up resistor required)	6	6	6	7	ns, Max
T _{SMCO}	CCLK to DATA out in readback at 2.5V	6	6	6	7	ns, Max
	CCLK to DATA out in readback at 1.8V	6	6	6	7	ns, Max

Table 64: MMCM Specification (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
RST _{MINPULSE}	Minimum Reset Pulse Width	1.5	1.5	1.5	1.5	ns
F _{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized ⁽⁹⁾	550	500	450	450	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300	300	300	300	MHz
F _{PFDMIN}	Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	135	135	135	135	MHz
	Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	10	10	10	10	MHz
T _{FBDELAY}	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				
T _{MMCMCK_PSEN} / T _{MMCMCKD_PSEN}	Setup and Hold of Phase Shift Enable	1.04 0.00	1.04 0.00	1.04 0.00	1.04 0.00	ns
T _{MMCMCK_PINCDEC} / T _{MMCMCKD_PINCDEC}	Setup and Hold of Phase Shift Increment/Decrement	1.04 0.00	1.04 0.00	1.04 0.00	1.04 0.00	ns
T _{MMCMCKO_PSDONE}	Phase Shift Clock-to-Out of PSDONE	0.32	0.34	0.38	0.38	ns

Notes:

1. When DIVCLK_DIVIDE = 3 or 4, F_{INMAX} is 315 MHz.
2. This duty cycle specification does not apply to the GTH_QUAD (GTH) to MMCM connection. The GTH transceivers drive the MMCMs at the following maximum frequencies: 323 MHz for -1 speed grade devices, 350 MHz for -2 speed grade devices, or 350 MHz for -3 speed grade devices.
3. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. The static offset is measured between any MMCM outputs with identical phase.
5. Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
6. Includes global clock buffer.
7. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
8. When CASCADE4_OUT = TRUE, F_{OUTMIN} is 0.036 MHz.
9. In ISE software 12.3 (or earlier versions supporting the Virtex-6 family), the phase frequency detector Optimized bandwidth setting is equivalent to the High bandwidth setting. Starting with ISE software 12.4, the Optimized bandwidth setting is automatically adjusted to Low when the software can determine that the phase frequency detector input is less than 135 MHz.

Table 69: Global Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T _{PSMMCMGC} / T _{PHMMCMGC}	No Delay Global Clock Input and IFF(2) with MMCM	XC6VLX75T	1.45/ −0.18	1.57/ −0.18	1.72/ −0.18	1.78/ −0.08	ns
		XC6VLX130T	1.53/ −0.18	1.65/ −0.18	1.81/ −0.18	1.87/ −0.07	ns
		XC6VLX195T	1.54/ −0.17	1.66/ −0.17	1.82/ −0.17	1.87/ −0.08	ns
		XC6VLX240T	1.54/ −0.17	1.66/ −0.17	1.82/ −0.17	1.87/ −0.08	ns
		XC6VLX365T	1.55/ −0.18	1.67/ −0.18	1.83/ −0.18	1.87/ −0.07	ns
		XC6VLX550T	N/A	1.84/ −0.17	2.02/ −0.17	2.06/ −0.06	ns
		XC6VLX760	N/A	2.26/ −0.13	2.49/ −0.13	2.06/ −0.03	ns
		XC6VSX315T	1.56/ −0.18	1.68/ −0.18	1.84/ −0.18	1.89/ −0.08	ns
		XC6VSX475T	N/A	1.85/ −0.23	2.03/ −0.23	2.07/ −0.13	ns
		XC6VHX250T	1.52/ −0.17	1.64/ −0.17	1.80/ −0.17	N/A	ns
		XC6VHX255T	1.52/ −0.12	1.64/ −0.12	1.85/ −0.12	N/A	ns
		XC6VHX380T	1.68/ −0.16	1.81/ −0.16	1.99/ −0.16	N/A	ns
		XC6VHX565T	N/A	1.81/ −0.01	1.99/ −0.01	N/A	ns
		XQ6VLX130T	N/A	1.65/ −0.18	1.81/ −0.18	1.87/ −0.07	ns
		XQ6VLX240T	N/A	1.66/ −0.17	1.82/ −0.17	1.87/ −0.08	ns
		XQ6VLX550T	N/A	N/A	2.02/ −0.17	2.06/ −0.06	ns
		XQ6VSX315T	N/A	1.68/ −0.18	1.84/ −0.18	1.89/ −0.08	ns
		XQ6VSX475T	N/A	N/A	2.03/ −0.23	2.07/ −0.13	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 FPGA clock transmitter and receiver data-valid windows.

Table 71: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion ⁽¹⁾	All	0.12	0.12	0.12	0.12	ns
T_{CKSKEW}	Global Clock Tree Skew ⁽²⁾	XC6VLX75T	0.15	0.16	0.18	0.17	ns
		XC6VLX130T	0.25	0.26	0.29	0.28	ns
		XC6VLX195T	0.26	0.27	0.31	0.30	ns
		XC6VLX240T	0.26	0.27	0.31	0.30	ns
		XC6VLX365T	0.28	0.29	0.31	0.31	ns
		XC6VLX550T	N/A	0.50	0.54	0.54	ns
		XC6VLX760	N/A	0.51	0.56	0.56	ns
		XC6VSX315T	0.27	0.28	0.32	0.30	ns
		XC6VSX475T	N/A	0.39	0.44	0.42	ns
		XC6VHX250T	0.25	0.26	0.29	N/A	ns
		XC6VHX255T	0.35	0.37	0.41	N/A	ns
		XC6VHX380T	0.45	0.47	0.52	N/A	ns
		XC6VHX565T	N/A	0.46	0.51	N/A	ns
		XQ6VLX130T	N/A	0.26	0.29	0.28	ns
		XQ6VLX240T	N/A	0.27	0.31	0.30	ns
		XQ6VLX550T	N/A	N/A	0.54	0.54	ns
		XQ6VSX315T	N/A	0.28	0.32	0.30	ns
		XQ6VSX475T	N/A	N/A	0.44	0.42	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.08	0.08	0.08	0.08	ns
T_{BUFIO_SKEW}	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	0.02	ns
T_{BUFIO_SKEW2}	I/O clock tree skew across three clock regions	All	0.10	0.12	0.23	0.12	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	ns

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 72: Package Skew

Symbol	Description	Device	Package	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	XC6VLX75T	FF484	95	ps
			FF784	146	ps
		XC6VLX130T	FF484	95	ps
			FF784	146	ps
			FF1156	165	ps
		XC6VLX195T	FF784	145	ps
			FF1156	182	ps
		XC6VLX240T	FF784	146	ps
			FF1156	182	ps
			FF1759	187	ps
		XC6VLX365T	FF1156	189	ps
			FF1759	184	ps
		XC6VLX550T	FF1759	196	ps
			FF1760	249	ps
		XC6VLX760	FF1760	236	ps
		XC6VSX315T	FF1156	168	ps
			FF1759	190	ps
		XC6VSX475T	FF1156	168	ps
			FF1759	204	ps
		XC6VHX250T	FF1154	166	ps
		XC6VHX255T	FF1155	168	ps
			FF1923	228	ps
		XC6VHX380T	FF1154	159	ps
			FF1155	172	ps
			FF1923	227	ps
			FF1924	220	ps
		XC6VHX565T	FF1923	232	ps
			FF1924	197	ps
		XQ6VLX130T	RF784	146	ps
			RF1156	165	ps
			FFG1156	165	ps
		XQ6VLX240T	RF784	146	ps
			RF1156	182	ps
			FFG1156	182	ps
			RF1759	187	ps
		XQ6VLX550T	RF1759	196	ps
		XQ6VSX315T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	190	ps
		XQ6VSX475T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	204	ps

Notes:

- These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
- Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Date	Version	Description of Revisions
02/08/11	2.12	Removed note 1 from Table 4 as the larger devices (XC6VLX550T, XC6VLX760, XC6VSX475T, and XC6VHX565T) are now offered in -2I. Updated Table 4 and Table 5 with data for the XC6VHX380T in the FF(G)1154 package. In Table 41 , updated -1L specification for DDR3. Added Note 1 to Table 42 . Moved the XC6VHX380T devices in the FF(G)1154 package to production release in Table 43 using ISE 12.4 software with current speed specifications. Updated description for F_{INDUTY} in Table 64 .
02/25/11	3.0	Designated the data sheet as Preliminary for all devices not already labeled production in Table 42 . Changed the XC6VHX380T devices in all packages to production status in Table 42 and Table 43 . Removed note 1 from Table 42 . Added maximum specifications to Table 25 . Updated $T_{HAVCC2HAVCCRX}$ in Table 27 . Updated the typical values and notes in Table 28 and Table 29 . Added values to Table 30 and Table 31 . In Table 34 , added values for T_{LOCK} and T_{PHASE} . Updated the values in Table 36 and added note 3. Updated Table 37 and added note 4.
03/21/11	3.1	Updated Table 2 including Note 7 . In Table 4 , added Note 3 and -2E, extended temperature range to the XC6VLX550T, XC6VLX760, XC6VSX475T, and XC6VHX380T devices, and added Note 5 for the XC6VHX565T. Updated Table 28 typical values. Updated the description for $F_{IDELAYCTRL_REF}$ in Table 53 . Updated F_{MCCK} in Table 59 .
04/01/11	3.2	Added T_j values for C, E, and I temperature ranges to Table 2 . Updated the I_{CCQ} values in Table 4 . Updated F_{GCLK} in Table 34 . Designated the data sheet as Production for all devices not already labeled production in Table 42 . Changed the XC6VHX255T and XC6VHX565T devices in all packages to production status in Table 42 and Table 43 . This included updates to the Virtex-6 Device Pin-to-Pin Output Parameter Guidelines and Virtex-6 Device Pin-to-Pin Input Parameter Guidelines for these devices. Production speed specifications for these devices are available using the speed specification v1.14 in the ISE 13.1 software update. Updated and added package skew values to Table 72 ; these values are correct with regards to previous production released speed specifications in software. Updated copyright page 1 and Notice of Disclaimer .
12/08/11	3.3	Production release of the Defense-grade XQ devices in Table 42 and Table 43 using ISE v13.3 v1.17 Patch for -2 and -1 speed specifications; and v1.10 for -1L speed specifications. Added the XQ6VLX130T, XQ6VLX240T, XQ6VLX550T, XQ6VSX315T, and XQ6VSX475T to the data sheet which included adding Table 45 . Updated T_j in Table 2 . In Table 40 , updated T_j for most specifications and added Note 4 . Added Note 4 to Table 41 . Added -1(XQ) speed specification columns only to Table 50 , Table 51 , Table 52 , and Table 58 . Updated V_{OD} in Table 8 , V_{OCM} in Table 9 , and V_{OCM} and V_{DIFF} in Table 10 . Updated the Power-On Power Supply Requirements section. In Table 27 , updated maximum specification for $T_{HAVCC2HAVCCRX}$ and added Note 3 . Updated T_j in Table 40 . In Table 41 , increased the DDR LVDS receiver (SPI-4.2) -1 speed grade performance value from 1.0 Gb/s to 1.1 Gb/s. In Table 60 , updated the F_{MAX} to add a separate row for the LX760 device values. The speed specifications in the software tools have always matched these values for the LX760, the data sheet is now correct. Updated the notes for $T_{OUTJITTER}$ in Table 64 .
01/12/12	3.4	Added the temperature range -2E to Note 5 in Table 4 .