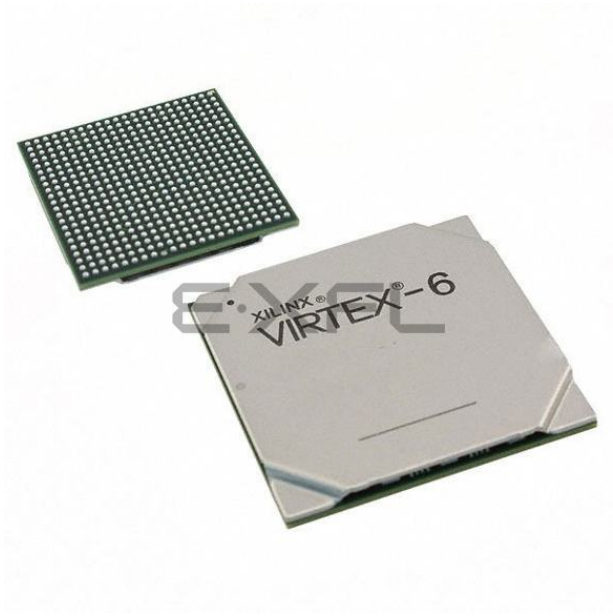
# AMD Xilinx - XC6VLX550T-1FFG1760I Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 42960 |
| Number of Logic Elements/Cells | 549888 |
| Total RAM Bits | 23298048 |
| Number of I/O | 1200 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.05V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1760-BBGA, FCBGA |
| Supplier Device Package | 1760-FCBGA (42.5x42.5) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc6vlx550t-1ffg1760i |

*Table 3:* **DC Characteristics Over Recommended Operating Conditions (1)(2)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{DRINT}$ | Data retention $V_{CCINT}$ voltage (below which configuration data might be lost) | 0.75 | – | – | V |
| $V_{DRI}$ | Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost) | 2.0 | – | – | V |
| $I_{REF}$ | $V_{REF}$ leakage current per pin | – | – | 10 | µA |
| $I_L$ | Input or output leakage current per pin (sample-tested) | – | – | 10 | µA |
| $C_{IN}$(3) | Die input capacitance at the pad | – | – | 8 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 2.5V | 20 | – | 80 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.8V | 8 | – | 40 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.5V | 5 | – | 30 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.2V | 1 | – | 20 | µA |
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{IN}$ = 2.5V | 3 | – | 80 | µA |
| $I_{BATT}$ | Battery supply current | – | – | 150 | nA |
| n | Temperature diode ideality factor | – | 1.0002 | – | n |
| r | Series resistance | – | 5 | – | Ω |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst case process at 25°C.
3. This measurement represents the die capacitance at the pad, not including the package.

*Table 16:* **GTX Transceiver Quiescent Supply Current (per Lane) (1)(2)(3)**

| Symbol | Description | Typ(4) | Max | Units |
|---|---|---|---|---|
| $I_{MGTAVTTQ}$ | Quiescent MGTAVTT supply current for one GTX transceiver | 0.9 | Note 2 | mA |
| $I_{MGTAVCCQ}$ | Quiescent MGTAVCC supply current for one GTX transceiver | 3.5 | | mA |

**Notes:**

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.
3. GTX transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX transceivers.
4. Typical values are specified at nominal voltage, 25°C.

## GTX Transceiver DC Input and Output Levels

Table 17 summarizes the DC output specifications of the GTX transceivers in Virtex-6 FPGAs. Consult UG366: *Virtex-6 FPGA GTX Transceivers User Guide* for further details.

*Table 17:* **GTX Transceiver DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $DV_{PPIN}$ | Differential peak-to-peak input voltage | External AC coupled ≤ 4.25 Gb/s | 125 | – | 2000 | mV |
| | | External AC coupled > 4.25 Gb/s | 175 | – | 2000 | mV |
| $V_{IN}$ | Absolute input voltage | DC coupled MGTAVTT = 1.2V | –400 | – | MGTAVTT | mV |
| $V_{CMIN}$ | Common mode input voltage | DC coupled MGTAVTT = 1.2V | – | 2/3 MGTAVTT | – | mV |
| $DV_{PPOUT}$ | Differential peak-to-peak output voltage(1) | Transmitter output swing is set to maximum setting | – | – | 1000 | mV |
| $V_{CMOUTDC}$ | DC common mode output voltage. | Equation based | MGTAVTT – $DV_{PPOUT}$/4 | | | mV |
| $R_{IN}$ | Differential input resistance | | 80 | 100 | 130 | Ω |
| $R_{OUT}$ | Differential output resistance | | 80 | 100 | 120 | Ω |
| $T_{OSKEW}$ | Transmitter output pair (TXP and TXN) intra-pair skew | | – | 2 | 8 | ps |
| $C_{EXT}$ | Recommended external AC coupling capacitor(2) | | – | 100 | – | nF |

**Notes:**

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG366: *Virtex-6 FPGA GTX Transceivers User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

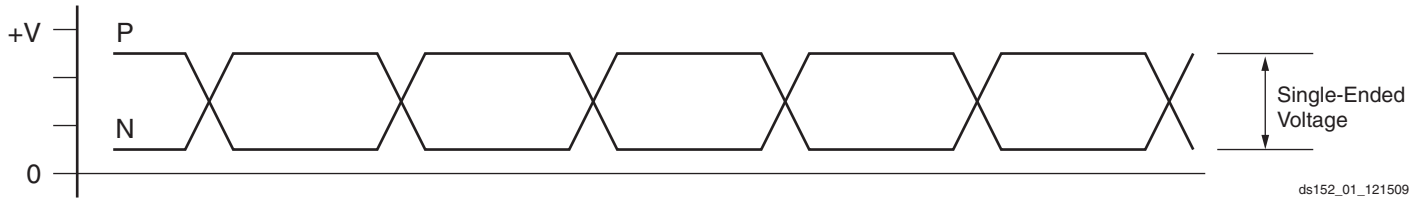


*Figure 1:* **Single-Ended Peak-to-Peak Voltage**

*Table 23:* **GTX Transceiver Transmitter Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTXTX}$ | Serial data rate range | | 0.480 | – | $F_{GTXMAX}$ | Gb/s |
| $T_{RTX}$ | TX Rise time | 20%–80% | – | 120 | – | ps |
| $T_{FTX}$ | TX Fall time | 80%–20% | – | 120 | – | ps |
| $T_{LLSKEW}$ | TX lane-to-lane skew(1) | | – | – | 350 | ps |
| $V_{TXOOBVDPP}$ | Electrical idle amplitude | | – | – | 15 | mV |
| $T_{TXOOBTRANSITION}$ | Electrical idle transition time | | – | – | 75 | ns |
| $TJ_{6.5}$ | Total Jitter(2)(3) | 6.5 Gb/s | – | – | 0.33 | UI |
| $DJ_{6.5}$ | Deterministic Jitter(2)(3) | | – | – | 0.17 | UI |
| $TJ_{5.0}$ | Total Jitter(2)(3) | 5.0 Gb/s | – | – | 0.33 | UI |
| $DJ_{5.0}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{4.25}$ | Total Jitter(2)(3) | 4.25 Gb/s | – | – | 0.33 | UI |
| $DJ_{4.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.14 | UI |
| $TJ_{3.75}$ | Total Jitter(2)(3) | 3.75 Gb/s | – | – | 0.34 | UI |
| $DJ_{3.75}$ | Deterministic Jitter(2)(3) | | – | – | 0.16 | UI |
| $TJ_{3.125}$ | Total Jitter(2)(3) | 3.125 Gb/s | – | – | 0.2 | UI |
| $DJ_{3.125}$ | Deterministic Jitter(2)(3) | | – | – | 0.1 | UI |
| $TJ_{3.125L}$ | Total Jitter(2)(3) | 3.125 Gb/s(4) | – | – | 0.35 | UI |
| $DJ_{3.125L}$ | Deterministic Jitter(2)(3) | | – | – | 0.16 | UI |
| $TJ_{2.5}$ | Total Jitter(2)(3) | 2.5 Gb/s(5) | – | – | 0.20 | UI |
| $DJ_{2.5}$ | Deterministic Jitter(2)(3) | | – | – | 0.08 | UI |
| $TJ_{1.25}$ | Total Jitter(2)(3) | 1.25 Gb/s(6) | – | – | 0.15 | UI |
| $DJ_{1.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.06 | UI |
| $TJ_{600}$ | Total Jitter(2)(3) | 600 Mb/s | – | – | 0.1 | UI |
| $DJ_{600}$ | Deterministic Jitter(2)(3) | | – | – | 0.03 | UI |
| $TJ_{480}$ | Total Jitter(2)(3) | 480 Mb/s | – | – | 0.1 | UI |
| $DJ_{480}$ | Deterministic Jitter(2)(3) | | – | – | 0.03 | UI |

**Notes:**

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
2. Using PLL_DIVSEL_FB = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 1.5625 GHz and OUTDIV = 1.
5. PLL frequency at 2.5 GHz and OUTDIV = 2.
6. PLL frequency at 2.5 GHz and OUTDIV = 4.

Figure 4 shows the timing parameters in Table 27.

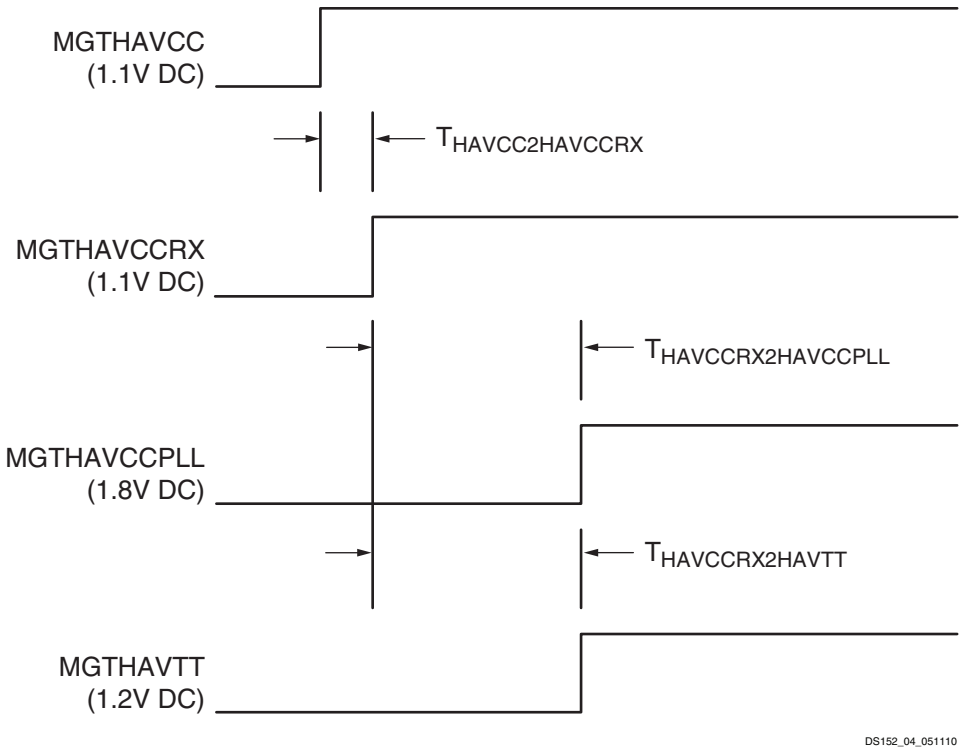


*Figure 4:* **GTH Transceiver Power Supply Power-On Sequencing**

*Table 28:* **GTH Transceiver Supply Current**

| Symbol | Description | Typ(1) | Max | Units |
|---|---|---|---|---|
| $I_{MGTHAVCC}$ | MGTHAVCC supply current for one GTH Quad (4 lanes) | 571 | Note 2 | mA |
| $I_{MGTHAVCCRX}$ | MGTHAVCCRX supply current for a GTH Quad (4 lanes) | 254 | Note 2 | mA |
| $I_{MGTHAVTT}$ | MGTHAVTT supply current for one GTH Quad (4 lanes) | 93 | Note 2 | mA |
| $I_{MGTHAVCCPLL}$ | MGTHAVCCPLL supply current for one GTH Quad (4 lanes) | 219 | Note 2 | mA |
| $MGTR_{REF}$ | Precision reference resistor for internal calibration termination | 1000.0 ± 1% tolerance | | Ω |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C, with a 10.3125 Gb/s line rate.
2. Values for currents other than the values specified in this table can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

*Table 29:* **GTH Transceiver Quiescent Supply Current(1)(2)**

| Symbol | Description | Typ(3) | Max | Units |
|---|---|---|---|---|
| $I_{MGTHAVCCQ}$ | Quiescent MGTHAVCC Supply Current for one GTH Quad (4 lanes) | 65 | Note 4 | mA |
| $I_{MGTHAVCCRXQ}$ | Quiescent MGTHAVCCRX Supply Current for one GTH Quad (4 lanes) | 17 | Note 4 | mA |
| $I_{MGTHAVTTQ}$ | Quiescent MGTHAVTT Supply Current for one GTH Quad (4 lanes) | 1 | Note 4 | mA |
| $I_{MGTHAVCCPLLQ}$ | Quiescent MGTHAVCCPLL Supply Current for one GTH Quad (4 lanes) | 1 | Note 4 | mA |

**Notes:**

1. Device powered and unconfigured.
2. GTH transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTH transceivers.
3. Typical values are specified at nominal voltage, 25°C.
4. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.

## GTH Transceiver Switching Characteristics

Consult UG371: *Virtex-6 FPGA GTH Transceivers User Guide* for further information.

*Table 32:* **GTH Transceiver Maximum Data Rate and PLL Frequency Range**

| Symbol | Description | Conditions | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | |
| $F_{GTHMAX}$ | Maximum GTH transceiver data rate | PLL Output Divider = 1 | 11.182 | 11.182 | 10.32 | Gb/s |
| | | PLL Output Divider = 4 | 2.795 | 2.795 | 2.58 | Gb/s |
| $F_{GTHMIN}$ | Minimum GTH transceiver data rate(1) | PLL Output Divider = 1 | 9.92 | 9.92 | 9.92 | Gb/s |
| | | PLL Output Divider = 4 | 2.48 | 2.48 | 2.48 | Gb/s |
| $F_{GPLLMAX}$ | Maximum GTH PLL frequency | | 5.591 | 5.591 | 5.16 | GHz |
| $F_{GPLLMIN}$ | Minimum GTH PLL frequency | | 4.96 | 4.96 | 4.96 | GHz |

**Notes:**

1. Lower data rates can be achieved using FPGA logic based oversampling designs.

*Table 33:* **GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1 | |
| $F_{GTHDRPCLK}$ | GTHDRPCLK maximum frequency | 70 | 70 | 60 | MHz |

*Table 34:* **GTH Transceiver Reference Clock Switching Characteristics**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $F_{GCLK}$ | Reference clock frequency range | -1 speed grade | 150 | – | 645 | MHz |
| | | -2 and -3 speed grades | 150 | – | 700 | MHz |
| $T_{RCLK}$ | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| $T_{FCLK}$ | Reference clock fall time | 80% – 20% | – | 200 | – | ps |
| $T_{DCREF}$ | Reference clock duty cycle | CLK | 45 | 50 | 55 | % |
| $T_{LOCK}$ | Clock recovery frequency acquisition time | Initial PLL lock | – | – | 2 | ms |
| $T_{PHASE}$ | Clock recovery phase acquisition time | Lock to data after PLL has locked to the reference clock | – | – | 20 | µs |

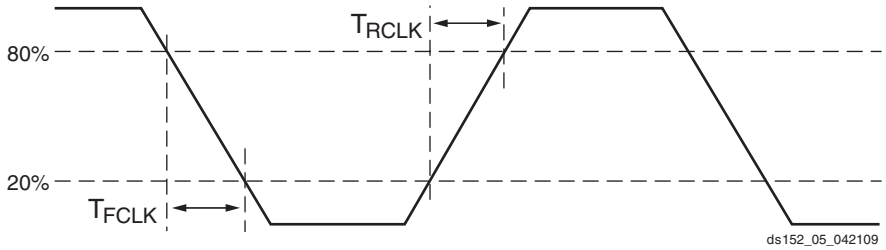


*Figure 5:* **Reference Clock Timing Parameters**

*Table 35:* **GTH Transceiver User Clock Switching Characteristics (1)**

| Symbol | Description | Conditions | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | |
| $F_{TXOUT}$ | TXUSERCLKOUT maximum frequency | | 350 | 350 | 323 | MHz |
| $F_{RXOUT}$ | RXUSERCLKOUT maximum frequency | | 350 | 350 | 323 | MHz |
| $F_{TXIN}$ | TXUSERCLKIN maximum frequency | 16-bit data path | 350 | 350 | 323 | MHz |
| | | 20-bit data path | 280 | 280 | 258 | MHz |
| | | 32-bit data path | 350 | 350 | 323 | MHz |
| | | 40-bit data path | 280 | 280 | 258 | MHz |
| | | 64-bit data path | 175 | 175 | 162 | MHz |
| | | 80-bit data path | 140 | 140 | 129 | MHz |
| | | 64B/66B-bit data path | 170 | 170 | 157 | MHz |
| $F_{RXIN}$ | RXUSERCLKIN maximum frequency | 16-bit data path | 350 | 350 | 323 | MHz |
| | | 20-bit data path | 280 | 280 | 258 | MHz |
| | | 32-bit data path | 350 | 350 | 323 | MHz |
| | | 40-bit data path | 280 | 280 | 258 | MHz |
| | | 64-bit data path | 175 | 175 | 162 | MHz |
| | | 80-bit data path | 140 | 140 | 129 | MHz |
| | | 64B/66B-bit data path | 170 | 170 | 157 | MHz |

**Notes:**

1. Clocking must be implemented as described in UG371:*Virtex-6 FPGA GTH Transceivers User Guide*.

*Table 36:* **GTH Transceiver Transmitter Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{RTX}$ | TX Rise time | 20%–80% | – | 50(3) | – | ps |
| $T_{FTX}$ | TX Fall time | 80%–20% | – | 50(3) | – | ps |
| $T_{LLSKEW}$ | TX lane-to-lane skew | within one GTH Quad | – | – | 300 | ps |
| **Transmitter Output Jitter(1)(2)** | | | | | | |
| $TJ_{11.18}$ | Total Jitter | 11.181 Gb/s | – | – | 0.280 | UI |
| $DJ_{11.18}$ | Deterministic Jitter | | – | – | 0.170 | UI |
| $TJ_{10.3125}$ | Total Jitter | 10.3125 Gb/s | – | – | 0.280 | UI |
| $DJ_{10.3125}$ | Deterministic Jitter | | – | – | 0.170 | UI |
| $TJ_{9.953}$ | Total Jitter | 9.953 Gb/s | – | – | 0.280 | UI |
| $DJ_{9.953}$ | Deterministic Jitter | | – | – | 0.170 | UI |
| $TJ_{2.667}$ | Total Jitter | 2.667 Gb/s | – | – | 0.110 | UI |
| $DJ_{2.667}$ | Deterministic Jitter | | – | – | 0.060 | UI |
| $TJ_{2.488}$ | Total Jitter | 2.488 Gb/s | – | – | 0.110 | UI |
| $DJ_{2.488}$ | Deterministic Jitter | | – | – | 0.060 | UI |

**Notes:**

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit-error ratio of $1e^{-12}$.
3. Rise and fall times are specified at the transmitter package balls.

# Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

*Table 39:* **Maximum Performance for PCI Express Designs**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $F_{PIPECLK}$ | Pipe clock maximum frequency | 250 | 250 | 250 | 250 | MHz |
| $F_{USERCLK}$ | User clock maximum frequency | 500 | 500 | 250 | 250 | MHz |
| $F_{DRPCLK}$ | DRP clock maximum frequency | 250 | 250 | 250 | 250 | MHz |

# System Monitor Analog-to-Digital Converter Specification

*Table 40:* **Analog-to-Digital Specifications**

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $AV_{DD}$ = 2.5V ± 5%, $V_{REFP}$ = 1.25V, $V_{REFN}$ = 0V, ADCCLK = 5.2 MHz, $T_j$ = –55°C to 125°C M-Grade, Typical values at $T_j$=+35°C | | | | | | |
| **DC Accuracy:** All external input channels. Both unipolar and bipolar modes. | | | | | | |
| Resolution | | | 10 | – | – | Bits |
| Integral Nonlinearity | INL | | – | – | ±1 | LSBs |
| Differential Nonlinearity | DNL | No missing codes ($T_{MIN}$ to $T_{MAX}$) Guaranteed Monotonic | – | – | ±0.9 | LSBs |
| Unipolar Offset Error (1) | | Uncalibrated | – | ±2 | ±30 | LSBs |
| Bipolar Offset Error (1) | | Uncalibrated measured in bipolar mode | – | ±2 | ±30 | LSBs |
| Gain Error | | Uncalibrated - External Reference | – | ±0.2 | ±2 | % |
| | | Uncalibrated - Internal Reference | – | ±2 | – | % |
| Bipolar Gain Error (1) | | Uncalibrated - External Reference | – | ±0.2 | ±2 | % |
| | | Uncalibrated - Internal Reference | – | ±2 | – | % |
| Total Unadjusted Error (Uncalibrated) | TUE | Deviation from ideal transfer function. External 1.25V reference | – | ±10 | – | LSBs |
| | | Deviation from ideal transfer function. Internal reference | – | ±20 | – | LSBs |
| Total Unadjusted Error (Calibrated) | TUE | Deviation from ideal transfer function. External 1.25V reference | – | ±1 | ±2 | LSBs |
| Calibrated Gain Temperature Coefficient | | Variation of FS code with temperature | – | ±0.01 | – | LSB/°C |
| DC Common-Mode Reject | $CMRR_{DC}$ | $V_N = V_{CM}$ = 0.5V ± 0.5V, $V_P – V_N$ = 100mV | – | 70 | – | dB |
| **Conversion Rate**(2) | | | | | | |
| Conversion Time - Continuous | $t_{CONV}$ | Number of CLK cycles | 26 | – | 32 | |
| Conversion Time - Event | $t_{CONV}$ | Number of CLK cycles | – | – | 21 | |
| T/H Acquisition Time | $t_{ACQ}$ | Number of CLK cycles | 4 | – | – | |
| DRP Clock Frequency | DCLK | DRP clock frequency | 8 | – | 80 | MHz |
| ADC Clock Frequency | ADCCLK | Derived from DCLK | 1 | – | 5.2 | MHz |
| CLK Duty cycle | | | 40 | – | 60 | % |

## Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.17 for -3, -2, and -1; and v1.10 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

### Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 42 correlates the current status of each Virtex-6 device on a per speed grade basis.

*Table 42:* **Virtex-6 Device Speed Grade Designations**

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XC6VLX75T | | | -3, -2, -1, -1L |
| XC6VLX130T | | | -3, -2, -1, -1L |
| XC6VLX195T | | | -3, -2, -1, -1L |
| XC6VLX240T | | | -3, -2, -1, -1L |
| XC6VLX365T | | | -3, -2, -1, -1L |
| XC6VLX550T | | | -2, -1, -1L |
| XC6VLX760 | | | -2, -1, -1L |
| XC6VSX315T | | | -3, -2, -1, -1L |
| XC6VSX475T | | | -2, -1, -1L |
| XC6VHX250T | | | -3, -2, -1 |
| XC6VHX255T | | | -3, -2, -1 |
| XC6VHX380T | | | -3, -2, -1 |
| XC6VHX565T | | | -2, -1 |
| XQ6VLX130T | | | -2, -1, -1L |
| XQ6VLX240T | | | -2, -1, -1L |
| XQ6VLX550T | | | -1, -1L |
| XQ6VSX315T | | | -2, -1, -1L |
| XQ6VSX475T | | | -1, -1L |

## Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 devices.

*Table 44:* **IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | |
| LVCMOS25, Fast, 24 mA | 0.51 | 0.57 | 0.66 | 0.70 | 1.66 | 1.79 | 1.99 | 1.96 | 1.66 | 1.79 | 1.99 | 1.96 | ns |
| LVCMOS18, Slow, 2 mA | 0.55 | 0.61 | 0.71 | 0.73 | 4.21 | 4.47 | 4.87 | 4.30 | 4.21 | 4.47 | 4.87 | 4.30 | ns |
| LVCMOS18, Slow, 4 mA | 0.55 | 0.61 | 0.71 | 0.73 | 2.79 | 2.96 | 3.21 | 2.94 | 2.79 | 2.96 | 3.21 | 2.94 | ns |
| LVCMOS18, Slow, 6 mA | 0.55 | 0.61 | 0.71 | 0.73 | 2.30 | 2.43 | 2.64 | 2.47 | 2.30 | 2.43 | 2.64 | 2.47 | ns |
| LVCMOS18, Slow, 8 mA | 0.55 | 0.61 | 0.71 | 0.73 | 2.01 | 2.11 | 2.27 | 2.24 | 2.01 | 2.11 | 2.27 | 2.24 | ns |
| LVCMOS18, Slow, 12 mA | 0.55 | 0.61 | 0.71 | 0.73 | 1.88 | 1.99 | 2.15 | 2.10 | 1.88 | 1.99 | 2.15 | 2.10 | ns |
| LVCMOS18, Slow, 16 mA | 0.55 | 0.61 | 0.71 | 0.73 | 1.84 | 1.95 | 2.11 | 2.04 | 1.84 | 1.95 | 2.11 | 2.04 | ns |
| LVCMOS18, Fast, 2 mA | 0.55 | 0.61 | 0.71 | 0.73 | 4.00 | 4.23 | 4.57 | 4.08 | 4.00 | 4.23 | 4.57 | 4.08 | ns |
| LVCMOS18, Fast, 4 mA | 0.55 | 0.61 | 0.71 | 0.73 | 2.62 | 2.76 | 2.97 | 2.74 | 2.62 | 2.76 | 2.97 | 2.74 | ns |
| LVCMOS18, Fast, 6 mA | 0.55 | 0.61 | 0.71 | 0.73 | 2.15 | 2.28 | 2.46 | 2.32 | 2.15 | 2.28 | 2.46 | 2.32 | ns |
| LVCMOS18, Fast, 8 mA | 0.55 | 0.61 | 0.71 | 0.73 | 1.90 | 1.99 | 2.13 | 2.14 | 1.90 | 1.99 | 2.13 | 2.14 | ns |
| LVCMOS18, Fast, 12 mA | 0.55 | 0.61 | 0.71 | 0.73 | 1.69 | 1.80 | 1.97 | 1.88 | 1.69 | 1.80 | 1.97 | 1.88 | ns |
| LVCMOS18, Fast, 16 mA | 0.55 | 0.61 | 0.71 | 0.73 | 1.63 | 1.74 | 1.91 | 1.88 | 1.63 | 1.74 | 1.91 | 1.88 | ns |
| LVCMOS15, Slow, 2 mA | 0.64 | 0.73 | 0.85 | 0.85 | 3.43 | 3.77 | 4.29 | 3.91 | 3.43 | 3.77 | 4.29 | 3.91 | ns |
| LVCMOS15, Slow, 4 mA | 0.64 | 0.73 | 0.85 | 0.85 | 2.58 | 2.79 | 3.10 | 2.93 | 2.58 | 2.79 | 3.10 | 2.93 | ns |
| LVCMOS15, Slow, 6 mA | 0.64 | 0.73 | 0.85 | 0.85 | 2.08 | 2.32 | 2.68 | 2.50 | 2.08 | 2.32 | 2.68 | 2.50 | ns |
| LVCMOS15, Slow, 8 mA | 0.64 | 0.73 | 0.85 | 0.85 | 1.81 | 1.98 | 2.23 | 2.24 | 1.81 | 1.98 | 2.23 | 2.24 | ns |
| LVCMOS15, Slow, 12 mA | 0.64 | 0.73 | 0.85 | 0.85 | 1.76 | 1.91 | 2.13 | 2.07 | 1.76 | 1.91 | 2.13 | 2.07 | ns |
| LVCMOS15, Slow, 16 mA | 0.64 | 0.73 | 0.85 | 0.85 | 1.69 | 1.83 | 2.04 | 1.98 | 1.69 | 1.83 | 2.04 | 1.98 | ns |
| LVCMOS15, Fast, 2 mA | 0.64 | 0.73 | 0.85 | 0.85 | 3.44 | 3.77 | 4.28 | 3.91 | 3.44 | 3.77 | 4.28 | 3.91 | ns |
| LVCMOS15, Fast, 4 mA | 0.64 | 0.73 | 0.85 | 0.85 | 2.37 | 2.53 | 2.78 | 2.66 | 2.37 | 2.53 | 2.78 | 2.66 | ns |
| LVCMOS15, Fast, 6 mA | 0.64 | 0.73 | 0.85 | 0.85 | 1.80 | 2.05 | 2.42 | 2.16 | 1.80 | 2.05 | 2.42 | 2.16 | ns |
| LVCMOS15, Fast, 8 mA | 0.64 | 0.73 | 0.85 | 0.85 | 1.76 | 1.90 | 2.11 | 2.04 | 1.76 | 1.90 | 2.11 | 2.04 | ns |
| LVCMOS15, Fast, 12 mA | 0.64 | 0.73 | 0.85 | 0.85 | 1.64 | 1.77 | 1.97 | 1.90 | 1.64 | 1.77 | 1.97 | 1.90 | ns |
| LVCMOS15, Fast, 16 mA | 0.64 | 0.73 | 0.85 | 0.85 | 1.62 | 1.76 | 1.96 | 1.92 | 1.62 | 1.76 | 1.96 | 1.92 | ns |
| LVCMOS12, Slow, 2 mA | 0.72 | 0.81 | 0.93 | 0.95 | 3.14 | 3.39 | 3.75 | 3.54 | 3.14 | 3.39 | 3.75 | 3.54 | ns |
| LVCMOS12, Slow, 4 mA | 0.72 | 0.81 | 0.93 | 0.95 | 2.43 | 2.63 | 2.93 | 2.79 | 2.43 | 2.63 | 2.93 | 2.79 | ns |
| LVCMOS12, Slow, 6 mA | 0.72 | 0.81 | 0.93 | 0.95 | 1.92 | 2.11 | 2.41 | 2.26 | 1.92 | 2.11 | 2.41 | 2.26 | ns |
| LVCMOS12, Slow, 8 mA | 0.72 | 0.81 | 0.93 | 0.95 | 1.87 | 2.02 | 2.25 | 2.17 | 1.87 | 2.02 | 2.25 | 2.17 | ns |
| LVCMOS12, Fast, 2 mA | 0.72 | 0.81 | 0.93 | 0.95 | 2.71 | 2.98 | 3.39 | 3.11 | 2.71 | 2.98 | 3.39 | 3.11 | ns |
| LVCMOS12, Fast, 4 mA | 0.72 | 0.81 | 0.93 | 0.95 | 1.93 | 2.16 | 2.51 | 2.31 | 1.93 | 2.16 | 2.51 | 2.31 | ns |
| LVCMOS12, Fast, 6 mA | 0.72 | 0.81 | 0.93 | 0.95 | 1.75 | 1.89 | 2.11 | 2.05 | 1.75 | 1.89 | 2.11 | 2.05 | ns |
| LVCMOS12, Fast, 8 mA | 0.72 | 0.81 | 0.93 | 0.95 | 1.69 | 1.82 | 2.02 | 1.98 | 1.69 | 1.82 | 2.02 | 1.98 | ns |
| LVDCI_25 | 0.51 | 0.57 | 0.66 | 0.70 | 2.05 | 2.14 | 2.26 | 2.26 | 2.05 | 2.14 | 2.26 | 2.26 | ns |
| LVDCI_18 | 0.55 | 0.61 | 0.71 | 0.73 | 2.07 | 2.23 | 2.47 | 2.38 | 2.07 | 2.23 | 2.47 | 2.38 | ns |
| LVDCI_15 | 0.64 | 0.73 | 0.85 | 0.85 | 1.85 | 2.01 | 2.24 | 2.18 | 1.85 | 2.01 | 2.24 | 2.18 | ns |

*Table 44:* **IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | |
| DIFF_SSTL18_I | 0.85 | 0.94 | 1.09 | 1.08 | 1.47 | 1.58 | 1.75 | 1.73 | 1.47 | 1.58 | 1.75 | 1.73 | ns |
| DIFF_SSTL18_I_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.40 | 1.51 | 1.67 | 1.65 | 1.40 | 1.51 | 1.67 | 1.65 | ns |
| DIFF_SSTL18_II | 0.85 | 0.94 | 1.09 | 1.08 | 1.39 | 1.50 | 1.67 | 1.66 | 1.39 | 1.50 | 1.67 | 1.66 | ns |
| DIFF_SSTL18_II_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.36 | 1.47 | 1.63 | 1.62 | 1.36 | 1.47 | 1.63 | 1.62 | ns |
| DIFF_SSTL18_II_T_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.40 | 1.51 | 1.67 | 1.65 | 1.40 | 1.51 | 1.67 | 1.65 | ns |
| DIFF_SSTL15 | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.71 | 1.69 | 1.42 | 1.54 | 1.71 | 1.69 | ns |
| DIFF_SSTL15_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.41 | 1.52 | 1.68 | 1.66 | 1.41 | 1.52 | 1.68 | 1.66 | ns |
| DIFF_SSTL15_T_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.41 | 1.52 | 1.68 | 1.66 | 1.41 | 1.52 | 1.68 | 1.66 | ns |

*Table 45:* **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices**

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| LVDS_25 | 0.94 | 1.09 | 1.08 | 1.54 | 2.16 | 1.62 | 1.54 | 2.16 | 1.62 | ns |
| LVDSEXT_25 | 0.94 | 1.09 | 1.08 | 1.65 | 2.20 | 1.73 | 1.65 | 2.20 | 1.73 | ns |
| HT_25 | 0.94 | 1.09 | 1.08 | 1.62 | 2.20 | 1.69 | 1.62 | 2.20 | 1.69 | ns |
| BLVDS_25 | 0.94 | 1.09 | 1.08 | 1.50 | 3.18 | 1.65 | 1.50 | 3.18 | 1.65 | ns |
| RSDS_25 (point to point) | 0.94 | 1.09 | 1.08 | 1.54 | 2.22 | 1.62 | 1.54 | 2.22 | 1.62 | ns |
| HSTL_I | 0.91 | 1.06 | 1.06 | 1.56 | 2.44 | 1.71 | 1.56 | 2.44 | 1.71 | ns |
| HSTL_II | 0.91 | 1.06 | 1.06 | 1.56 | 2.21 | 1.72 | 1.56 | 2.21 | 1.72 | ns |
| HSTL_III | 0.91 | 1.06 | 1.06 | 1.54 | 2.50 | 1.69 | 1.54 | 2.50 | 1.69 | ns |
| HSTL_I_18 | 0.91 | 1.06 | 1.06 | 1.58 | 2.43 | 1.72 | 1.58 | 2.43 | 1.72 | ns |
| HSTL_II_18 | 0.91 | 1.06 | 1.06 | 1.62 | 2.30 | 1.78 | 1.62 | 2.30 | 1.78 | ns |
| HSTL_III_18 | 0.91 | 1.06 | 1.06 | 1.54 | 2.49 | 1.69 | 1.54 | 2.49 | 1.69 | ns |
| SSTL2_I | 0.91 | 1.06 | 1.06 | 1.60 | 2.50 | 1.74 | 1.60 | 2.50 | 1.74 | ns |
| SSTL2_II | 0.91 | 1.06 | 1.06 | 1.54 | 2.49 | 1.71 | 1.54 | 2.49 | 1.71 | ns |
| SSTL15 | 0.91 | 1.06 | 1.06 | 1.54 | 2.07 | 1.69 | 1.54 | 2.07 | 1.69 | ns |
| LVCMOS25, Slow, 2 mA | 0.57 | 0.66 | 0.70 | 5.46 | 6.01 | 5.63 | 5.46 | 6.01 | 5.63 | ns |
| LVCMOS25, Slow, 4 mA | 0.57 | 0.66 | 0.70 | 3.49 | 3.79 | 3.65 | 3.49 | 3.79 | 3.65 | ns |
| LVCMOS25, Slow, 6 mA | 0.57 | 0.66 | 0.70 | 2.81 | 3.08 | 2.95 | 2.81 | 3.08 | 2.95 | ns |
| LVCMOS25, Slow, 8 mA | 0.57 | 0.66 | 0.70 | 2.41 | 2.72 | 2.59 | 2.41 | 2.72 | 2.59 | ns |
| LVCMOS25, Slow, 12 mA | 0.57 | 0.66 | 0.70 | 1.95 | 2.23 | 2.10 | 1.95 | 2.23 | 2.10 | ns |
| LVCMOS25, Slow, 16 mA | 0.57 | 0.66 | 0.70 | 2.05 | 2.29 | 2.21 | 2.05 | 2.29 | 2.21 | ns |
| LVCMOS25, Slow, 24 mA | 0.57 | 0.66 | 0.70 | 1.82 | 2.24 | 1.98 | 1.82 | 2.24 | 1.98 | ns |
| LVCMOS25, Fast, 2 mA | 0.57 | 0.66 | 0.70 | 5.49 | 6.04 | 5.62 | 5.49 | 6.04 | 5.62 | ns |
| LVCMOS25, Fast, 4 mA | 0.57 | 0.66 | 0.70 | 3.50 | 3.82 | 3.65 | 3.50 | 3.82 | 3.65 | ns |
| LVCMOS25, Fast, 6 mA | 0.57 | 0.66 | 0.70 | 2.73 | 2.99 | 2.88 | 2.73 | 2.99 | 2.88 | ns |
| LVCMOS25, Fast, 8 mA | 0.57 | 0.66 | 0.70 | 2.33 | 2.65 | 2.53 | 2.33 | 2.65 | 2.53 | ns |
| LVCMOS25, Fast, 12 mA | 0.57 | 0.66 | 0.70 | 1.88 | 2.08 | 2.03 | 1.88 | 2.08 | 2.03 | ns |

*Table 50:* **OLOGIC Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| **Setup/Hold** | | | | | | | |
| $T_{ODCK}/T_{OCKD}$ | D1/D2 pins Setup/Hold with respect to CLK | 0.45/ –0.08 | 0.50/ –0.08 | 0.54/ –0.08 | 0.54/ –0.08 | 0.69/ –0.11 | ns |
| $T_{OOCECK}/T_{OCKOCE}$ | OCE pin Setup/Hold with respect to CLK | 0.17/ –0.03 | 0.20/ –0.03 | 0.22/ –0.03 | 0.27/ –0.05 | 0.27/ –0.04 | ns |
| $T_{OSRCK}/T_{OCKSR}$ | SR pin Setup/Hold with respect to CLK | 0.59/ –0.24 | 0.62/ –0.24 | 0.54/ –0.08 | 0.54/ –0.08 | 0.79/ –0.35 | ns |
| $T_{OTCK}/T_{OCKT}$ | T1/T2 pins Setup/Hold with respect to CLK | 0.44/ –0.07 | 0.51/ –0.07 | 0.56/ –0.07 | 0.60/ –0.10 | 0.68/ –0.13 | ns |
| $T_{OTCECK}/T_{OCKTCE}$ | TCE pin Setup/Hold with respect to CLK | 0.15/ –0.04 | 0.19/ –0.04 | 0.21/ –0.04 | 0.27/ –0.05 | 0.29/ –0.05 | ns |
| **Combinatorial** | | | | | | | |
| $T_{DOQ}$ | D1 to OQ out or T1 to TQ out | 0.78 | 0.87 | 1.01 | 1.01 | 1.15 | ns |
| **Sequential Delays** | | | | | | | |
| $T_{OCKQ}$ | CLK to OQ/TQ out | 0.54 | 0.61 | 0.71 | 0.71 | 0.80 | ns |
| $T_{RQ}$ | SR pin to OQ/TQ out | 0.80 | 0.90 | 1.05 | 1.05 | 1.19 | ns |
| $T_{GSRQ}$ | Global Set/Reset to Q outputs | 7.60 | 7.60 | 10.51 | 10.51 | 10.51 | ns |
| **Set/Reset** | | | | | | | |
| $T_{RPW}$ | Minimum Pulse Width, SR inputs | 0.78 | 0.95 | 1.20 | 1.20 | 1.30 | ns, Min |

## Output Serializer/Deserializer Switching Characteristics

*Table 52:* **OSERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| **Setup/Hold** | | | | | | | |
| $T_{OSDCK\_D}/T_{OSCKD\_D}$ | D input Setup/Hold with respect to CLKDIV | 0.23/ –0.10 | 0.28/ –0.10 | 0.31/ –0.10 | 0.35/ –0.10 | 0.36/ –0.15 | ns |
| $T_{OSDCK\_T}/T_{OSCKD\_T}$(1) | T input Setup/Hold with respect to CLK | 0.44/ –0.10 | 0.51/ –0.09 | 0.56/ –0.08 | 0.60/ –0.08 | 0.68/ –0.15 | ns |
| $T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1) | T input Setup/Hold with respect to CLKDIV | 0.25/ –0.10 | 0.27/ –0.09 | 0.31/ –0.08 | 0.31/ –0.08 | 0.47/ –0.15 | ns |
| $T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$ | OCE input Setup/Hold with respect to CLK | 0.17/ –0.03 | 0.20/ –0.03 | 0.22/ –0.03 | 0.27/ –0.03 | 0.27/ –0.04 | ns |
| $T_{OSCCK\_S}$ | SR (Reset) input Setup with respect to CLKDIV | 0.07 | 0.07 | 0.07 | 0.07 | 0.08 | ns |
| $T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$ | TCE input Setup/Hold with respect to CLK | 0.15/ –0.04 | 0.19/ –0.04 | 0.21/ –0.04 | 0.27/ –0.04 | 0.29/ –0.05 | ns |
| **Sequential Delays** | | | | | | | |
| $T_{OSCKO\_OQ}$ | Clock to out from CLK to OQ | 0.63 | 0.71 | 0.82 | 0.82 | 0.93 | ns |
| $T_{OSCKO\_TQ}$ | Clock to out from CLK to TQ | 0.63 | 0.71 | 0.82 | 0.82 | 0.93 | ns |
| **Combinatorial** | | | | | | | |
| $T_{OSDO\_TTQ}$ | T input to TQ Out | 0.76 | 0.84 | 0.97 | 0.97 | 1.11 | ns |

**Notes:**

1. $T_{OSDCK\_T2}$ and $T_{OSCKD\_T2}$ are reported as $T_{OSDCK\_T}/T_{OSCKD\_T}$ in TRACE report.

## Block RAM and FIFO Switching Characteristics

*Table 57:* **Block RAM and FIFO Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| **Block RAM and FIFO Clock-to-Out Delays** | | | | | | |
| $T_{RCKO\_DO}$ and $T_{RCKO\_DO\_REG}$[1] | Clock CLK to DOUT output (without output register)[2][3] | 1.60 | 1.79 | 2.08 | 2.36 | ns, Max |
| | Clock CLK to DOUT output (with output register)[4][5] | 0.60 | 0.66 | 0.75 | 0.83 | ns, Max |
| $T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$ | Clock CLK to DOUT output with ECC (without output register)[2][3] | 2.62 | 2.89 | 3.30 | 3.73 | ns, Max |
| | Clock CLK to DOUT output with ECC (with output register)[4][5] | 0.71 | 0.77 | 0.86 | 0.94 | ns, Max |
| $T_{RCKO\_CASC}$ and $T_{RCKO\_CASC\_REG}$ | Clock CLK to DOUT output with Cascade (without output register)[2] | 2.49 | 2.77 | 3.18 | 3.61 | ns, Max |
| | Clock CLK to DOUT output with Cascade (with output register)[4] | 1.29 | 1.41 | 1.58 | 1.79 | ns, Max |
| $T_{RCKO\_FLAGS}$ | Clock CLK to FIFO flags outputs[6] | 0.74 | 0.81 | 0.91 | 0.98 | ns, Max |
| $T_{RCKO\_POINTERS}$ | Clock CLK to FIFO pointers outputs[7] | 0.90 | 0.98 | 1.09 | 1.21 | ns, Max |
| $T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$ | Clock CLK to BITERR (with output register) | 0.62 | 0.68 | 0.76 | 0.82 | ns, Max |
| | Clock CLK to BITERR (without output register) | 2.21 | 2.46 | 2.84 | 3.23 | ns, Max |
| $T_{RCKO\_PARITY\_ECC}$ | Clock CLK to ECCPARITY in ECC encode only mode | 0.86 | 0.94 | 1.06 | 1.18 | ns, Max |
| $T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$ | Clock CLK to RDADDR output with ECC (without output register) | 0.73 | 0.79 | 0.90 | 1.00 | ns, Max |
| | Clock CLK to RDADDR output with ECC (with output register) | 0.76 | 0.82 | 0.92 | 1.02 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | |
| $T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$ | ADDR inputs[8] | 0.47/ 0.27 | 0.53/ 0.29 | 0.62/ 0.32 | 0.66/ 0.34 | ns, Min |
| $T_{RDCK\_DI}/T_{RCKD\_DI}$ | DIN inputs[9] | 0.84/ 0.30 | 0.95/ 0.32 | 1.11/ 0.34 | 1.26/ 0.36 | ns, Min |
| $T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$ | DIN inputs with block RAM ECC in standard mode[9] | 0.47/ 0.30 | 0.52/ 0.32 | 0.59/ 0.34 | 0.68/ 0.36 | ns, Min |
| | DIN inputs with block RAM ECC encode only[9] | 0.68/ 0.30 | 0.75/ 0.32 | 0.85/ 0.34 | 0.97/ 0.36 | ns, Min |
| | DIN inputs with FIFO ECC in standard mode[9] | 0.77/ 0.30 | 0.87/ 0.32 | 1.02/ 0.34 | 1.16/ 0.36 | ns, Min |
| $T_{RCCK\_CLK}/T_{RCKC\_CLK}$ | Inject single/double bit error in ECC mode | 0.90/ 0.27 | 1.02/ 0.28 | 1.20/ 0.29 | 1.56/ 0.29 | ns, Min |
| $T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$ | Block RAM Enable (EN) input | 0.31/ 0.26 | 0.35/ 0.27 | 0.41/ 0.30 | 0.44/ 0.31 | ns, Min |
| $T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$ | CE input of output register | 0.18/ 0.25 | 0.19/ 0.27 | 0.22/ 0.31 | 0.24/ 0.33 | ns, Min |
| $T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$ | Synchronous RSTREG input | 0.22/ 0.23 | 0.24/ 0.24 | 0.28/ 0.26 | 0.31/ 0.27 | ns, Min |
| $T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$ | Synchronous RSTRAM input | 0.32/ 0.23 | 0.36/ 0.24 | 0.41/ 0.27 | 0.46/ 0.29 | ns, Min |

## DSP48E1 Switching Characteristics

*Table 58:* **DSP48E1 Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| **Setup and Hold Times of Data/Control Pins to the Input Register Clock** | | | | | | | |
| $T_{DSPDCK\_\{A, ACIN; B, BCIN\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{A, ACIN; B, BCIN\}\_\{AREG; BREG\}}$ | {A, ACIN, B, BCIN} input to {A, B} register CLK | 0.25/ 0.27 | 0.29/ 0.30 | 0.35/ 0.34 | 0.36/ 0.34 | 0.46/ 0.39 | ns |
| $T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$ | C input to C register CLK | 0.16/ 0.20 | 0.19/ 0.22 | 0.22/ 0.24 | 0.25/ 0.24 | 0.33/ 0.30 | ns |
| $T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$ | D input to D register CLK | 0.07/ 0.31 | 0.10/ 0.34 | 0.15/ 0.39 | 0.16/ 0.39 | 0.24/ 0.45 | ns |
| **Setup and Hold Times of Data Pins to the Pipeline Register Clock** | | | | | | | |
| $T_{DSPDCK\_\{A, ACIN, B, BCIN\}\_MREG\_MULT}$/ $T_{DSPCKD\_\{A, ACIN, B, BCIN\}\_MREG\_MULT}$ | {A, ACIN, B, BCIN} input to M register CLK | 2.36/ 0.04 | 2.70/ 0.04 | 3.21/ 0.04 | 3.21/ 0.04 | 3.66/ 0.02 | ns |
| $T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD\_\{A, D\}\_ADREG}$ | {A, D} input to AD register CLK | 1.24/ 0.10 | 1.42/ 0.12 | 1.69/ 0.13 | 1.69/ 0.13 | 1.91/ 0.16 | ns |
| **Setup and Hold Times of Data/Control Pins to the Output Register Clock** | | | | | | | |
| $T_{DSPDCK\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}$ | {A, ACIN, B, BCIN} input to P register CLK using multiplier | 3.83/ –0.13 | 4.37/ –0.13 | 5.20/ –0.13 | 5.20/ –0.13 | 5.94/ –0.24 | ns |
| $T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$ | D input to P register CLK | 3.62/ –0.47 | 4.13/ –0.47 | 4.90/ –0.47 | 4.90/ –0.47 | 5.61/ –0.77 | ns |
| $T_{DSPDCK\_\{A, ACIN, B, BCIN\}\_PREG}$/ $T_{DSPCKD\_\{A, ACIN, B, BCIN\}\_PREG}$ | {A, ACIN, B, BCIN} input to P register CLK not using multiplier | 1.59/ –0.13 | 1.81/ –0.13 | 2.15/ –0.13 | 2.15/ –0.13 | 2.44/ –0.24 | ns |
| $T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$ | C input to P register CLK | 1.42/ –0.10 | 1.61/ –0.10 | 1.91/ –0.10 | 1.91/ –0.10 | 2.16/ –0.19 | ns |
| $T_{DSPDCK\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_PREG}$/ $T_{DSPCKD\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_PREG}$ | {PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK | 1.23/ –0.02 | 1.41/ –0.02 | 1.67/ –0.02 | 1.67/ –0.02 | 1.91/ –0.07 | ns |
| **Setup and Hold Times of the CE Pins** | | | | | | | |
| $T_{DSPDCK\_\{CEA; CEB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{CEA; CEB\}\_\{AREG; BREG\}}$ | {CEA; CEB} input to {A; B} register CLK | 0.14/ 0.19 | 0.17/ 0.22 | 0.22/ 0.25 | 0.22/ 0.25 | 0.30/ 0.28 | ns |
| $T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$ | CEC input to C register CLK | 0.15/ 0.18 | 0.18/ 0.20 | 0.24/ 0.23 | 0.24/ 0.23 | 0.31/ 0.26 | ns |
| $T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$ | CED input to D register CLK | 0.20/ 0.12 | 0.24/ 0.13 | 0.31/ 0.14 | 0.31/ 0.14 | 0.43/ 0.16 | ns |
| $T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$ | CEM input to M register CLK | 0.16/ 0.19 | 0.20/ 0.21 | 0.26/ 0.25 | 0.26/ 0.25 | 0.32/ 0.28 | ns |
| $T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$ | CEP input to P register CLK | 0.32/ 0.02 | 0.38/ 0.02 | 0.46/ 0.03 | 0.46/ 0.03 | 0.54/ 0.04 | ns |
| **Setup and Hold Times of the RST Pins** | | | | | | | |
| $T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$ | {RSTA, RSTB} input to {A, B} register CLK | 0.27/ 0.17 | 0.31/ 0.19 | 0.38/ 0.22 | 0.38/ 0.22 | 0.41/ 0.25 | ns |
| $T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$ | RSTC input to C register CLK | 0.18/ 0.08 | 0.20/ 0.08 | 0.23/ 0.09 | 0.23/ 0.09 | 0.27/ 0.11 | ns |
| $T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$ | RSTD input to D register CLK | 0.28/ 0.15 | 0.32/ 0.16 | 0.38/ 0.19 | 0.38/ 0.19 | 0.45/ 0.21 | ns |
| $T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$ | RSTM input to M register CLK | 0.20/ 0.24 | 0.23/ 0.26 | 0.26/ 0.30 | 0.26/ 0.30 | 0.29/ 0.34 | ns |

*Table 58:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| $T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$ | RSTP input to P register CLK | 0.26/ 0.04 | 0.30/ 0.04 | 0.35/ 0.05 | 0.35/ 0.05 | 0.43/ 0.06 | ns |
| **Combinatorial Delays from Input Pins to Output Pins** | | | | | | | |
| $T_{DSPDO\_\{A, B\}\_\{P, CARRYOUT\}\_MULT}$ | {A, B} input to {P, CARRYOUT} output using multiplier | 3.76 | 4.29 | 5.08 | 5.08 | 5.87 | ns |
| $T_{DSPDO\_D\_\{P, CARRYOUT\}\_MULT}$ | D input to {P, CARRYOUT} output using multiplier | 3.57 | 4.07 | 4.82 | 4.82 | 5.57 | ns |
| $T_{DSPDO\_\{A, B\}\_\{P, CARRYOUT\}}$ | {A, B} input to {P, CARRYOUT} output not using multiplier | 1.55 | 1.76 | 2.07 | 2.07 | 2.41 | ns |
| $T_{DSPDO\_\{C, CARRYIN\}\_\{P, CARRYOUT\}}$ | {C, CARRYIN} input to {P, CARRYOUT} output | 1.38 | 1.56 | 1.83 | 1.83 | 2.13 | ns |
| **Combinatorial Delays from Input Pins to Cascading Output Pins** | | | | | | | |
| $T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$ | {A, B} input to {ACOUT, BCOUT} output | 0.49 | 0.56 | 0.65 | 0.65 | 0.73 | ns |
| $T_{DSPDO\_\{A, B\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$ | {A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier | 3.87 | 4.42 | 5.24 | 5.24 | 6.09 | ns |
| $T_{DSPDO\_D\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$ | D input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier | 3.66 | 4.17 | 4.94 | 4.94 | 5.76 | ns |
| $T_{DSPDO\_\{A, B\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$ | {A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier | 1.64 | 1.86 | 2.19 | 2.19 | 2.60 | ns |
| $T_{DSPDO\_\_\{C, CARRYIN\}\_\{PCOUT, CARRYCASCOUT,MULTSIGNOUT\}}$ | {C, CARRYIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output | 1.46 | 1.66 | 1.95 | 1.95 | 2.32 | ns |
| **Combinatorial Delays from Cascading Input Pins to All Output Pins** | | | | | | | |
| $T_{DSPDO\_\{ACIN, BCIN\}\_\{P, CARRYOUT\}\_MULT}$ | {ACIN, BCIN} input to {P, CARRYOUT} output using multiplier | 3.67 | 4.19 | 4.97 | 4.97 | 5.75 | ns |
| $T_{DSPDO\_\{ACIN, BCIN\}\_\{P, CARRYOUT}$ | {ACIN, BCIN} input to {P, CARRYOUT} output not using multiplier | 1.43 | 1.63 | 1.92 | 1.92 | 2.25 | ns |
| $T_{DSPDO\_\{ACIN; BCIN\}\_\{ACOUT; BCOUT\}}$ | {ACIN, BCIN} input to {ACOUT, BCOUT} output | 0.36 | 0.42 | 0.49 | 0.49 | 0.56 | ns |
| $T_{DSPDO\_\{ACIN, BCIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$ | {ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier | 3.76 | 4.29 | 5.10 | 5.10 | 5.94 | ns |
| $T_{DSPDO\_\{ACIN, BCIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$ | {ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier | 1.52 | 1.73 | 2.05 | 2.05 | 2.44 | ns |
| $T_{DSPDO\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_\{P, CARRYOUT\}}$ | {PCIN, CARRYCASCIN, MULTSIGNIN} input to {P, CARRYOUT} output | 1.19 | 1.35 | 1.60 | 1.60 | 1.87 | ns |

*Table 58:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| **Maximum Frequency** | | | | | | | |
| $F_{MAX}$ | With all registers used | 600 | 540 | 450 | 450 | 410 | MHz |
| $F_{MAX\_PATDET}$ | With pattern detector | 551 | 483 | 408 | 408 | 356 | MHz |
| $F_{MAX\_MULT\_NOMREG}$ | Two register multiply without MREG | 356 | 311 | 262 | 262 | 224 | MHz |
| $F_{MAX\_MULT\_NOMREG\_PATDET}$ | Two register multiply without MREG with pattern detect | 327 | 286 | 241 | 241 | 211 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG}$ | Without ADREG | 398 | 347 | 292 | 292 | 254 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$ | Without ADREG with pattern detect | 398 | 347 | 292 | 292 | 254 | MHz |
| $F_{MAX\_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG) | 266 | 233 | 196 | 196 | 171 | MHz |
| $F_{MAX\_NOPIPELINEREG\_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect | 250 | 219 | 184 | 184 | 160 | MHz |

## Configuration Switching Characteristics

*Table 59:* **Configuration Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| **Power-up Timing Characteristics** | | | | | | |
| $T_{PL}$(1) | Program Latency | 5 | 5 | 5 | 5 | ms, Max |
| $T_{POR}$(1) | Power-on-Reset | 15/55 | 15/55 | 15/55 | 15/60 | ms, Min/Max |
| $T_{ICCK}$ | CCLK (output) delay | 400 | 400 | 400 | 400 | ns, Min |
| $T_{PROGRAM}$ | Program Pulse Width | 250 | 250 | 250 | 250 | ns, Min |
| **Master/Slave Serial Mode Programming Switching** | | | | | | |
| $T_{DCCK}/T_{CCKD}$ | DIN Setup/Hold, slave mode | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | 4.5/0.0 | ns, Min |
| $T_{DSCCK}/T_{SCCKD}$ | DIN Setup/Hold, master mode | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | 5.0/0.0 | ns, Min |
| $T_{CCO}$ | DOUT at 2.5V | 6 | 6 | 6 | 7 | ns, Max |
| | DOUT at 1.8V | 6 | 6 | 6 | 7 | ns, Max |
| $F_{MCCK}$ | Maximum CCLK frequency, serial modes | 105 | 105 | 105 | 70 | MHz, Max |
| $F_{MCCKTOL}$ | Frequency Tolerance, master mode with respect to nominal CCLK. | 55 | 55 | 55 | 60 | % |
| $F_{MSCCK}$ | Slave mode external CCLK | 100 | 100 | 100 | 100 | MHz |
| **SelectMAP Mode Programming Switching** | | | | | | |
| $T_{SMDCCK}/T_{SMCCKD}$ | SelectMAP Data Setup/Hold | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | 5.5/0.0 | ns, Min |
| $T_{SMCSCCK}/T_{SMCCKCS}$ | CSI_B Setup/Hold | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | 5.5/0.0 | ns, Min |
| $T_{SMCCKW}/T_{SMWCCK}$ | RDWR_B Setup/Hold | 10.0/0.0 | 10.0/0.0 | 10.0/0.0 | 16.0/0.0 | ns, Min |
| $T_{SMCKCSO}$ | CSO_B clock to out (330 Ω pull-up resistor required) | 6 | 6 | 6 | 7 | ns, Max |
| $T_{SMCO}$ | CCLK to DATA out in readback at 2.5V | 6 | 6 | 6 | 7 | ns, Max |
| | CCLK to DATA out in readback at 1.8V | 6 | 6 | 6 | 7 | ns, Max |

*Table 70:* **Clock-Capable Clock Input Setup and Hold With MMCM**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1L | |
| **Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard.(1)** | | | | | | | |
| $T_{PSMMCMCC}$/ $T_{PHMMCMCC}$ | No Delay Clock-capable Clock Input and IFF(2) with MMCM | XC6VLX75T | 1.56/ –0.25 | 1.69/ –0.25 | 1.86/ –0.25 | 1.91/ –0.15 | ns |
| | | XC6VLX130T | 1.64/ –0.25 | 1.78/ –0.25 | 1.95/ –0.25 | 2.00/ –0.14 | ns |
| | | XC6VLX195T | 1.65/ –0.24 | 1.79/ –0.24 | 1.96/ –0.24 | 2.01/ –0.15 | ns |
| | | XC6VLX240T | 1.65/ –0.24 | 1.79/ –0.24 | 1.96/ –0.24 | 2.01/ –0.15 | ns |
| | | XC6VLX365T | 1.66/ –0.25 | 1.79/ –0.25 | 1.97/ –0.25 | 2.02/ –0.15 | ns |
| | | XC6VLX550T | N/A | 1.97/ –0.24 | 2.16/ –0.24 | 2.19/ –0.14 | ns |
| | | XC6VLX760 | N/A | 2.39/ –0.20 | 2.63/ –0.20 | 2.21/ –0.10 | ns |
| | | XC6VSX315T | 1.67/ –0.25 | 1.80/ –0.25 | 1.98/ –0.25 | 2.03/ –0.16 | ns |
| | | XC6VSX475T | N/A | 1.98/ –0.29 | 2.17/ –0.29 | 2.21/ –0.20 | ns |
| | | XC6VHX250T | 1.63/ –0.24 | 1.76/ –0.24 | 1.94/ –0.24 | N/A | ns |
| | | XC6VHX255T | 1.63/ –0.19 | 1.76/ –0.19 | 1.99/ –0.19 | N/A | ns |
| | | XC6VHX380T | 1.80/ –0.23 | 1.94/ –0.23 | 2.13/ –0.23 | N/A | ns |
| | | XC6VHX565T | N/A | 1.94/ –0.08 | 2.13/ –0.08 | N/A | ns |
| | | XQ6VLX130T | N/A | 1.78/ –0.25 | 1.95/ –0.25 | 2.00/ –0.14 | ns |
| | | XQ6VLX240T | N/A | 1.79/ –0.24 | 1.96/ –0.24 | 2.01/ –0.15 | ns |
| | | XQ6VLX550T | N/A | N/A | 2.16/ –0.24 | 2.19/ –0.14 | ns |
| | | XQ6VSX315T | N/A | 1.80/ –0.25 | 1.98/ –0.25 | 2.03/ –0.16 | ns |
| | | XQ6VSX475T | N/A | N/A | 2.17/ –0.29 | 2.21/ –0.20 | ns |

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 73:* **Sample Window**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1L | |
| $T_{SAMP}$ | Sampling Error at Receiver Pins(1) | All | 510 | 560 | 610 | 670 | ps |
| $T_{SAMP\_BUFIO}$ | Sampling Error at Receiver Pins using BUFIO(2) | All | 300 | 350 | 400 | 440 | ps |

**Notes:**

1. This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

*Table 74:* **Pin-to-Pin Setup/Hold and Clock-to-Out**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO** | | | | | | |
| $T_{PSCS}/T_{PHCS}$ | Setup/Hold of I/O clock | –0.28/1.09 | –0.28/1.16 | –0.28/1.33 | –0.18/1.79 | ns |
| **Pin-to-Pin Clock-to-Out Using BUFIO** | | | | | | |
| $T_{ICKOFCS}$ | Clock-to-Out of I/O clock | 4.22 | 4.59 | 5.22 | 5.63 | ns |

# Revision History

The following table shows the revision history for this document:

| Date | Version | Description of Revisions |
|---|---|---|
| 06/24/09 | 1.0 | Initial Xilinx release. |
| 07/16/09 | 1.1 | Revised the maximum $V_{CCAUX}$ and $V_{IN}$ numbers in Table 2, page 2. Removed empty column from Table 3, page 3. Revised specifications on Table 20, page 13. Updated Table 38, page 22 and added notes 1 and 2. Revised $T_{DLYCCO\_RDY}$, $T_{IDELAYCTRL\_RPW}$, and $T_{IDELAYPAT\_JIT}$ in Table 53, page 41. Updated Table 58, page 46 to more closely match the DSP48E1 speed specifications. Updated $T_{TAPTCK}/T_{TCKTAP}$ in Table 59, page 49. Updated XC6VLX130T parameters in Table 68 through Table 70, page 59. |
| 08/19/09 | 1.2 | Added values for -1L voltages and speed grade in all pertinent tables. Added $V_{FS}$ and notes to Table 1 and Table 2. Removed $DV_{PPIN}$ from the example in Figure 2. Added networking applications to Table 41, page 25. Changed and added to the block RAM $F_{MAX}$ section in Table 57, page 44 including removing Note 12. Changed $F_{PFDMAX}$ values and corrected units for $T_{STATPHAOFFSET}$ and $T_{OUTDUTY}$ in Table 64, page 52. Updated Table 71, page 60. |
| 09/16/09 | 2.0 | Added Virtex-6 HXT devices to entire document including GTH Transceiver Specifications. Updated speed specifications as described in Switching Characteristics, includes changes in Table 51, Table 57, Table 58, and Table 66 through Table 70. Comprehensive changes to Table 14, Table 15, and Table 16. Added conditions to $D_{VPPOUT}$ and revised description of $T_{OSKEW}$ in Table 17. Removed $V_{ISE}$ specification and note from Table 18. Added note 3 to Table 23. Updated note 3 in Table 24. Updated LVCMOS25 delays in Table 44. Updated specification for $T_{IOTPHZ}$ in Table 46. Removed $T_{BUFHSKEW}$ from Table 71, page 60 and added values for $T_{BUFIOSKEW}$. Added values in Table 74. |

| Date | Version | Description of Revisions |
|---|---|---|
| 02/08/11 | 2.12 | Removed note 1 from Table 4 as the larger devices (XC6VLX550T, XC6VLX760, XC6VSX475T, and XC6VHX565T) are now offered in -2I. Updated Table 4 and Table 5 with data for the XC6VHX380T in the FF(G)1154 package. In Table 41, updated -1L specification for DDR3. Added Note 1 to Table 42. Moved the XC6VHX380Tdevices in the FF(G)1154 package to production release in Table 43 using ISE 12.4 software with current speed specifications. Updated description for $F_{INDUTY}$ in Table 64. |
| 02/25/11 | 3.0 | Designated the data sheet as Preliminary for all devices not already labeled production in Table 42. Changed the XC6VHX380T devices in all packages to production status in Table 42 and Table 43. Removed note 1 from Table 42.<br>Added maximum specifications to Table 25. Updated $T_{HAVCC2HAVCCRX}$ in Table 27. Updated the typical values and notes in Table 28 and Table 29. Added values to Table 30 and Table 31. In Table 34, added values for $T_{LOCK}$ and $T_{PHASE}$. Updated the values in Table 36 and added note 3. Updated Table 37 and added note 4. |
| 03/21/11 | 3.1 | Updated Table 2 including Note 7. In Table 4, added Note 3 and -2E, extended temperature range to the XC6VLX550T, XC6VLX760, XC6VSX475T, and XC6VHX380T devices, and added Note 5 for the XC6VHX565T. Updated Table 28 typical values. Updated the description for $F_{IDELAYCTRL\_REF}$ in Table 53. Updated $F_{MCCK}$ in Table 59. |
| 04/01/11 | 3.2 | Added Tj values for C, E, and I temperature ranges to Table 2. Updated the $I_{CCQ}$ values in Table 4. Updated $F_{GCLK}$ in Table 34.<br>Designated the data sheet as Production for all devices not already labeled production in Table 42. Changed the XC6VHX255T and XC6VHX565T devices in all packages to production status in Table 42 and Table 43. This included updates to the Virtex-6 Device Pin-to-Pin Output Parameter Guidelines and Virtex-6 Device Pin-to-Pin Input Parameter Guidelines for these devices. Production speed specifications for these devices are available using the speed specification v1.14 in the ISE 13.1 software update.<br>Updated and added package skew values to Table 72; these values are correct with regards to previous production released speed specifications in software. Updated copyright page 1 and Notice of Disclaimer. |
| 12/08/11 | 3.3 | Production release of the Defense-grade XQ devices in Table 42 and Table 43 using ISE v13.3 v1.17 Patch for -2 and -1 speed specifications; and v1.10 for -1L speed specifications. Added the XQ6VLX130T, XQ6VLX240T, XQ6VLX550T, XQ6VSX315T, and XQ6VSX475T to the data sheet which included adding Table 45. Updated $T_j$ in Table 2. In Table 40, updated $T_j$ for most specifications and added Note 4. Added Note 4 to Table 41. Added -1(XQ) speed specification columns only to Table 50, Table 51, Table 52, and Table 58.<br>Updated $V_{OD}$ in Table 8, $V_{OCM}$ in Table 9, and $V_{OCM}$ and $V_{DIFF}$ in Table 10. Updated the Power-On Power Supply Requirements section. In Table 27, updated maximum specification for $T_{HAVCC2HAVCCRX}$ and added Note 3. Updated Tj in Table 40. In Table 41, increased the DDR LVDS receiver (SPI-4.2) -1 speed grade performance value from 1.0 Gb/s to 1.1 Gb/s. In Table 60, updated the $F_{MAX}$ to add a separate row for the LX760 device values. The speed specifications in the software tools have always matched these values for the LX760, the data sheet is now correct. Updated the notes for $T_{OUTJITTER}$ in Table 64. |
| 01/12/12 | 3.4 | Added the temperature range -2E to Note 5 in Table 4. |

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