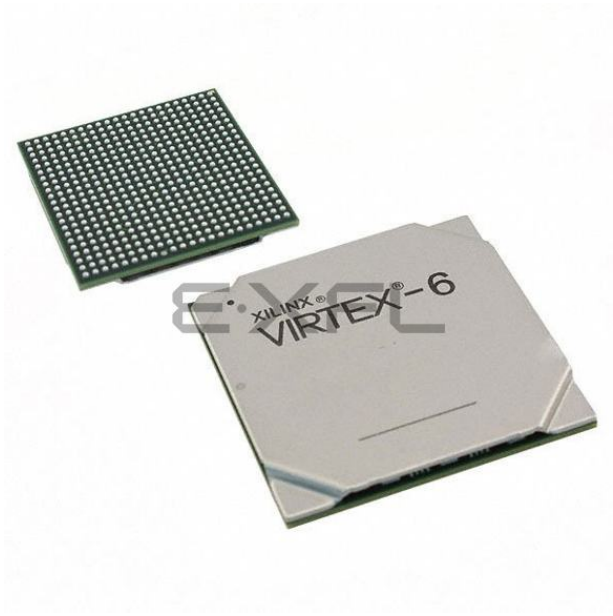

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Details	
Product Status	Active
Number of LABs/CLBs	5820
Number of Logic Elements/Cells	74496
Total RAM Bits	5750784
Number of I/O	240
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA, FCBGA
Supplier Device Package	484-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vlx75t-2ff484i

Table 2: **Recommended Operating Conditions**

Symbol	Description	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND for all devices except -1L devices.	0.95	1.05	V
	For -1L commercial temperature range devices: internal supply voltage relative to GND, T_j = 0°C to +85°C	0.87	0.93	V
	For -1L industrial temperature range devices: internal supply voltage relative to GND, T_j = –40°C to +100°C	0.91	0.97	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	2.375	2.625	V
V_{CCO}(1)(2)(3)	Supply voltage relative to GND	1.14	2.625	V
V_{IN}	2.5V supply voltage relative to GND	GND – 0.20	2.625	V
	2.5V and below supply voltage relative to GND	GND – 0.20	V_{CCO} + 0.2	V
I_{IN}(5)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	10	mA
V_{BATT}(6)	Battery voltage relative to GND	1.0	2.5	V
V_{FS}(7)	External voltage supply for eFUSE programming	2.375	2.625	V
T_j	Junction temperature operating range for commercial (C) temperature devices	0	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	100	°C
	Junction temperature operating range for military (M) temperature devices	–55	125	°C

Notes:

1. Configuration data is retained even if V_{CCO} drops to 0V.
2. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, and 2.5V.
3. The configuration supply voltage V_{CC_CONFIG} is also known as V_{CCO_0}.
4. All voltages are relative to ground.
5. A total of 100 mA per bank should not be exceeded.
6. V_{BATT} is required only when using bitstream encryption. If battery is not used, connect V_{BATT} to either ground or V_{CCAUX}.
7. During eFUSE programming, V_{FS} must be within the recommended operating range and T_j = +15°C to +85°C. Otherwise, V_{FS} can be connected to GND.

Table 4: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed and Temperature Grade						Units
			-3 (C)	-2 (C, E, & I)	-1 (C & I)	-1 (I & M)(2)	-1L (C)	-1L (I)(1)	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC6VLX75T	45	45	45	N/A	45	45	mA
		XC6VLX130T	75	75	75	N/A	75	75	mA
		XC6VLX195T	113	113	113	N/A	113	113	mA
		XC6VLX240T	135	135	135	N/A	135	135	mA
		XC6VLX365T	191	191	191	N/A	191	191	mA
		XC6VLX550T(3)	N/A	286	286	N/A	286	286	mA
		XC6VLX760(3)	N/A	387	387	N/A	387	387	mA
		XC6VSX315T	186	186	186	N/A	186	186	mA
		XC6VSX475T(3)	N/A	279	279	N/A	279	279	mA
		XC6VHX250T	152	152	152	N/A	N/A	N/A	mA
		XC6VHX255T	152	152	152	N/A	N/A	N/A	mA
		XC6VHX380T(4)	227	227	227	N/A	N/A	N/A	mA
		XC6VHX565T(5)	N/A	315	315	N/A	N/A	N/A	mA
		XQ6VLX130T(6)	N/A	75	N/A	75	N/A	75	mA
		XQ6VLX240T(6)	N/A	135	N/A	135	N/A	135	mA
		XQ6VLX550T(7)	N/A	N/A	N/A	286	N/A	286	mA
		XQ6VSX315T(6)	N/A	186	N/A	186	N/A	186	mA
		XQ6VSX475T(7)	N/A	N/A	N/A	279	N/A	279	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j). -1 and -2 industrial (I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. -1L industrial temperature range devices have the values specified in this column.
2. Use the XPE tool to calculate 125°C values for -1M temperature range devices.
3. The -2E extended temperature range (T_j = 0°C to +100°C) is only available in these devices. The -2I temperature range (T_j = –40°C to +100°C) is available for all other devices except the XC6VHX565T.
4. The XC6VHX380T is available with both -2E and -2I temperature ranges.
5. The XC6VHX565T is only available in the following temperature ranges: -1C, -1I, -2C, and -2E.
6. The XQ6VLX130T, XQ6VLX240T, and XQ6VSX315T are available in -2I, -1I, -1M, and -1LI temperature ranges.
7. The XQ6VLX550T and the XQ6VSX475T are only available in -1I and -1LI temperature ranges.
8. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
9. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPE or XPower Analyzer (XPA) tools.

HT DC Specifications (HT_25)

Table 8: **HT DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage for XC devices	R_T = 100 Ω across Q and $\overline{Q}$ signals	480	600	885	mV
	Differential Output Voltage for XQ devices		480	600	930	mV
ΔV_{OD}	Change in V_{OD} Magnitude		–15	–	15	mV
V_{OCM}	Output Common Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	440	600	760	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		–15	–	15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		–15	–	15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		–15	–	15	mV

LVDS DC Specifications (LVDS_25)

Table 9: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage for XC devices	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
	Output Common-Mode Voltage for XQ devices		1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 10: **Extended LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.715	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High for XC devices	R_T = 100 Ω across Q and $\overline{Q}$ signals	350	–	840	mV
	Differential Output Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High for XQ devices		350	–	850	mV
V_{OCM}	Output Common-Mode Voltage for XC devices	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
	Output Common-Mode Voltage for XQ devices		1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	–	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 13: **Absolute Maximum Ratings for GTX Transceivers(1)**

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	–0.5	1.1	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	–0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 14: **Recommended Operating Conditions for GTX Transceivers(1)(2)**

Symbol	Description	Speed Grade	PLL Frequency	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	-3, -2(3)	> 2.7 GHz	1.0	1.03	1.06	V
		-3, -2(3)	≤ 2.7 GHz	0.95	1.0	1.06	V
		-1	≤ 2.7 GHz	0.95	1.0	1.06	V
		-1L	≤ 2.7 GHz	0.95	1.0	1.05	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	All	–	1.14	1.2	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	All	–	1.14	1.2	1.26	V

Notes:

1. Each voltage listed requires the filter circuit described in UG366: *Virtex-6 FPGA GTX Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +100°C for all XC devices and T_j = –55°C to +125°C for the XQ devices
3. If a GTX Quad contains transceivers operating with a mixture of PLL frequencies above and below 2.7 GHz, the MGTAVCC voltage supply must be in the range of 1.0V to 1.06V.

Table 15: **GTX Transceiver Supply Current (per Lane) (1)(2)**

Symbol	Description	Typ	Max	Units
$I_{MGTAVTT}$	MGTAVTT supply current for one GTX transceiver	55.9	Note 2	mA
$I_{MGTAVCC}$	MGTAVCC supply current for one GTX transceiver	56.1		mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	100.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
2. Values for currents of other transceiver configurations and conditions can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

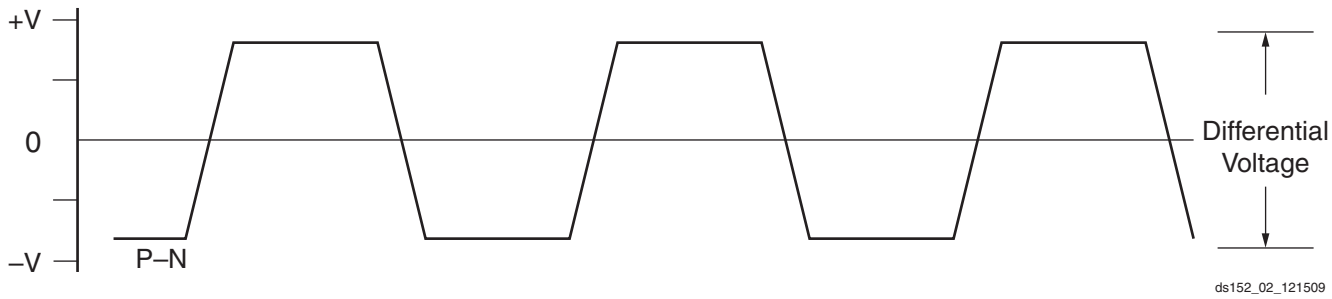

Figure 2: **Differential Peak-to-Peak Voltage**

Table 18 summarizes the DC specifications of the clock input of the GTX transceiver. Consult UG366: *Virtex-6 FPGA GTX Transceivers User Guide* for further details.

Table 18: **GTX Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	210	800	2000	mV
R_{IN}	Differential input resistance	90	100	130	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTX Transceiver Switching Characteristics

Consult UG366: *Virtex-6 FPGA GTX Transceivers User Guide* for further information.

Table 19: **GTX Transceiver Performance**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F_{GTXMAX}	Maximum GTX transceiver data rate	6.6	6.6	5.0	5.0	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	3.3(1)	3.3(1)	2.7	2.7	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.2	1.2	1.2	1.2	GHz

Notes:

1. See Table 14 for MGTAVCC requirements when PLL frequency is greater than 2.7 GHz.

Table 20: **GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	150	150	125	100	MHz

GTH Transceiver DC Input and Output Levels

Table 30 summarizes the DC output specifications of the GTH transceivers in Virtex-6 FPGAs. Consult UG371: *Virtex-6 FPGA GTH Transceivers User Guide* for further details.

Table 30: **GTH Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
D_{VPPIN}	Differential peak-to-peak input voltage	External AC coupled	175	–	1200	mV
D_{VPPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to maximum setting	800	–	1200	mV
R_{IN}	Differential input resistance		80	100	120	Ω
R_{OUT}	Differential output resistance		80	100	120	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	–	ps
C_{EXT}	Recommended external AC coupling capacitor(2)		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG371: *Virtex-6 FPGA GTH Transceivers User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 31 summarizes the DC specifications of the clock input of the GTH transceiver. Consult UG371: *Virtex-6 FPGA GTH Transceivers User Guide* for further details.

Table 31: **GTH Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	≤ 600 MHz	500	–	1600	mV
		> 600 MHz	600	–	1600	mV
R_{IN}	Differential input resistance		80	100	120	Ω
C_{EXT}	Required external AC coupling capacitor		–	100	–	nF

Table 35: **GTH Transceiver User Clock Switching Characteristics (1)**

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F_{TXOUT}	TXUSERCLKOUT maximum frequency		350	350	323	MHz
F_{RXOUT}	RXUSERCLKOUT maximum frequency		350	350	323	MHz
F_{TXIN}	TXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz
F_{RXIN}	RXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz

Notes:

1. Clocking must be implemented as described in UG371:*Virtex-6 FPGA GTH Transceivers User Guide*.

Table 36: **GTH Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
T_{RTX}	TX Rise time	20%–80%	–	50(3)	–	ps
T_{FTX}	TX Fall time	80%–20%	–	50(3)	–	ps
T_{LLSKEW}	TX lane-to-lane skew	within one GTH Quad	–	–	300	ps
Transmitter Output Jitter(1)(2)						
$TJ_{11.18}$	Total Jitter	11.181 Gb/s	–	–	0.280	UI
$DJ_{11.18}$	Deterministic Jitter		–	–	0.170	UI
$TJ_{10.3125}$	Total Jitter	10.3125 Gb/s	–	–	0.280	UI
$DJ_{10.3125}$	Deterministic Jitter		–	–	0.170	UI
$TJ_{9.953}$	Total Jitter	9.953 Gb/s	–	–	0.280	UI
$DJ_{9.953}$	Deterministic Jitter		–	–	0.170	UI
$TJ_{2.667}$	Total Jitter	2.667 Gb/s	–	–	0.110	UI
$DJ_{2.667}$	Deterministic Jitter		–	–	0.060	UI
$TJ_{2.488}$	Total Jitter	2.488 Gb/s	–	–	0.110	UI
$DJ_{2.488}$	Deterministic Jitter		–	–	0.060	UI

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit-error ratio of $1e^{-12}$.
3. Rise and fall times are specified at the transmitter package balls.

Table 37: **GTH Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
R_{XRL}	Run length (CID)		8000	–	–	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance		–200	–	200	ppm
SJ Jitter Tolerance(1)(2)(3)(4)						
$JT\_SJ_{11.18}$	Sinusoidal Jitter	11.18 Gb/s	0.3	–	–	UI
$JT\_SJ_{10.32}$	Sinusoidal Jitter	10.32 Gb/s	0.3	–	–	UI
$JT\_SJ_{9.95}$	Sinusoidal Jitter	9.95 Gb/s	0.3	–	–	UI
$JT\_SJ_{2.667}$	Sinusoidal Jitter	2.667 Gb/s	0.5	–	–	UI
$JT\_SJ_{2.48}$	Sinusoidal Jitter	2.48 Gb/s	0.5	–	–	UI

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. High-frequency jitter tolerance including 6 db of channel loss at a high frequency of the data rate divided by two.

Ethernet MAC Switching Characteristics

Consult UG368: *Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide* for further information.

Table 38: **Maximum Ethernet MAC Performance**

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1	-1L	
$F_{TEMACCLIENT}$	Client interface maximum frequency	10 Mb/s – 8-bit width	2.5(1)	2.5(1)	2.5(1)	2.5(1)	MHz
		100 Mb/s – 8-bit width	25(2)	25(2)	25(2)	25(2)	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		1000 Mb/s – 16-bit width	62.5	62.5	62.5	62.5	MHz
		2000 Mb/s – 16-bit width	125	125	125	N/A	MHz
		2500 Mb/s – 16-bit width	156.25	156.25	156.25	N/A	MHz
$F_{TEMACPHY}$	Physical interface maximum frequency	10 Mb/s – 4-bit width	2.5	2.5	2.5	2.5	MHz
		100 Mb/s – 4-bit width	25	25	25	25	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		2000 Mb/s – 8-bit width	250	250	250	N/A	MHz
		2500 Mb/s – 8-bit width	312.5	312.5	312.5	N/A	MHz

Notes:

1. When not using clock enable, the F_{MAX} is lowered to 1.25 MHz.
2. When not using clock enable, the F_{MAX} is lowered to 12.5 MHz.

Table 40: **Analog-to-Digital Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Analog Inputs[3]						
Dedicated Analog Inputs Input Voltage Range V_P - V_N		Unipolar Operation	0	–	1	Volts
		Bipolar Operation	–0.5	–	+0.5	
		Unipolar Common Mode Range (FS input)	0	–	+0.5	
		Bipolar Common Mode Range (FS input)	+0.5	–	+0.6	
		Bandwidth	–	20	–	MHz
Auxiliary Analog Inputs Input Voltage Range $V_{AUXP[0]}$ /$V_{AUXN[0]}$ to $V_{AUXP[15]}$ /$V_{AUXN[15]}$ T_j = –55°C to 125°C		Unipolar Operation	0	–	1	Volts
		Bipolar Operation	–0.5	–	+0.5	
		Unipolar Common Mode Range (FS input)	0	–	+0.5	
		Bipolar Common Mode Range (FS input)	+0.5	–	+0.6	
		Bandwidth	–	10	–	kHz
Input Leakage Current		A/D not converting, ADCCLK stopped	–	±1.0	–	µA
Input Capacitance			–	10	–	pF
On-chip Supply Monitor Error		V_{CCINT} and V_{CCAUX} with calibration enabled. External 1.25V reference T_j = –55°C to 125°C.	–	–	±1.0	% Reading
		V_{CCINT} and V_{CCAUX} with calibration enabled. Internal reference T_j = –40°C to 100°C.[4]	–	±2	–	% Reading
On-chip Temperature Monitor Error		T_j = –55°C to +125°C with calibration enabled. External 1.25V reference.	–	–	±4	°C
		T_j = –40°C to +100°C with calibration enabled. Internal reference.[4]	–	±5	–	°C
External Reference Inputs[5]						
Positive Reference Input Voltage Range	V_{REFP}	Measured Relative to V_{REFN}	1.20	1.25	1.30	Volts
Negative Reference Input Voltage Range	V_{REFN}	Measured Relative to AGND	–50	0	100	mV
Input current	I_{REF}	ADCCLK = 5.2 MHz	–	–	100	µA
Power Requirements						
Analog Power Supply	AV_{DD}	Measured Relative to AV_{SS}	2.375	2.5	2.625	Volts
Analog Supply Current	AI_{DD}	ADCCLK = 5.2 MHz	–	–	12	mA

Notes:

1. Offset errors are removed by enabling the System Monitor automatic gain calibration feature.
2. See "System Monitor Timing" in UG370: *Virtex-6 FPGA System Monitor User Guide*
3. See "Analog Inputs" in UG370: *Virtex-6 FPGA System Monitor User Guide* for a detailed description.
4. These internal references are not specified over the junction temperature operating range for military (M) temperature devices.
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function.This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the Switching Characteristics, page 26.

Table 41: **Interface Performances**

Description	Speed Grade			
	-3	-2	-1	-1L
Networking Applications				
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	710 Mb/s	710 Mb/s	650 Mb/s	585 Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 10)	1.4 Gb/s	1.3 Gb/s	1.25 Gb/s	1.1 Gb/s
SDR LVDS receiver (SFI-4.1)(1)	710 Mb/s	710 Mb/s	650 Mb/s	585 Mb/s
DDR LVDS receiver (SPI-4.2)(1)	1.4 Gb/s	1.3 Gb/s	1.1 Gb/s	0.9 Gb/s
Maximum Physical Interface (PHY) Rate for Memory Interfaces(2)(3)(4)				
DDR2	800 Mb/s	800 Mb/s	800 Mb/s	606 Mb/s
DDR3	1066 Mb/s	1066 Mb/s	800 Mb/s	800 Mb/s
QDR II + SRAM	400 MHz	350 MHz	300 MHz	–
RLDRAM II	500 MHz	400 MHz	350 MHz	–

Notes:

1. LVDS receivers are typically bounded with certain applications where specific DPA algorithms dominate deterministic performance.
2. Verified on Xilinx memory characterization platforms designed according to the guidelines in UG: *Virtex-6 FPGA Memory Interface Solutions User Guide*.
3. Consult DS186: *Virtex-6 FPGA Memory Interface Solutions Data Sheet* for performance and feature information on memory interface cores (controller plus PHY).
4. Memory Interface data rates have not been tested over the junction temperature operating range for military (M) temperature devices. Customers are responsible for specifying and testing their specific M temperature grade memory implementation.

Table 44: **IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVCMOS25, Fast, 24 mA	0.51	0.57	0.66	0.70	1.66	1.79	1.99	1.96	1.66	1.79	1.99	1.96	ns
LVCMOS18, Slow, 2 mA	0.55	0.61	0.71	0.73	4.21	4.47	4.87	4.30	4.21	4.47	4.87	4.30	ns
LVCMOS18, Slow, 4 mA	0.55	0.61	0.71	0.73	2.79	2.96	3.21	2.94	2.79	2.96	3.21	2.94	ns
LVCMOS18, Slow, 6 mA	0.55	0.61	0.71	0.73	2.30	2.43	2.64	2.47	2.30	2.43	2.64	2.47	ns
LVCMOS18, Slow, 8 mA	0.55	0.61	0.71	0.73	2.01	2.11	2.27	2.24	2.01	2.11	2.27	2.24	ns
LVCMOS18, Slow, 12 mA	0.55	0.61	0.71	0.73	1.88	1.99	2.15	2.10	1.88	1.99	2.15	2.10	ns
LVCMOS18, Slow, 16 mA	0.55	0.61	0.71	0.73	1.84	1.95	2.11	2.04	1.84	1.95	2.11	2.04	ns
LVCMOS18, Fast, 2 mA	0.55	0.61	0.71	0.73	4.00	4.23	4.57	4.08	4.00	4.23	4.57	4.08	ns
LVCMOS18, Fast, 4 mA	0.55	0.61	0.71	0.73	2.62	2.76	2.97	2.74	2.62	2.76	2.97	2.74	ns
LVCMOS18, Fast, 6 mA	0.55	0.61	0.71	0.73	2.15	2.28	2.46	2.32	2.15	2.28	2.46	2.32	ns
LVCMOS18, Fast, 8 mA	0.55	0.61	0.71	0.73	1.90	1.99	2.13	2.14	1.90	1.99	2.13	2.14	ns
LVCMOS18, Fast, 12 mA	0.55	0.61	0.71	0.73	1.69	1.80	1.97	1.88	1.69	1.80	1.97	1.88	ns
LVCMOS18, Fast, 16 mA	0.55	0.61	0.71	0.73	1.63	1.74	1.91	1.88	1.63	1.74	1.91	1.88	ns
LVCMOS15, Slow, 2 mA	0.64	0.73	0.85	0.85	3.43	3.77	4.29	3.91	3.43	3.77	4.29	3.91	ns
LVCMOS15, Slow, 4 mA	0.64	0.73	0.85	0.85	2.58	2.79	3.10	2.93	2.58	2.79	3.10	2.93	ns
LVCMOS15, Slow, 6 mA	0.64	0.73	0.85	0.85	2.08	2.32	2.68	2.50	2.08	2.32	2.68	2.50	ns
LVCMOS15, Slow, 8 mA	0.64	0.73	0.85	0.85	1.81	1.98	2.23	2.24	1.81	1.98	2.23	2.24	ns
LVCMOS15, Slow, 12 mA	0.64	0.73	0.85	0.85	1.76	1.91	2.13	2.07	1.76	1.91	2.13	2.07	ns
LVCMOS15, Slow, 16 mA	0.64	0.73	0.85	0.85	1.69	1.83	2.04	1.98	1.69	1.83	2.04	1.98	ns
LVCMOS15, Fast, 2 mA	0.64	0.73	0.85	0.85	3.44	3.77	4.28	3.91	3.44	3.77	4.28	3.91	ns
LVCMOS15, Fast, 4 mA	0.64	0.73	0.85	0.85	2.37	2.53	2.78	2.66	2.37	2.53	2.78	2.66	ns
LVCMOS15, Fast, 6 mA	0.64	0.73	0.85	0.85	1.80	2.05	2.42	2.16	1.80	2.05	2.42	2.16	ns
LVCMOS15, Fast, 8 mA	0.64	0.73	0.85	0.85	1.76	1.90	2.11	2.04	1.76	1.90	2.11	2.04	ns
LVCMOS15, Fast, 12 mA	0.64	0.73	0.85	0.85	1.64	1.77	1.97	1.90	1.64	1.77	1.97	1.90	ns
LVCMOS15, Fast, 16 mA	0.64	0.73	0.85	0.85	1.62	1.76	1.96	1.92	1.62	1.76	1.96	1.92	ns
LVCMOS12, Slow, 2 mA	0.72	0.81	0.93	0.95	3.14	3.39	3.75	3.54	3.14	3.39	3.75	3.54	ns
LVCMOS12, Slow, 4 mA	0.72	0.81	0.93	0.95	2.43	2.63	2.93	2.79	2.43	2.63	2.93	2.79	ns
LVCMOS12, Slow, 6 mA	0.72	0.81	0.93	0.95	1.92	2.11	2.41	2.26	1.92	2.11	2.41	2.26	ns
LVCMOS12, Slow, 8 mA	0.72	0.81	0.93	0.95	1.87	2.02	2.25	2.17	1.87	2.02	2.25	2.17	ns
LVCMOS12, Fast, 2 mA	0.72	0.81	0.93	0.95	2.71	2.98	3.39	3.11	2.71	2.98	3.39	3.11	ns
LVCMOS12, Fast, 4 mA	0.72	0.81	0.93	0.95	1.93	2.16	2.51	2.31	1.93	2.16	2.51	2.31	ns
LVCMOS12, Fast, 6 mA	0.72	0.81	0.93	0.95	1.75	1.89	2.11	2.05	1.75	1.89	2.11	2.05	ns
LVCMOS12, Fast, 8 mA	0.72	0.81	0.93	0.95	1.69	1.82	2.02	1.98	1.69	1.82	2.02	1.98	ns
LVDCI_25	0.51	0.57	0.66	0.70	2.05	2.14	2.26	2.26	2.05	2.14	2.26	2.26	ns
LVDCI_18	0.55	0.61	0.71	0.73	2.07	2.23	2.47	2.38	2.07	2.23	2.47	2.38	ns
LVDCI_15	0.64	0.73	0.85	0.85	1.85	2.01	2.24	2.18	1.85	2.01	2.24	2.18	ns

Table 45: **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVDCI_DV2_18	0.61	0.72	0.73	1.81	2.36	1.98	1.81	2.36	1.98	ns
LVDCI_DV2_15	0.73	0.85	0.85	1.77	2.30	1.98	1.77	2.30	1.98	ns
LVPECL_25	0.94	1.09	1.08	1.49	2.68	1.64	1.49	2.68	1.64	ns
HSTL_I_12	0.91	1.06	1.06	1.60	2.48	1.74	1.60	2.48	1.74	ns
HSTL_I_DCI	0.91	1.06	1.06	1.50	2.43	1.64	1.50	2.43	1.64	ns
HSTL_II_DCI	0.91	1.06	1.06	1.49	2.39	1.66	1.49	2.39	1.66	ns
HSTL_II_T_DCI	0.91	1.06	1.06	1.50	2.43	1.64	1.50	2.43	1.64	ns
HSTL_III_DCI	0.91	1.06	1.06	1.45	2.48	1.61	1.45	2.48	1.61	ns
HSTL_I_DCI_18	0.91	1.06	1.06	1.53	2.44	1.66	1.53	2.44	1.66	ns
HSTL_II_DCI_18	0.91	1.06	1.06	1.46	2.41	1.59	1.46	2.41	1.59	ns
HSTL_II _T_DCI_18	0.91	1.06	1.06	1.53	2.43	1.66	1.53	2.43	1.66	ns
HSTL_III_DCI_18	0.91	1.06	1.06	1.54	2.50	1.67	1.54	2.50	1.67	ns
DIFF_HSTL_I_18	0.94	1.09	1.08	1.58	2.30	1.72	1.58	2.30	1.72	ns
DIFF_HSTL_I_DCI_18	0.94	1.09	1.08	1.53	2.21	1.66	1.53	2.21	1.66	ns
DIFF_HSTL_I	0.94	1.09	1.08	1.56	2.28	1.71	1.56	2.28	1.71	ns
DIFF_HSTL_I_DCI	0.94	1.09	1.08	1.50	2.28	1.64	1.50	2.28	1.64	ns
DIFF_HSTL_II_18	0.94	1.09	1.08	1.62	2.33	1.78	1.62	2.33	1.78	ns
DIFF_HSTL_II_DCI_18	0.94	1.09	1.08	1.46	2.18	1.59	1.46	2.18	1.59	ns
DIFF_HSTL_II _T_DCI_18	0.94	1.09	1.08	1.53	2.22	1.66	1.53	2.22	1.66	ns
DIFF_HSTL_II	0.94	1.09	1.08	1.56	2.29	1.72	1.56	2.29	1.72	ns
DIFF_HSTL_II_DCI	0.94	1.09	1.08	1.49	2.26	1.66	1.49	2.26	1.66	ns
SSTL2_I_DCI	0.91	1.06	1.06	1.53	2.51	1.68	1.53	2.51	1.68	ns
SSTL2_II_DCI	0.91	1.06	1.06	1.50	2.50	1.69	1.50	2.50	1.69	ns
SSTL2_II_T_DCI	0.91	1.06	1.06	1.53	2.52	1.68	1.53	2.52	1.68	ns
SSTL18_I	0.91	1.06	1.06	1.58	2.48	1.73	1.58	2.48	1.73	ns
SSTL18_II	0.91	1.06	1.06	1.50	2.46	1.66	1.50	2.46	1.66	ns
SSTL18_I_DCI	0.91	1.06	1.06	1.51	2.49	1.65	1.51	2.49	1.65	ns
SSTL18_II_DCI	0.91	1.06	1.06	1.47	2.41	1.62	1.47	2.41	1.62	ns
SSTL18_II_T_DCI	0.91	1.06	1.06	1.51	2.49	1.65	1.51	2.49	1.65	ns
SSTL15_T_DCI	0.91	1.06	1.06	1.52	2.48	1.66	1.52	2.48	1.66	ns
SSTL15_DCI	0.91	1.06	1.06	1.52	2.48	1.66	1.52	2.48	1.66	ns
DIFF_SSTL2_I	0.94	1.09	1.08	1.60	2.34	1.74	1.60	2.34	1.74	ns
DIFF_SSTL2_I_DCI	0.94	1.09	1.08	1.53	2.25	1.68	1.53	2.25	1.68	ns
DIFF_SSTL2_II	0.94	1.09	1.08	1.54	2.29	1.71	1.54	2.29	1.71	ns
DIFF_SSTL2_II_DCI	0.94	1.09	1.08	1.50	2.23	1.69	1.50	2.23	1.69	ns
DIFF_SSTL2_II_T_DCI	0.94	1.09	1.08	1.53	2.26	1.68	1.53	2.26	1.68	ns
DIFF_SSTL18_I	0.94	1.09	1.08	1.58	2.22	1.73	1.58	2.22	1.73	ns
DIFF_SSTL18_I_DCI	0.94	1.09	1.08	1.51	2.30	1.65	1.51	2.30	1.65	ns

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 55: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Sequential Delays						
T_{SHCKO}	Clock to A – B outputs	0.92	1.10	1.36	1.49	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	1.19	1.40	1.71	1.87	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{DS}/T_{DH}	A – D inputs to CLK	0.62/0.18	0.72/0.20	0.88/0.22	0.98/0.23	ns, Min
T_{AS}/T_{AH}	Address An inputs to clock	0.19/0.52	0.22/0.59	0.27/0.66	0.30/0.75	ns, Min
T_{WS}/T_{WH}	WE input to clock	0.27/0.00	0.32/0.00	0.40/0.00	0.47/–0.03	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.28/–0.01	0.34/–0.01	0.41/–0.01	0.48/–0.05	ns, Min
Clock CLK						
T_{MPW}	Minimum pulse width	0.70	0.82	1.00	1.04	ns, Min
T_{MCP}	Minimum clock period	1.40	1.64	2.00	2.08	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 56: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Sequential Delays						
T_{REG}	Clock to A – D outputs	1.11	1.30	1.58	1.74	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.37	1.60	1.93	2.12	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	1.08	1.27	1.55	1.74	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{WS}/T_{WH}	WE input	0.05/0.00	0.07/0.00	0.09/0.00	0.11/0.03	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.06/–0.01	0.08/–0.01	0.10/–0.01	0.12/0.02	ns, Min
T_{DS}/T_{DH}	A – D inputs to CLK	0.64/0.18	0.76/0.21	0.94/0.24	1.07/0.23	ns, Min
Clock CLK						
T_{MPW}	Minimum pulse width	0.60	0.70	0.85	0.89	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Table 57: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{RCCK_WE}/T_{RCKC_WE}	Write Enable (WE) input (Block RAM only)	0.44/ 0.19	0.47/ 0.25	0.52/ 0.35	0.67/ 0.24	ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN FIFO inputs	0.47/ 0.26	0.50/ 0.27	0.55/ 0.30	0.68/ 0.31	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	RDEN FIFO inputs	0.46/ 0.26	0.50/ 0.27	0.55/ 0.30	0.67/ 0.31	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers(10)	0.90	0.98	1.10	1.23	ns, Max
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	FIFO reset timing(11)	0.22/ 0.23	0.24/ 0.24	0.28/ 0.26	0.31/ 0.27	ns, Min
Maximum Frequency						
F_{MAX}	Block RAM in TDP and SDP modes (Write First and No Change modes)	600	540	450	340	MHz
	Block RAM (Read First mode)	525	475	400	275	MHz
	Block RAM (SDP mode)(12)	525	475	400	275	MHz
$F_{MAX\_CASCADE}$	Block RAM Cascade (Write First and No Change modes)	550	490	400	300	MHz
	Block RAM Cascade (Read First mode)	475	425	350	235	MHz
F_{MAX_FIFO}	FIFO in all modes	600	540	450	340	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	450	400	325	250	MHz

Notes:

1. TRACE will report all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. The FIFO reset must be asserted for at least three positive clock edges.
12. When using ISE software v12.4 or later, if the RDADDR_COLLISION_HWCONFIG attribute is set to PERFORMANCE or the block RAM is in single-port operation, then the faster F_{MAX} for WRITE_FIRST/NO_CHANGE modes apply.

Table 59: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$	DI Setup/Hold	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$	DEN Setup/Hold time	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$	DWE Setup/Hold time	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{MMCMCKO\_DO}$	CLK to out of DO(3)	2.60	3.02	3.64	3.68	ns
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY	0.32	0.34	0.38	0.38	ns

Notes:

1. To support longer delays in configuration, use the design solutions described in UG360: *Virtex-6 FPGA Configuration User Guide*.
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
3. DO will hold until next DRP operation.

Clock Buffers and Networks

Table 60: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-2	-1	-1L	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins Setup/Hold	All	0.11/ 0.00	0.13/ 0.00	0.16/ 0.00	0.13/ 0.00	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins Setup/Hold	All	0.11/ 0.00	0.13/ 0.00	0.16/ 0.00	0.13/ 0.00	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	All	0.07	0.08	0.10	0.10	ns
Maximum Frequency							
F_{MAX}	Global clock tree (BUFG)	All except LX760	800	750	700	667	MHz
		LX760	N/A	700	700	667	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 61: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BIOCKO_O}	Clock to out delay from I to O	0.14	0.16	0.18	0.21	ns
Maximum Frequency						
F_{MAX}	I/O clock tree (BUFIO)	800	800	710	710	MHz

Table 62: **Regional Clock Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BRCKO_O}	Clock to out delay from I to O	0.56	0.62	0.73	0.82	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.28	0.31	0.36	0.41	ns

Virtex-6 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 65. Values are expressed in nanoseconds unless otherwise noted.

Table 65: **Global Clock Input to Output Delay Without MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* MMCM.							
T_{ICKOF}	Global Clock input and OUTFF *without* MMCM	XC6VLX75T	4.91	5.32	5.88	6.02	ns
		XC6VLX130T	4.89	5.33	6.00	6.13	ns
		XC6VLX195T	5.02	5.46	6.13	6.27	ns
		XC6VLX240T	5.02	5.46	6.13	6.27	ns
		XC6VLX365T	5.30	5.75	6.43	6.37	ns
		XC6VLX550T	N/A	6.02	6.72	6.60	ns
		XC6VLX760	N/A	6.26	6.97	6.87	ns
		XC6VSX315T	5.40	5.85	6.54	6.49	ns
		XC6VSX475T	N/A	6.01	6.71	6.61	ns
		XC6VHX250T	5.18	5.63	6.30	N/A	ns
		XC6VHX255T	5.20	5.66	6.34	N/A	ns
		XC6VHX380T	5.38	5.84	6.53	N/A	ns
		XC6VHX565T	N/A	6.03	6.71	N/A	ns
		XQ6VLX130T	N/A	5.33	6.00	6.13	ns
		XQ6VLX240T	N/A	5.46	6.13	6.27	ns
		XQ6VLX550T	N/A	N/A	6.72	6.60	ns
		XQ6VSX315T	N/A	5.85	6.54	6.49	ns
		XQ6VSX475T	N/A	N/A	6.71	6.61	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 70: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard.(1)							
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No Delay Clock-capable Clock Input and IFF(2) with MMCM	XC6VLX75T	1.56/ –0.25	1.69/ –0.25	1.86/ –0.25	1.91/ –0.15	ns
		XC6VLX130T	1.64/ –0.25	1.78/ –0.25	1.95/ –0.25	2.00/ –0.14	ns
		XC6VLX195T	1.65/ –0.24	1.79/ –0.24	1.96/ –0.24	2.01/ –0.15	ns
		XC6VLX240T	1.65/ –0.24	1.79/ –0.24	1.96/ –0.24	2.01/ –0.15	ns
		XC6VLX365T	1.66/ –0.25	1.79/ –0.25	1.97/ –0.25	2.02/ –0.15	ns
		XC6VLX550T	N/A	1.97/ –0.24	2.16/ –0.24	2.19/ –0.14	ns
		XC6VLX760	N/A	2.39/ –0.20	2.63/ –0.20	2.21/ –0.10	ns
		XC6VSX315T	1.67/ –0.25	1.80/ –0.25	1.98/ –0.25	2.03/ –0.16	ns
		XC6VSX475T	N/A	1.98/ –0.29	2.17/ –0.29	2.21/ –0.20	ns
		XC6VHX250T	1.63/ –0.24	1.76/ –0.24	1.94/ –0.24	N/A	ns
		XC6VHX255T	1.63/ –0.19	1.76/ –0.19	1.99/ –0.19	N/A	ns
		XC6VHX380T	1.80/ –0.23	1.94/ –0.23	2.13/ –0.23	N/A	ns
		XC6VHX565T	N/A	1.94/ –0.08	2.13/ –0.08	N/A	ns
		XQ6VLX130T	N/A	1.78/ –0.25	1.95/ –0.25	2.00/ –0.14	ns
		XQ6VLX240T	N/A	1.79/ –0.24	1.96/ –0.24	2.01/ –0.15	ns
		XQ6VLX550T	N/A	N/A	2.16/ –0.24	2.19/ –0.14	ns
		XQ6VSX315T	N/A	1.80/ –0.25	1.98/ –0.25	2.03/ –0.16	ns
		XQ6VSX475T	N/A	N/A	2.17/ –0.29	2.21/ –0.20	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 FPGA clock transmitter and receiver data-valid windows.

Table 71: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion(1)	All	0.12	0.12	0.12	0.12	ns
T_{CKSKEW}	Global Clock Tree Skew(2)	XC6VLX75T	0.15	0.16	0.18	0.17	ns
		XC6VLX130T	0.25	0.26	0.29	0.28	ns
		XC6VLX195T	0.26	0.27	0.31	0.30	ns
		XC6VLX240T	0.26	0.27	0.31	0.30	ns
		XC6VLX365T	0.28	0.29	0.31	0.31	ns
		XC6VLX550T	N/A	0.50	0.54	0.54	ns
		XC6VLX760	N/A	0.51	0.56	0.56	ns
		XC6VSX315T	0.27	0.28	0.32	0.30	ns
		XC6VSX475T	N/A	0.39	0.44	0.42	ns
		XC6VHX250T	0.25	0.26	0.29	N/A	ns
		XC6VHX255T	0.35	0.37	0.41	N/A	ns
		XC6VHX380T	0.45	0.47	0.52	N/A	ns
		XC6VHX565T	N/A	0.46	0.51	N/A	ns
		XQ6VLX130T	N/A	0.26	0.29	0.28	ns
		XQ6VLX240T	N/A	0.27	0.31	0.30	ns
		XQ6VLX550T	N/A	N/A	0.54	0.54	ns
		XQ6VSX315T	N/A	0.28	0.32	0.30	ns
		XQ6VSX475T	N/A	N/A	0.44	0.42	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.08	0.08	0.08	0.08	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	0.02	ns
$T_{BUFIOSKEW2}$	I/O clock tree skew across three clock regions	All	0.10	0.12	0.23	0.12	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 72: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC6VLX75T	FF484	95	ps
			FF784	146	ps
		XC6VLX130T	FF484	95	ps
			FF784	146	ps
			FF1156	165	ps
		XC6VLX195T	FF784	145	ps
			FF1156	182	ps
		XC6VLX240T	FF784	146	ps
			FF1156	182	ps
			FF1759	187	ps
		XC6VLX365T	FF1156	189	ps
			FF1759	184	ps
		XC6VLX550T	FF1759	196	ps
			FF1760	249	ps
		XC6VLX760	FF1760	236	ps
		XC6VSX315T	FF1156	168	ps
			FF1759	190	ps
		XC6VSX475T	FF1156	168	ps
			FF1759	204	ps
		XC6VHX250T	FF1154	166	ps
		XC6VHX255T	FF1155	168	ps
			FF1923	228	ps
		XC6VHX380T	FF1154	159	ps
			FF1155	172	ps
			FF1923	227	ps
			FF1924	220	ps
		XC6VHX565T	FF1923	232	ps
			FF1924	197	ps
		XQ6VLX130T	RF784	146	ps
			RF1156	165	ps
			FFG1156	165	ps
		XQ6VLX240T	RF784	146	ps
			RF1156	182	ps
			FFG1156	182	ps
			RF1759	187	ps
		XQ6VLX550T	RF1759	196	ps
		XQ6VSX315T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	190	ps
		XQ6VSX475T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	204	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Date	Version	Description of Revisions
01/18/10	2.1	Changed absolute maximum ratings for both V_{IN} and V_{TS} in Table 1. Added data to Table 3. Added data to Table 5. Updated SSTL15 in Table 7. Updated V_{OCM} and V_{OD} values in Table 8. Added eFUSE endurance Table 12. Added values to $V_{MGTREFCLK}$ and V_{IN} in Table 13, page 11. Added values and updated tables in the GTX Transceiver Specifications and GTH Transceiver Specifications sections. Added Table 27 and Figure 4. Revised parameters and values in Table 39. Updated Table 40, page 23. Added data to Table 41. Updated speed specification to v1.04 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX240T for -1 and -2 speed grades. Speed specification changes and numerous updates also made to Table 44, and Table 49 through Table 71. Added data to Table 73 and Table 74.
02/09/10	2.2	Revised description of C_{IN} in Table 3. Clarified values in Table 5. Fixed SDR LVDS unit error in Table 41.
04/12/10	2.3	Added note 3 and update value of *n* in Table 3. Clarified simultaneous power-down in Power-On Power Supply Requirements. Updated external reference junction temperatures in Table 40, Analog-to-Digital Specifications. Updated speed specification to v1.05 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX130T for -1 and -2 speed grades. Fixed note 4 in Table 48. Increased the -2 specification for $F_{IDELAYCTRL\_REF}$ and clarified units for $T_{IDELAYPAT\_JIT}$ in Table 53. Added note 1 to Table 62.
05/11/10	2.4	Updated F_{RXREC} in Table 22. Revised $F_{IDELAYCTRL\_REF}$ in Table 53. Removed $T_{RCKO\_PARITY\_ECC}$: Clock CLK to ECCPARITY in standard ECC mode row in Table 57. Added XC6VLX130T values to Table 72.
05/26/10	2.5	Added XC6VLX195T data to Table 5. Updated values in Table 22 including adding note 2 and note 3. Updated speed specification to v1.06 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX195T for -1 and -2 speed grades. Added XC6VLX195T values to Table 72.
07/16/10	2.6	Changed Table 42 and Table 43 to production status on the -3 speed grade XC6VLX130T, XC6VLX195T, and XC6VLX240T devices. Added XC6VHX250Tdata to Table 4 and Table 72. Added Note 6 to Table 64.
07/23/10	2.7	Changed Table 42 and Table 43 to production status on the XC6VLX75T, XC6VLX365T, XC6VLX550T, XC6VLX760, XC6VSX315T, and XC6VSX475T devices using ISE 12.2 software with speed specification v1.08. Updated $V_{CMOUTDC}$ equation to MGTAVTT – D_{VPPOUT}/4 in Table 17. Updated some -3, -2, -1 specifications in Table 65 through Table 72. Added and updated -1L specifications to Table 41 and for most switching characteristics tables.
07/30/10	2.8	Changed Table 42 and Table 43 to production status on the -1L speed grade for the XC6VLX130T, XC6VLX195T, XC6VLX240T, XC6VLX365T, and XC6VLX550T devices using ISE 12.2 software with current speed specifications. Also updated the speed specifications for XC6VLX75T, XC6VLX550T, and XC6VSX315T. Updated V_{CCINT} specifications for -1L speed grade industrial temperature range devices in Table 2.
09/20/10	2.9	In Table 32, changed $F_{GPLLMAX}$ specification in -3 column from 5.951 to 5.591. In Table 40, changed F_{MAX} for the DCLK from 250 MHz to 80 MHz.
10/18/10	2.10	The specification change in version 2.9, Table 40 is described in XCN10032, *Virtex-6 FPGA: GTX Transceiver User Guide, Family Data Sheet (SYSMON DCLK), and JTAG ID Changes* In this version (2.10), -1L(I) data is added to Table 4 and clarified in Note 2. Changed Table 42 and Table 43 to production status on the -1L speed grade XC6VLX75T, XC6VLX760, XC6VSX315T, and XC6VSX475T devices using ISE 12.3 software with current speed specifications. Revised the XC6VLX760 -1L speed specification for $T_{PHMMCMGC}$ in Table 69 and $T_{PHMMCMCC}$ in Table 70.
01/17/11	2.11	Changed in Table 42 and Table 43 to production status on the XC6VHX250T devices using ISE 12.4 software with current speed specifications. Added industrial temperature range (T_j) recommended specifications to Table 2; including specific ranges for the -2I XC6VSX475T, XC6VLX550T, XC6VLX760, and XC6VHX565Tdevices. Added note 3 to Table 36 and maximum total jitter values. Added note 4 to Table 37 and maximum sinusoidal jitter values. Added note 2 to Table 43. Revised F_{MAX} descriptions in Table 57 and added note 12. Added note 8 to F_{PFDMIN} in Table 64. The following revisions are due to specification changes as described in XCN11009, *Virtex-6 FPGA: Data Sheet, User Guides, and JTAG ID Updates*. In Table 59:*Configuration Switching Characteristics*, page 49, revised -1L specifications for T_{POR}, F_{MCCK}, $F_{MCCKTOL}$, $T_{SMCSCCK}$, T_{SMCCKW}, F_{RBCCK}, F_{TCK}, F_{TCKB}, T_{MCCKL}, and T_{MCCKH}. In Table 64: *MMCM Specification*, added bandwidth settings to F_{PFDMIN} and added note 1.