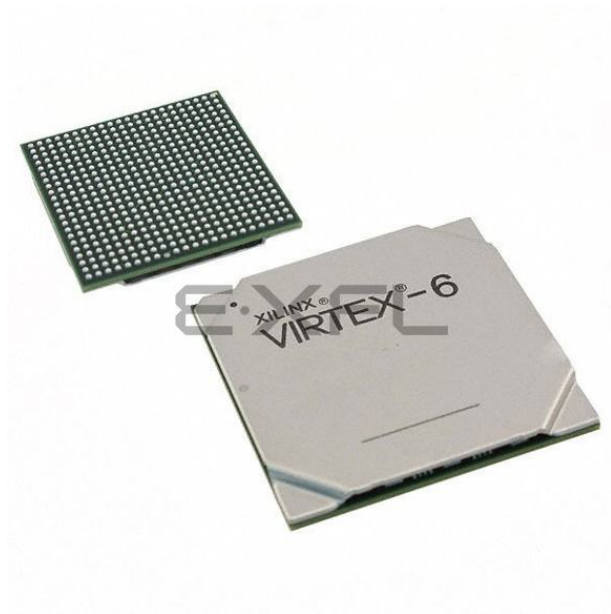




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	5820
Number of Logic Elements/Cells	74496
Total RAM Bits	5750784
Number of I/O	240
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA, FCBGA
Supplier Device Package	484-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vlx75t-3ff484c

Table 21: GTX Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		62.5	–	650	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	200	μ s

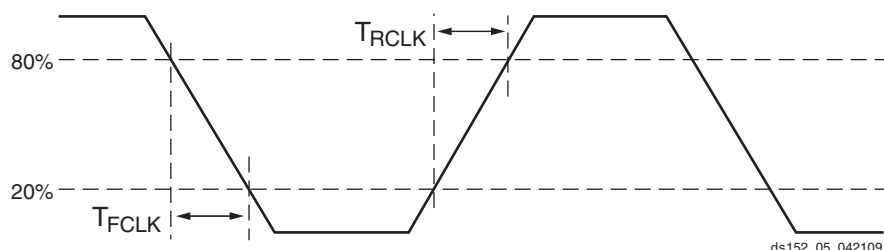


Figure 3: Reference Clock Timing Parameters

Table 22: GTX Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1	-1L	
F_{TXOUT}	TXOUTCLK maximum frequency	Internal 20-bit data path	330	330	250	250	MHz
		Internal 16-bit data path	412.5	412.5	312.5	250	MHz
F_{RXREC}	RXRECCLK maximum frequency	Internal 20-bit data path	330	330	250	250	MHz
		Internal 16-bit data path	412.5	412.5	312.5	250	MHz
T_{RX}	RXUSRCLK maximum frequency		412.5 ⁽²⁾	412.5 ⁽²⁾	312.5	250	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	376	376	312.5	250	MHz
		2 byte interface	406.25	406.25	312.5	250	MHz
		4 byte interface	206.25	206.25	156.25	125	MHz
T_{TX}	TXUSRCLK maximum frequency		412.5 ⁽³⁾	412.5 ⁽³⁾	312.5	250	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	376	376	312.5	250	MHz
		2 byte interface	406.25	406.25	312.5	250	MHz
		4 byte interface	206.25	206.25	156.25	125	MHz

Notes:

1. Clocking must be implemented as described in [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#).
2. 406.25 MHz when the RX elastic buffer is bypassed.
3. 406.25 MHz when the TX buffer is bypassed.

GTH Transceiver DC Input and Output Levels

Table 30 summarizes the DC output specifications of the GTH transceivers in Virtex-6 FPGAs. Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further details.

Table 30: GTH Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
D_{VPPIN}	Differential peak-to-peak input voltage	External AC coupled	175	–	1200	mV
D_{VPPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	800	–	1200	mV
R_{IN}	Differential input resistance		80	100	120	Ω
R_{OUT}	Differential output resistance		80	100	120	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	–	ps
C_{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 31 summarizes the DC specifications of the clock input of the GTH transceiver. Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further details.

Table 31: GTH Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	≤ 600 MHz	500	–	1600	mV
		> 600 MHz	600	–	1600	mV
R_{IN}	Differential input resistance		80	100	120	Ω
C_{EXT}	Required external AC coupling capacitor		–	100	–	nF

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 39: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F _{PIPECLK}	Pipe clock maximum frequency	250	250	250	250	MHz
F _{USERCLK}	User clock maximum frequency	500	500	250	250	MHz
F _{DRPCLK}	DRP clock maximum frequency	250	250	250	250	MHz

System Monitor Analog-to-Digital Converter Specification

Table 40: Analog-to-Digital Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
AV _{DD} = 2.5V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 5.2 MHz, T _j = -55°C to 125°C M-Grade, Typical values at T _j = +35°C						
DC Accuracy: All external input channels. Both unipolar and bipolar modes.						
Resolution			10	—	—	Bits
Integral Nonlinearity	INL		—	—	±1	LSBs
Differential Nonlinearity	DNL	No missing codes (T _{MIN} to T _{MAX}) Guaranteed Monotonic	—	—	±0.9	LSBs
Unipolar Offset Error ⁽¹⁾		Uncalibrated	—	±2	±30	LSBs
Bipolar Offset Error ⁽¹⁾		Uncalibrated measured in bipolar mode	—	±2	±30	LSBs
Gain Error		Uncalibrated - External Reference	—	±0.2	±2	%
		Uncalibrated - Internal Reference	—	±2	—	%
Bipolar Gain Error ⁽¹⁾		Uncalibrated - External Reference	—	±0.2	±2	%
		Uncalibrated - Internal Reference	—	±2	—	%
Total Unadjusted Error (Uncalibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	—	±10	—	LSBs
		Deviation from ideal transfer function. Internal reference	—	±20	—	LSBs
Total Unadjusted Error (Calibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	—	±1	±2	LSBs
Calibrated Gain Temperature Coefficient		Variation of FS code with temperature	—	±0.01	—	LSB/°C
DC Common-Mode Reject	CMRR _{DC}	V _N = V _{CM} = 0.5V ± 0.5V, V _P - V _N = 100mV	—	70	—	dB
Conversion Rate ⁽²⁾						
Conversion Time - Continuous	t _{CONV}	Number of CLK cycles	26	—	32	
Conversion Time - Event	t _{CONV}	Number of CLK cycles	—	—	21	
T/H Acquisition Time	t _{ACQ}	Number of CLK cycles	4	—	—	
DRP Clock Frequency	DCLK	DRP clock frequency	8	—	80	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	—	5.2	MHz
CLK Duty cycle			40	—	60	%

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [Switching Characteristics, page 26](#).

Table 41: Interface Performances

Description	Speed Grade			
	-3	-2	-1	-1L
Networking Applications				
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	710 Mb/s	710 Mb/s	650 Mb/s	585 Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 10)	1.4 Gb/s	1.3 Gb/s	1.25 Gb/s	1.1 Gb/s
SDR LVDS receiver (SFI-4.1) ⁽¹⁾	710 Mb/s	710 Mb/s	650 Mb/s	585 Mb/s
DDR LVDS receiver (SPI-4.2) ⁽¹⁾	1.4 Gb/s	1.3 Gb/s	1.1 Gb/s	0.9 Gb/s
Maximum Physical Interface (PHY) Rate for Memory Interfaces⁽²⁾⁽³⁾⁽⁴⁾				
DDR2	800 Mb/s	800 Mb/s	800 Mb/s	606 Mb/s
DDR3	1066 Mb/s	1066 Mb/s	800 Mb/s	800 Mb/s
QDR II + SRAM	400 MHz	350 MHz	300 MHz	—
RLDRAM II	500 MHz	400 MHz	350 MHz	—

Notes:

1. LVDS receivers are typically bounded with certain applications where specific DPA algorithms dominate deterministic performance.
2. Verified on Xilinx memory characterization platforms designed according to the guidelines in UG: *Virtex-6 FPGA Memory Interface Solutions User Guide*.
3. Consult [DS186](#); *Virtex-6 FPGA Memory Interface Solutions Data Sheet* for performance and feature information on memory interface cores (controller plus PHY).
4. Memory Interface data rates have not been tested over the junction temperature operating range for military (M) temperature devices. Customers are responsible for specifying and testing their specific M temperature grade memory implementation.

Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.17 for -3, -2, and -1; and v1.10 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

[Table 42](#) correlates the current status of each Virtex-6 device on a per speed grade basis.

Table 42: Virtex-6 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6VLX75T			-3, -2, -1, -1L
XC6VLX130T			-3, -2, -1, -1L
XC6VLX195T			-3, -2, -1, -1L
XC6VLX240T			-3, -2, -1, -1L
XC6VLX365T			-3, -2, -1, -1L
XC6VLX550T			-2, -1, -1L
XC6VLX760			-2, -1, -1L
XC6VSX315T			-3, -2, -1, -1L
XC6VSX475T			-2, -1, -1L
XC6VHX250T			-3, -2, -1
XC6VHX255T			-3, -2, -1
XC6VHX380T			-3, -2, -1
XC6VHX565T			-2, -1
XQ6VLX130T			-2, -1, -1L
XQ6VLX240T			-2, -1, -1L
XQ6VLX550T			-1, -1L
XQ6VSX315T			-2, -1, -1L
XQ6VSX475T			-1, -1L

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 devices.

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVC MOS25, Fast, 24 mA	0.51	0.57	0.66	0.70	1.66	1.79	1.99	1.96	1.66	1.79	1.99	1.96	ns
LVC MOS18, Slow, 2 mA	0.55	0.61	0.71	0.73	4.21	4.47	4.87	4.30	4.21	4.47	4.87	4.30	ns
LVC MOS18, Slow, 4 mA	0.55	0.61	0.71	0.73	2.79	2.96	3.21	2.94	2.79	2.96	3.21	2.94	ns
LVC MOS18, Slow, 6 mA	0.55	0.61	0.71	0.73	2.30	2.43	2.64	2.47	2.30	2.43	2.64	2.47	ns
LVC MOS18, Slow, 8 mA	0.55	0.61	0.71	0.73	2.01	2.11	2.27	2.24	2.01	2.11	2.27	2.24	ns
LVC MOS18, Slow, 12 mA	0.55	0.61	0.71	0.73	1.88	1.99	2.15	2.10	1.88	1.99	2.15	2.10	ns
LVC MOS18, Slow, 16 mA	0.55	0.61	0.71	0.73	1.84	1.95	2.11	2.04	1.84	1.95	2.11	2.04	ns
LVC MOS18, Fast, 2 mA	0.55	0.61	0.71	0.73	4.00	4.23	4.57	4.08	4.00	4.23	4.57	4.08	ns
LVC MOS18, Fast, 4 mA	0.55	0.61	0.71	0.73	2.62	2.76	2.97	2.74	2.62	2.76	2.97	2.74	ns
LVC MOS18, Fast, 6 mA	0.55	0.61	0.71	0.73	2.15	2.28	2.46	2.32	2.15	2.28	2.46	2.32	ns
LVC MOS18, Fast, 8 mA	0.55	0.61	0.71	0.73	1.90	1.99	2.13	2.14	1.90	1.99	2.13	2.14	ns
LVC MOS18, Fast, 12 mA	0.55	0.61	0.71	0.73	1.69	1.80	1.97	1.88	1.69	1.80	1.97	1.88	ns
LVC MOS18, Fast, 16 mA	0.55	0.61	0.71	0.73	1.63	1.74	1.91	1.88	1.63	1.74	1.91	1.88	ns
LVC MOS15, Slow, 2 mA	0.64	0.73	0.85	0.85	3.43	3.77	4.29	3.91	3.43	3.77	4.29	3.91	ns
LVC MOS15, Slow, 4 mA	0.64	0.73	0.85	0.85	2.58	2.79	3.10	2.93	2.58	2.79	3.10	2.93	ns
LVC MOS15, Slow, 6 mA	0.64	0.73	0.85	0.85	2.08	2.32	2.68	2.50	2.08	2.32	2.68	2.50	ns
LVC MOS15, Slow, 8 mA	0.64	0.73	0.85	0.85	1.81	1.98	2.23	2.24	1.81	1.98	2.23	2.24	ns
LVC MOS15, Slow, 12 mA	0.64	0.73	0.85	0.85	1.76	1.91	2.13	2.07	1.76	1.91	2.13	2.07	ns
LVC MOS15, Slow, 16 mA	0.64	0.73	0.85	0.85	1.69	1.83	2.04	1.98	1.69	1.83	2.04	1.98	ns
LVC MOS15, Fast, 2 mA	0.64	0.73	0.85	0.85	3.44	3.77	4.28	3.91	3.44	3.77	4.28	3.91	ns
LVC MOS15, Fast, 4 mA	0.64	0.73	0.85	0.85	2.37	2.53	2.78	2.66	2.37	2.53	2.78	2.66	ns
LVC MOS15, Fast, 6 mA	0.64	0.73	0.85	0.85	1.80	2.05	2.42	2.16	1.80	2.05	2.42	2.16	ns
LVC MOS15, Fast, 8 mA	0.64	0.73	0.85	0.85	1.76	1.90	2.11	2.04	1.76	1.90	2.11	2.04	ns
LVC MOS15, Fast, 12 mA	0.64	0.73	0.85	0.85	1.64	1.77	1.97	1.90	1.64	1.77	1.97	1.90	ns
LVC MOS15, Fast, 16 mA	0.64	0.73	0.85	0.85	1.62	1.76	1.96	1.92	1.62	1.76	1.96	1.92	ns
LVC MOS12, Slow, 2 mA	0.72	0.81	0.93	0.95	3.14	3.39	3.75	3.54	3.14	3.39	3.75	3.54	ns
LVC MOS12, Slow, 4 mA	0.72	0.81	0.93	0.95	2.43	2.63	2.93	2.79	2.43	2.63	2.93	2.79	ns
LVC MOS12, Slow, 6 mA	0.72	0.81	0.93	0.95	1.92	2.11	2.41	2.26	1.92	2.11	2.41	2.26	ns
LVC MOS12, Slow, 8 mA	0.72	0.81	0.93	0.95	1.87	2.02	2.25	2.17	1.87	2.02	2.25	2.17	ns
LVC MOS12, Fast, 2 mA	0.72	0.81	0.93	0.95	2.71	2.98	3.39	3.11	2.71	2.98	3.39	3.11	ns
LVC MOS12, Fast, 4 mA	0.72	0.81	0.93	0.95	1.93	2.16	2.51	2.31	1.93	2.16	2.51	2.31	ns
LVC MOS12, Fast, 6 mA	0.72	0.81	0.93	0.95	1.75	1.89	2.11	2.05	1.75	1.89	2.11	2.05	ns
LVC MOS12, Fast, 8 mA	0.72	0.81	0.93	0.95	1.69	1.82	2.02	1.98	1.69	1.82	2.02	1.98	ns
LVDCI_25	0.51	0.57	0.66	0.70	2.05	2.14	2.26	2.26	2.05	2.14	2.26	2.26	ns
LVDCI_18	0.55	0.61	0.71	0.73	2.07	2.23	2.47	2.38	2.07	2.23	2.47	2.38	ns
LVDCI_15	0.64	0.73	0.85	0.85	1.85	2.01	2.24	2.18	1.85	2.01	2.24	2.18	ns

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
DIFF_SSTL18_I	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
DIFF_SSTL18_I_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL18_II	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
DIFF_SSTL18_II_DCI	0.85	0.94	1.09	1.08	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
DIFF_SSTL18_II_T_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
DIFF_SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVDS_25	0.94	1.09	1.08	1.54	2.16	1.62	1.54	2.16	1.62	ns
LVDSEXT_25	0.94	1.09	1.08	1.65	2.20	1.73	1.65	2.20	1.73	ns
HT_25	0.94	1.09	1.08	1.62	2.20	1.69	1.62	2.20	1.69	ns
BLVDS_25	0.94	1.09	1.08	1.50	3.18	1.65	1.50	3.18	1.65	ns
RSDS_25 (point to point)	0.94	1.09	1.08	1.54	2.22	1.62	1.54	2.22	1.62	ns
HSTL_I	0.91	1.06	1.06	1.56	2.44	1.71	1.56	2.44	1.71	ns
HSTL_II	0.91	1.06	1.06	1.56	2.21	1.72	1.56	2.21	1.72	ns
HSTL_III	0.91	1.06	1.06	1.54	2.50	1.69	1.54	2.50	1.69	ns
HSTL_I_18	0.91	1.06	1.06	1.58	2.43	1.72	1.58	2.43	1.72	ns
HSTL_II_18	0.91	1.06	1.06	1.62	2.30	1.78	1.62	2.30	1.78	ns
HSTL_III_18	0.91	1.06	1.06	1.54	2.49	1.69	1.54	2.49	1.69	ns
SSTL2_I	0.91	1.06	1.06	1.60	2.50	1.74	1.60	2.50	1.74	ns
SSTL2_II	0.91	1.06	1.06	1.54	2.49	1.71	1.54	2.49	1.71	ns
SSTL15	0.91	1.06	1.06	1.54	2.07	1.69	1.54	2.07	1.69	ns
LVC MOS25, Slow, 2 mA	0.57	0.66	0.70	5.46	6.01	5.63	5.46	6.01	5.63	ns
LVC MOS25, Slow, 4 mA	0.57	0.66	0.70	3.49	3.79	3.65	3.49	3.79	3.65	ns
LVC MOS25, Slow, 6 mA	0.57	0.66	0.70	2.81	3.08	2.95	2.81	3.08	2.95	ns
LVC MOS25, Slow, 8 mA	0.57	0.66	0.70	2.41	2.72	2.59	2.41	2.72	2.59	ns
LVC MOS25, Slow, 12 mA	0.57	0.66	0.70	1.95	2.23	2.10	1.95	2.23	2.10	ns
LVC MOS25, Slow, 16 mA	0.57	0.66	0.70	2.05	2.29	2.21	2.05	2.29	2.21	ns
LVC MOS25, Slow, 24 mA	0.57	0.66	0.70	1.82	2.24	1.98	1.82	2.24	1.98	ns
LVC MOS25, Fast, 2 mA	0.57	0.66	0.70	5.49	6.04	5.62	5.49	6.04	5.62	ns
LVC MOS25, Fast, 4 mA	0.57	0.66	0.70	3.50	3.82	3.65	3.50	3.82	3.65	ns
LVC MOS25, Fast, 6 mA	0.57	0.66	0.70	2.73	2.99	2.88	2.73	2.99	2.88	ns
LVC MOS25, Fast, 8 mA	0.57	0.66	0.70	2.33	2.65	2.53	2.33	2.65	2.53	ns
LVC MOS25, Fast, 12 mA	0.57	0.66	0.70	1.88	2.08	2.03	1.88	2.08	2.03	ns

Table 48: Output Delay Measurement Methodology (Cont'd)

Description	I/O Standard Attribute	R _{REF} (Ω)	C _{REF} ⁽¹⁾ (pF)	V _{MEAS} (V)	V _{REF} (V)
HT (HyperTransport), 2.5V	LDT_25	100	0	0 ⁽²⁾	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	100	0	0 ⁽²⁾	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V _{REF}	0.75
HSTL, Class III, with DCI	HSTL_III_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V _{REF}	0.9
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termini.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V _{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V _{REF}	1.25

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 49: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Setup/Hold						
T _{ICE1CK} /T _{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.21/ 0.03	0.25/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T _{ISRCK} /T _{ICKSR}	SR pin Setup/Hold with respect to CLK	0.66/ −0.08	0.78/ −0.08	0.96/ −0.08	1.09/ −0.11	ns
T _{IDOCK} /T _{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.07/ 0.41	0.08/ 0.46	0.10/ 0.54	0.11/ 0.64	ns
T _{IDOCKD} /T _{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.10/ 0.32	0.12/ 0.36	0.14/ 0.42	0.16/ 0.50	ns
Combinatorial						
T _{IDI}	D pin to O pin propagation delay, no Delay	0.15	0.17	0.20	0.23	ns
T _{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.19	0.22	0.25	0.28	ns
Sequential Delays						
T _{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.48	0.54	0.64	0.73	ns
T _{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.52	0.58	0.68	0.78	ns
T _{ICKQ}	CLK to Q outputs	0.54	0.61	0.70	0.93	ns
T _{RQ_ILOGIC}	SR pin to OQ/TQ out	0.85	0.97	1.15	1.32	ns
T _{GSRQ_ILOGIC}	Global Set/Reset to Q outputs	7.60	7.60	10.51	10.51	ns
Set/Reset						
T _{RPW_ILOGIC}	Minimum Pulse Width, SR inputs	0.78	0.95	1.20	1.30	ns, Min

Block RAM and FIFO Switching Characteristics

Table 57: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Block RAM and FIFO Clock-to-Out Delays						
T _{RCKO_DO} and T _{RCKO_DO_REG} ⁽¹⁾	Clock CLK to DOUT output (without output register) ⁽²⁾⁽³⁾	1.60	1.79	2.08	2.36	ns, Max
	Clock CLK to DOUT output (with output register) ⁽⁴⁾⁽⁵⁾	0.60	0.66	0.75	0.83	ns, Max
T _{RCKO_DO_ECC} and T _{RCKO_DO_ECC_REG}	Clock CLK to DOUT output with ECC (without output register) ⁽²⁾⁽³⁾	2.62	2.89	3.30	3.73	ns, Max
	Clock CLK to DOUT output with ECC (with output register) ⁽⁴⁾⁽⁵⁾	0.71	0.77	0.86	0.94	ns, Max
T _{RCKO_CASC} and T _{RCKO_CASC_REG}	Clock CLK to DOUT output with Cascade (without output register) ⁽²⁾	2.49	2.77	3.18	3.61	ns, Max
	Clock CLK to DOUT output with Cascade (with output register) ⁽⁴⁾	1.29	1.41	1.58	1.79	ns, Max
T _{RCKO_FLAGS}	Clock CLK to FIFO flags outputs ⁽⁶⁾	0.74	0.81	0.91	0.98	ns, Max
T _{RCKO_POINTERS}	Clock CLK to FIFO pointers outputs ⁽⁷⁾	0.90	0.98	1.09	1.21	ns, Max
T _{RCKO_SDBIT_ECC} and T _{RCKO_SDBIT_ECC_REG}	Clock CLK to BITERR (with output register)	0.62	0.68	0.76	0.82	ns, Max
	Clock CLK to BITERR (without output register)	2.21	2.46	2.84	3.23	ns, Max
T _{RCKO_PARITY_ECC}	Clock CLK to ECCPARITY in ECC encode only mode	0.86	0.94	1.06	1.18	ns, Max
T _{RCKO_RDADDR_ECC} and T _{RCKO_RDADDR_ECC_REG}	Clock CLK to RDADDR output with ECC (without output register)	0.73	0.79	0.90	1.00	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.76	0.82	0.92	1.02	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{RCKC_ADDR} /T _{RCKC_ADDR}	ADDR inputs ⁽⁸⁾	0.47/ 0.27	0.53/ 0.29	0.62/ 0.32	0.66/ 0.34	ns, Min
T _{RDCK_DI} /T _{RCKD_DI}	DIN inputs ⁽⁹⁾	0.84/ 0.30	0.95/ 0.32	1.11/ 0.34	1.26/ 0.36	ns, Min
T _{RDCK_DI_ECC} /T _{RCKD_DI_ECC}	DIN inputs with block RAM ECC in standard mode ⁽⁹⁾	0.47/ 0.30	0.52/ 0.32	0.59/ 0.34	0.68/ 0.36	ns, Min
	DIN inputs with block RAM ECC encode only ⁽⁹⁾	0.68/ 0.30	0.75/ 0.32	0.85/ 0.34	0.97/ 0.36	ns, Min
	DIN inputs with FIFO ECC in standard mode ⁽⁹⁾	0.77/ 0.30	0.87/ 0.32	1.02/ 0.34	1.16/ 0.36	ns, Min
T _{RCKC_CLK} /T _{RCKC_CLK}	Inject single/double bit error in ECC mode	0.90/ 0.27	1.02/ 0.28	1.20/ 0.29	1.56/ 0.29	ns, Min
T _{RCKC_RDEN} /T _{RCKC_RDEN}	Block RAM Enable (EN) input	0.31/ 0.26	0.35/ 0.27	0.41/ 0.30	0.44/ 0.31	ns, Min
T _{RCKC_REGCE} /T _{RCKC_REGCE}	CE input of output register	0.18/ 0.25	0.19/ 0.27	0.22/ 0.31	0.24/ 0.33	ns, Min
T _{RCKC_RSTREG} /T _{RCKC_RSTREG}	Synchronous RSTREG input	0.22/ 0.23	0.24/ 0.24	0.28/ 0.26	0.31/ 0.27	ns, Min
T _{RCKC_RSTRAM} /T _{RCKC_RSTRAM}	Synchronous RSTRAM input	0.32/ 0.23	0.36/ 0.24	0.41/ 0.27	0.46/ 0.29	ns, Min

Table 57: Block RAM and FIFO Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{RCKK_WE}/T_{RCKC_WE}	Write Enable (WE) input (Block RAM only)	0.44/ 0.19	0.47/ 0.25	0.52/ 0.35	0.67/ 0.24	ns, Min
$T_{RCKK_WREN}/T_{RCKC_WREN}$	WREN FIFO inputs	0.47/ 0.26	0.50/ 0.27	0.55/ 0.30	0.68/ 0.31	ns, Min
$T_{RCKK_RDEN}/T_{RCKC_RDEN}$	RDEN FIFO inputs	0.46/ 0.26	0.50/ 0.27	0.55/ 0.30	0.67/ 0.31	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers ⁽¹⁰⁾	0.90	0.98	1.10	1.23	ns, Max
$T_{RCKK_RSTREG}/T_{RCKC_RSTREG}$	FIFO reset timing ⁽¹¹⁾	0.22/ 0.23	0.24/ 0.24	0.28/ 0.26	0.31/ 0.27	ns, Min
Maximum Frequency						
F_{MAX}	Block RAM in TDP and SDP modes (Write First and No Change modes)	600	540	450	340	MHz
	Block RAM (Read First mode)	525	475	400	275	MHz
	Block RAM (SDP mode) ⁽¹²⁾	525	475	400	275	MHz
$F_{MAX_CASCADE}$	Block RAM Cascade (Write First and No Change modes)	550	490	400	300	MHz
	Block RAM Cascade (Read First mode)	475	425	350	235	MHz
F_{MAX_FIFO}	FIFO in all modes	600	540	450	340	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	450	400	325	250	MHz

Notes:

- TRACE will report all of these parameters as T_{RCKO_DO} .
- T_{RCKO_DOR} includes T_{RCKO_DOW} , T_{RCKO_DOPR} , and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
- These parameters also apply to synchronous FIFO with $DO_REG = 0$.
- T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
- These parameters also apply to multirate (asynchronous) and synchronous FIFO with $DO_REG = 1$.
- T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY} , T_{RCKO_AFULL} , T_{RCKO_EMPTY} , T_{RCKO_FULL} , T_{RCKO_RDERR} , T_{RCKO_WRERR} .
- $T_{RCKO_POINTERS}$ includes both $T_{RCKO_RDCOUNT}$ and $T_{RCKO_WRCOUNT}$.
- The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
- T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
- T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
- The FIFO reset must be asserted for at least three positive clock edges.
- When using ISE software v12.4 or later, if the RDADDR_COLLISION_HWCONFIG attribute is set to PERFORMANCE or the block RAM is in single-port operation, then the faster F_{MAX} for WRITE_FIRST/NO_CHANGE modes apply.

Table 58: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
$T_{\text{DSPDO}}_{\{\text{PCIN}, \text{CARRYCASCIN}, \text{MULTSIGNIN}\}}_{\{\text{PCOUT}, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.28	1.46	1.72	1.72	2.06	ns
Clock to Outs from Output Register Clock to Output Pins							
$T_{\text{DSPCKO}}_{\{\text{P}, \text{CARRYOUT}\}}_{\text{PREG}}$	CLK (PREG) to {P, CARRYOUT} output	0.38	0.43	0.50	0.50	0.57	ns
$T_{\text{DSPCKO}}_{\{\text{PCOUT}, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}_{\text{PREG}}$	CLK (PREG) to {CARRYCASCOUT, PCOUT, MULTSIGNOUT} output	0.50	0.56	0.66	0.66	0.76	ns
Clock to Outs from Pipeline Register Clock to Output Pins							
$T_{\text{DSPCKO}}_{\{\text{P}, \text{CARRYOUT}\}}_{\text{MREG}}$	CLK (MREG) to {P, CARRYOUT} output	1.72	1.96	2.30	2.30	2.69	ns
$T_{\text{DSPCKO}}_{\{\text{PCOUT}, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}_{\text{MREG}}$	CLK (MREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.81	2.06	2.43	2.43	2.88	ns
$T_{\text{DSPCKO}}_{\{\text{P}, \text{CARRYOUT}\}}_{\text{ADREG_MULT}}$	CLK (ADREG) to {P, CARRYOUT} output	2.79	3.16	3.72	3.72	4.32	ns
$T_{\text{DSPCKO}}_{\{\text{PCOUT}, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}_{\text{ADREG_MULT}}$	CLK (ADREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.87	3.26	3.84	3.84	4.51	ns
Clock to Outs from Input Register Clock to Output Pins							
$T_{\text{DSPCKO}}_{\{\text{P}, \text{CARRYOUT}\}}_{\{\text{AREG}, \text{BREG}\}}_{\text{MULT}}$	CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier	3.97	4.52	5.36	5.36	6.20	ns
$T_{\text{DSPCKO}}_{\{\text{P}, \text{CARRYOUT}\}}_{\{\text{AREG}, \text{BREG}\}}$	CLK (AREG, BREG) to {P, CARRYOUT} output not using multiplier	1.70	1.93	2.27	2.27	2.65	ns
$T_{\text{DSPCKO}}_{\{\text{P}, \text{CARRYOUT}\}}_{\text{CREG}}$	CLK (CREG) to {P, CARRYOUT} output	1.70	1.93	2.27	2.27	2.80	ns
$T_{\text{DSPCKO}}_{\{\text{P}, \text{CARRYOUT}\}}_{\text{DREG_MULT}}$	CLK (DREG) to {P, CARRYOUT} output	3.89	4.44	5.25	5.25	6.07	ns
Clock to Outs from Input Register Clock to Cascading Output Pins							
$T_{\text{DSPCKO}}_{\{\text{ACOUT}, \text{BCOUT}\}}_{\{\text{AREG}, \text{BREG}\}}$	CLK (AREG, BREG) to {P, CARRYOUT} output	0.66	0.76	0.89	0.89	1.01	ns
$T_{\text{DSPCKO}}_{\{\text{PCOUT}, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}_{\{\text{AREG}, \text{BREG}\}}_{\text{MULT}}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	4.05	4.63	5.49	5.49	6.39	ns
$T_{\text{DSPCKO}}_{\{\text{PCOUT}, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}_{\{\text{AREG}, \text{BREG}\}}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.79	2.03	2.40	2.40	2.84	ns
$T_{\text{DSPCKO}}_{\{\text{PCOUT}, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}_{\text{DREG_MULT}}$	CLK (DREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.98	4.54	5.38	5.38	6.26	ns
$T_{\text{DSPCKO}}_{\{\text{PCOUT}, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}_{\text{CREG}}$	CLK (CREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.78	2.03	2.40	2.40	2.99	ns

Table 58: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Maximum Frequency							
F _{MAX}	With all registers used	600	540	450	450	410	MHz
F _{MAX_PATDET}	With pattern detector	551	483	408	408	356	MHz
F _{MAX_MULT_NOMREG}	Two register multiply without MREG	356	311	262	262	224	MHz
F _{MAX_MULT_NOMREG_PATDET}	Two register multiply without MREG with pattern detect	327	286	241	241	211	MHz
F _{MAX_PREADD_MULT_NOADREG}	Without ADREG	398	347	292	292	254	MHz
F _{MAX_PREADD_MULT_NOADREG_PATDET}	Without ADREG with pattern detect	398	347	292	292	254	MHz
F _{MAX_NOPIPELINEREG}	Without pipeline registers (MREG, ADREG)	266	233	196	196	171	MHz
F _{MAX_NOPIPELINEREG_PATDET}	Without pipeline registers (MREG, ADREG) with pattern detect	250	219	184	184	160	MHz

Configuration Switching Characteristics

Table 59: Configuration Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Power-up Timing Characteristics						
T _{PL} ⁽¹⁾	Program Latency	5	5	5	5	ms, Max
T _{POR} ⁽¹⁾	Power-on-Reset	15/55	15/55	15/55	15/60	ms, Min/Max
T _{ICCK}	CCLK (output) delay	400	400	400	400	ns, Min
T _{PROGRAM}	Program Pulse Width	250	250	250	250	ns, Min
Master/Slave Serial Mode Programming Switching						
T _{DCCK} /T _{CCKD}	DIN Setup/Hold, slave mode	4.0/0.0	4.0/0.0	4.0/0.0	4.5/0.0	ns, Min
T _{DSCCK} /T _{SCCKD}	DIN Setup/Hold, master mode	4.0/0.0	4.0/0.0	4.0/0.0	5.0/0.0	ns, Min
T _{CCO}	DOUT at 2.5V	6	6	6	7	ns, Max
	DOUT at 1.8V	6	6	6	7	ns, Max
F _{MCCK}	Maximum CCLK frequency, serial modes	105	105	105	70	MHz, Max
F _{MCCKTOL}	Frequency Tolerance, master mode with respect to nominal CCLK.	55	55	55	60	%
F _{MSCCK}	Slave mode external CCLK	100	100	100	100	MHz
SelectMAP Mode Programming Switching						
T _{SMDCK} /T _{SMCKD}	SelectMAP Data Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	5.5/0.0	ns, Min
T _{SMCSCCK} /T _{SMCKCS}	CSI_B Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	5.5/0.0	ns, Min
T _{SMCCKW} /T _{SMWCK}	RDWR_B Setup/Hold	10.0/0.0	10.0/0.0	10.0/0.0	16.0/0.0	ns, Min
T _{SMCKCSO}	CSO_B clock to out (330 Ω pull-up resistor required)	6	6	6	7	ns, Max
T _{SMCO}	CCLK to DATA out in readback at 2.5V	6	6	6	7	ns, Max
	CCLK to DATA out in readback at 1.8V	6	6	6	7	ns, Max

Table 59: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T _{SMCKBY}	CCLK to BUSY out in readback at 2.5V	6	6	6	7	ns, Max
	CCLK to BUSY out in readback at 1.8V	6	6	6	7	ns, Max
F _{SMCK}	Maximum Frequency with respect to nominal CCLK	100	100	100	70	MHz, Max
F _{RBCK}	Maximum Readback Frequency with respect to nominal CCLK	100	100	100	60	MHz, Max
F _{MCCKTOL}	Frequency tolerance, master mode with respect to nominal CCLK	55	55	55	60	%
Boundary-Scan Port Timing Specifications						
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI Setup time before TCK/ Hold time after TCK	3.0/2.0	3.0/2.0	3.0/2.0	4.0/2.0	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output valid at 2.5V	6	6	6	7	ns, Max
	TCK falling edge to TDO output valid at 1.8V	6	6	6	7	ns, Max
F _{TCK}	Maximum configuration TCK clock frequency	66	66	66	33	MHz, Max
F _{TCKB_MIN}	Minimum boundary-scan TCK clock frequency when using IEEE Std 1149.6 (AC-JTAG). Minimum operating temperature for IEEE Std 1149.6 is 0°C.	15	15	15	15	MHz, Min
F _{TCKB}	Maximum boundary-scan TCK clock frequency	66	66	66	33	MHz, Max
BPI Master Flash Mode Programming Switching						
T _{BPICCO} ⁽²⁾	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 2.5V	6	6	6	7	ns
	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 1.8V	6	6	6	7	ns
T _{BPIDCC} /T _{BPICCD}	Setup/Hold on D[15:0] data input pins	4.0/0.0	4.0/0.0	4.0/0.0	5.0/0.0	ns
T _{INITADDR}	Minimum period of initial ADDR[25:0] address cycles	3	3	3	3	CCLK cycles
SPI Master Flash Mode Programming Switching						
T _{SPIDCC} /T _{SPIDCCD}	DIN Setup/Hold before/after the rising CCLK edge	3.0/0.0	3.0/0.0	3.0/0.0	3.5/0.0	ns
T _{SPICCM}	MOSI clock to out at 2.5V	6	6	6	7	ns
	MOSI clock to out at 1.8V	6	6	6	7	ns
T _{SPICFC}	FCS_B clock to out at 2.5V	6	6	6	7	ns
	FCS_B clock to out at 1.8V	6	6	6	7	ns
T _{FSINIT} /T _{FSINITH}	FS[2:0] to INIT_B rising edge Setup and Hold	2	2	2	2	μs
CCLK Output (Master Modes)						
T _{MCCKL}	Master CCLK clock Low time duty cycle	45/55	45/55	45/55	40/60	%, Min/Max
T _{MCCKH}	Master CCLK clock High time duty cycle	45/55	45/55	45/55	40/60	%, Min/Max
CCLK Input (Slave Modes)						
T _{SCCKL}	Slave CCLK clock minimum Low time	2.5	2.5	2.5	2.5	ns, Min
T _{SCCKH}	Slave CCLK clock minimum High time	2.5	2.5	2.5	2.5	ns, Min
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
F _{DCK}	Maximum frequency for DCLK	200	200	200	200	MHz
T _{MMCMCDCK_DADDR} / T _{MMCMCKD_DADDR}	DADDR Setup/Hold	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns

Table 59: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{\text{MMCMDCK_DI/}}/T_{\text{MMCCKD_DI}}$	DI Setup/Hold	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{\text{MMCMDCK_DEN/}}/T_{\text{MMCCKD_DEN}}$	DEN Setup/Hold time	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{\text{MMCMDCK_DWE/}}/T_{\text{MMCCKD_DWE}}$	DWE Setup/Hold time	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{\text{MMCCKO_DO}}$	CLK to out of DO ⁽³⁾	2.60	3.02	3.64	3.68	ns
$T_{\text{MMCCKO_DRDY}}$	CLK to out of DRDY	0.32	0.34	0.38	0.38	ns

Notes:

1. To support longer delays in configuration, use the design solutions described in [UG360: Virtex-6 FPGA Configuration User Guide](#).
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
3. DO will hold until next DRP operation.

Clock Buffers and Networks

Table 60: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	Devices	Speed Grade				Units
			-3	-2	-1	-1L	
$T_{\text{BCCCK_CE/}}/T_{\text{BCCCK_CE}}^{(1)}$	CE pins Setup/Hold	All	0.11/ 0.00	0.13/ 0.00	0.16/ 0.00	0.13/ 0.00	ns
$T_{\text{BCCCK_S/}}/T_{\text{BCCCK_S}}^{(1)}$	S pins Setup/Hold	All	0.11/ 0.00	0.13/ 0.00	0.16/ 0.00	0.13/ 0.00	ns
$T_{\text{BCKO_O}}^{(2)}$	BUFGCTRL delay from I0/I1 to O	All	0.07	0.08	0.10	0.10	ns
Maximum Frequency							
F_{MAX}	Global clock tree (BUFG)	All except LX760	800	750	700	667	MHz
		LX760	N/A	700	700	667	MHz

Notes:

1. $T_{\text{BCCCK_CE}}$ and $T_{\text{BCCCK_S}}$ must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. $T_{\text{BCKO_O}}$ (BUFG delay from I0 to O) values are the same as $T_{\text{BCKO_O}}$ values.

Table 61: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{\text{BIOCKO_O}}$	Clock to out delay from I to O	0.14	0.16	0.18	0.21	ns
Maximum Frequency						
F_{MAX}	I/O clock tree (BUFIO)	800	800	710	710	MHz

Table 62: Regional Clock Switching Characteristics (BUFR)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{\text{BRCKO_O}}$	Clock to out delay from I to O	0.56	0.62	0.73	0.82	ns
$T_{\text{BRCKO_O_BYP}}$	Clock to out delay from I to O with Divide Bypass attribute set	0.28	0.31	0.36	0.41	ns

Table 66: Global Clock Input to Output Delay With MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> MMCM.							
T _{ICKOFFMMCMGC}	Global Clock Input and OUTFF <i>with</i> MMCM	XC6VLX75T	2.34	2.50	2.77	2.85	ns
		XC6VLX130T	2.35	2.51	2.78	2.87	ns
		XC6VLX195T	2.36	2.52	2.79	2.88	ns
		XC6VLX240T	2.36	2.52	2.79	2.88	ns
		XC6VLX365T	2.37	2.53	2.79	2.89	ns
		XC6VLX550T	N/A	2.55	2.82	2.93	ns
		XC6VLX760	N/A	2.54	2.82	2.92	ns
		XC6VSX315T	2.35	2.51	2.79	2.87	ns
		XC6VSX475T	N/A	2.43	2.70	2.79	ns
		XC6VHX250T	2.36	2.53	2.80	N/A	ns
		XC6VHX255T	2.46	2.63	2.91	N/A	ns
		XC6VHX380T	2.39	2.59	2.83	N/A	ns
		XC6VHX565T	N/A	2.54	2.81	N/A	ns
		XQ6VLX130T	N/A	2.51	2.78	2.87	ns
		XQ6VLX240T	N/A	2.52	2.79	2.88	ns
		XQ6VLX550T	N/A	N/A	2.82	2.93	ns
		XQ6VSX315T	N/A	2.51	2.79	2.87	ns
		XQ6VSX475T	N/A	N/A	2.70	2.79	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 70: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard. ⁽¹⁾							
T _{PSMMCMCC} / T _{PHMMCMCC}	No Delay Clock-capable Clock Input and IFF ⁽²⁾ with MMCM	XC6VLX75T	1.56/ −0.25	1.69/ −0.25	1.86/ −0.25	1.91/ −0.15	ns
		XC6VLX130T	1.64/ −0.25	1.78/ −0.25	1.95/ −0.25	2.00/ −0.14	ns
		XC6VLX195T	1.65/ −0.24	1.79/ −0.24	1.96/ −0.24	2.01/ −0.15	ns
		XC6VLX240T	1.65/ −0.24	1.79/ −0.24	1.96/ −0.24	2.01/ −0.15	ns
		XC6VLX365T	1.66/ −0.25	1.79/ −0.25	1.97/ −0.25	2.02/ −0.15	ns
		XC6VLX550T	N/A	1.97/ −0.24	2.16/ −0.24	2.19/ −0.14	ns
		XC6VLX760	N/A	2.39/ −0.20	2.63/ −0.20	2.21/ −0.10	ns
		XC6VSX315T	1.67/ −0.25	1.80/ −0.25	1.98/ −0.25	2.03/ −0.16	ns
		XC6VSX475T	N/A	1.98/ −0.29	2.17/ −0.29	2.21/ −0.20	ns
		XC6VHX250T	1.63/ −0.24	1.76/ −0.24	1.94/ −0.24	N/A	ns
		XC6VHX255T	1.63/ −0.19	1.76/ −0.19	1.99/ −0.19	N/A	ns
		XC6VHX380T	1.80/ −0.23	1.94/ −0.23	2.13/ −0.23	N/A	ns
		XC6VHX565T	N/A	1.94/ −0.08	2.13/ −0.08	N/A	ns
		XQ6VLX130T	N/A	1.78/ −0.25	1.95/ −0.25	2.00/ −0.14	ns
		XQ6VLX240T	N/A	1.79/ −0.24	1.96/ −0.24	2.01/ −0.15	ns
		XQ6VLX550T	N/A	N/A	2.16/ −0.24	2.19/ −0.14	ns
		XQ6VSX315T	N/A	1.80/ −0.25	1.98/ −0.25	2.03/ −0.16	ns
		XQ6VSX475T	N/A	N/A	2.17/ −0.29	2.21/ −0.20	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 FPGA clock transmitter and receiver data-valid windows.

Table 71: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion ⁽¹⁾	All	0.12	0.12	0.12	0.12	ns
T_{CKSKEW}	Global Clock Tree Skew ⁽²⁾	XC6VLX75T	0.15	0.16	0.18	0.17	ns
		XC6VLX130T	0.25	0.26	0.29	0.28	ns
		XC6VLX195T	0.26	0.27	0.31	0.30	ns
		XC6VLX240T	0.26	0.27	0.31	0.30	ns
		XC6VLX365T	0.28	0.29	0.31	0.31	ns
		XC6VLX550T	N/A	0.50	0.54	0.54	ns
		XC6VLX760	N/A	0.51	0.56	0.56	ns
		XC6VSX315T	0.27	0.28	0.32	0.30	ns
		XC6VSX475T	N/A	0.39	0.44	0.42	ns
		XC6VHX250T	0.25	0.26	0.29	N/A	ns
		XC6VHX255T	0.35	0.37	0.41	N/A	ns
		XC6VHX380T	0.45	0.47	0.52	N/A	ns
		XC6VHX565T	N/A	0.46	0.51	N/A	ns
		XQ6VLX130T	N/A	0.26	0.29	0.28	ns
		XQ6VLX240T	N/A	0.27	0.31	0.30	ns
		XQ6VLX550T	N/A	N/A	0.54	0.54	ns
		XQ6VSX315T	N/A	0.28	0.32	0.30	ns
		XQ6VSX475T	N/A	N/A	0.44	0.42	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.08	0.08	0.08	0.08	ns
T_{BUFIO_SKEW}	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	0.02	ns
T_{BUFIO_SKEW2}	I/O clock tree skew across three clock regions	All	0.10	0.12	0.23	0.12	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 73: Sample Window

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{SAMP}	Sampling Error at Receiver Pins ⁽¹⁾	All	510	560	610	670	ps
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO ⁽²⁾	All	300	350	400	440	ps

Notes:

1. This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 MMCM jitter
 - MMCM accuracy (phase offset)
 - MMCM phase shift resolution
These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 74: Pin-to-Pin Setup/Hold and Clock-to-Out

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO						
T _{PSCS} /T _{PHCS}	Setup/Hold of I/O clock	−0.28/1.09	−0.28/1.16	−0.28/1.33	−0.18/1.79	ns
Pin-to-Pin Clock-to-Out Using BUFIO						
T _{ICKOFC}	Clock-to-Out of I/O clock	4.22	4.59	5.22	5.63	ns

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
07/16/09	1.1	Revised the maximum V_{CCAUX} and V_{IN} numbers in Table 2, page 2 . Removed empty column from Table 3, page 3 . Revised specifications on Table 20, page 13 . Updated Table 38, page 22 and added notes 1 and 2. Revised T_{DLYCCO_RDY} , $T_{IDELAYCTRL_RPW}$, and $T_{IDELAYPAT_JIT}$ in Table 53, page 41 . Updated Table 58, page 46 to more closely match the DSP48E1 speed specifications. Updated T_{TAPTCK}/T_{TCKTAP} in Table 59, page 49 . Updated XC6VLX130T parameters in Table 68 through Table 70, page 59 .
08/19/09	1.2	Added values for -1L voltages and speed grade in all pertinent tables. Added V_{FS} and notes to Table 1 and Table 2 . Removed DV_{PPIN} from the example in Figure 2 . Added networking applications to Table 41, page 25 . Changed and added to the block RAM F_{MAX} section in Table 57, page 44 including removing Note 12. Changed F_{PFDMAX} values and corrected units for $T_{STATPHAOFFSET}$ and $T_{OUTDUTY}$ in Table 64, page 52 . Updated Table 71, page 60 .
09/16/09	2.0	Added Virtex-6 HXT devices to entire document including GTH Transceiver Specifications . Updated speed specifications as described in Switching Characteristics , includes changes in Table 51 , Table 57 , Table 58 , and Table 66 through Table 70 . Comprehensive changes to Table 14 , Table 15 , and Table 16 . Added conditions to DV_{PPOUT} and revised description of T_{OSKEW} in Table 17 . Removed V_{ISE} specification and note from Table 18 . Added note 3 to Table 23 . Updated note 3 in Table 24 . Updated LVCMOS25 delays in Table 44 . Updated specification for T_{IOTPHZ} in Table 46 . Removed $T_{BUFHSKEW}$ from Table 71, page 60 and added values for $T_{BUFIOSKEW}$. Added values in Table 74 .

Date	Version	Description of Revisions
01/18/10	2.1	Changed absolute maximum ratings for both V_{IN} and V_{TS} in Table 1 . Added data to Table 3 . Added data to Table 5 . Updated SSTL15 in Table 7 . Updated V_{OCM} and V_{OD} values in Table 8 . Added eFUSE endurance Table 12 . Added values to $V_{MGTREFCLK}$ and V_{IN} in Table 13 , page 11 . Added values and updated tables in the GTX Transceiver Specifications and GTH Transceiver Specifications sections. Added Table 27 and Figure 4 . Revised parameters and values in Table 39 . Updated Table 40 , page 23 . Added data to Table 41 . Updated speed specification to v1.04 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX240T for -1 and -2 speed grades. Speed specification changes and numerous updates also made to Table 44 , and Table 49 through Table 71 . Added data to Table 73 and Table 74 .
02/09/10	2.2	Revised description of C_{IN} in Table 3 . Clarified values in Table 5 . Fixed SDR LVDS unit error in Table 41 .
04/12/10	2.3	Added note 3 and update value of n in Table 3 . Clarified simultaneous power-down in Power-On Power Supply Requirements . Updated external reference junction temperatures in Table 40 , Analog-to-Digital Specifications . Updated speed specification to v1.05 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX130T for -1 and -2 speed grades. Fixed note 4 in Table 48 . Increased the -2 specification for $F_{IDELAYCTRL_REF}$ and clarified units for $T_{IDELAYPAT_JIT}$ in Table 53 . Added note 1 to Table 62 .
05/11/10	2.4	Updated F_{RXREC} in Table 22 . Revised $F_{IDELAYCTRL_REF}$ in Table 53 . Removed $T_{RCKO_PARITY_ECC}$: Clock CLK to ECCPARITY in standard ECC mode row in Table 57 . Added XC6VLX130T values to Table 72 .
05/26/10	2.5	Added XC6VLX195T data to Table 5 . Updated values in Table 22 including adding note 2 and note 3. Updated speed specification to v1.06 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX195T for -1 and -2 speed grades. Added XC6VLX195T values to Table 72 .
07/16/10	2.6	Changed Table 42 and Table 43 to production status on the -3 speed grade XC6VLX130T, XC6VLX195T, and XC6VLX240T devices. Added XC6VHX250T data to Table 4 and Table 72 . Added Note 6 to Table 64 .
07/23/10	2.7	Changed Table 42 and Table 43 to production status on the XC6VLX75T, XC6VLX365T, XC6VLX550T, XC6VLX760, XC6VSX315T, and XC6VSX475T devices using ISE 12.2 software with speed specification v1.08. Updated $V_{CMOUTDC}$ equation to $MGTAVTT - D_{VPPOUT}/4$ in Table 17 . Updated some -3, -2, -1 specifications in Table 65 through Table 72 . Added and updated -1L specifications to Table 41 and for most switching characteristics tables.
07/30/10	2.8	Changed Table 42 and Table 43 to production status on the -1L speed grade for the XC6VLX130T, XC6VLX195T, XC6VLX240T, XC6VLX365T, and XC6VLX550T devices using ISE 12.2 software with current speed specifications. Also updated the speed specifications for XC6VLX75T, XC6VLX550T, and XC6VSX315T. Updated V_{CCINT} specifications for -1L speed grade industrial temperature range devices in Table 2 .
09/20/10	2.9	In Table 32 , changed $F_{GPLLMAX}$ specification in -3 column from 5.951 to 5.591. In Table 40 , changed F_{MAX} for the DCLK from 250 MHz to 80 MHz.
10/18/10	2.10	The specification change in version 2.9, Table 40 is described in XCN10032 , <i>Virtex-6 FPGA: GTX Transceiver User Guide, Family Data Sheet (SYSMON DCLK), and JTAG ID Changes</i> . In this version (2.10), -1L(I) data is added to Table 4 and clarified in Note 2. Changed Table 42 and Table 43 to production status on the -1L speed grade XC6VLX75T, XC6VLX760, XC6VSX315T, and XC6VSX475T devices using ISE 12.3 software with current speed specifications. Revised the XC6VLX760 -1L speed specification for $T_{PHMMCMGC}$ in Table 69 and $T_{PHMMCMCC}$ in Table 70 .
01/17/11	2.11	Changed in Table 42 and Table 43 to production status on the XC6VHX250T devices using ISE 12.4 software with current speed specifications. Added industrial temperature range (T_I) recommended specifications to Table 2 ; including specific ranges for the -2I XC6VSX475T, XC6VLX550T, XC6VLX760, and XC6VHX565T devices. Added note 3 to Table 36 and maximum total jitter values. Added note 4 to Table 37 and maximum sinusoidal jitter values. Added note 2 to Table 43 . Revised F_{MAX} descriptions in Table 57 and added note 12. Added note 8 to F_{PFDMIN} in Table 64 . The following revisions are due to specification changes as described in XCN11009 , <i>Virtex-6 FPGA: Data Sheet, User Guides, and JTAG ID Updates</i> . In Table 59: Configuration Switching Characteristics , page 49 , revised -1L specifications for T_{POR} , F_{MCKK} , $F_{MCKKTOL}$, T_{SMCCKK} , T_{SMCKKW} , F_{RBCKK} , F_{TCK} , F_{TCKB} , T_{MCKKL} , and T_{MCKKH} . In Table 64: MMCM Specification , added bandwidth settings to F_{PFDMIN} and added note 1.

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