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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	59280
Number of Logic Elements/Cells	758784
Total RAM Bits	26542080
Number of I/O	1200
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1760-BBGA, FCBGA
Supplier Device Package	1760-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vlx760-1ff1760c

Table 2: Recommended Operating Conditions

Symbol	Description	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND for all devices except -1L devices.	0.95	1.05	V
	For -1L commercial temperature range devices: internal supply voltage relative to GND, $T_j = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	0.87	0.93	V
	For -1L industrial temperature range devices: internal supply voltage relative to GND, $T_j = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$	0.91	0.97	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	2.375	2.625	V
$V_{CCO}^{(1)(2)(3)}$	Supply voltage relative to GND	1.14	2.625	V
V_{IN}	2.5V supply voltage relative to GND	GND – 0.20	2.625	V
	2.5V and below supply voltage relative to GND	GND – 0.20	$V_{CCO} + 0.2$	V
$I_{IN}^{(5)}$	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	10	mA
$V_{BATT}^{(6)}$	Battery voltage relative to GND	1.0	2.5	V
$V_{FS}^{(7)}$	External voltage supply for eFUSE programming	2.375	2.625	V
T_j	Junction temperature operating range for commercial (C) temperature devices	0	85	$^{\circ}\text{C}$
	Junction temperature operating range for extended (E) temperature devices	0	100	$^{\circ}\text{C}$
	Junction temperature operating range for industrial (I) temperature devices	–40	100	$^{\circ}\text{C}$
	Junction temperature operating range for military (M) temperature devices	–55	125	$^{\circ}\text{C}$

Notes:

1. Configuration data is retained even if V_{CCO} drops to 0V.
2. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, and 2.5V.
3. The configuration supply voltage V_{CC_CONFIG} is also known as V_{CCO_0} .
4. All voltages are relative to ground.
5. A total of 100 mA per bank should not be exceeded.
6. V_{BATT} is required only when using bitstream encryption. If battery is not used, connect V_{BATT} to either ground or V_{CCAUX} .
7. During eFUSE programming, V_{FS} must be within the recommended operating range and $T_j = +15^{\circ}\text{C}$ to $+85^{\circ}\text{C}$. Otherwise, V_{FS} can be connected to GND.

Important Note

Typical values for quiescent supply current are specified at nominal voltage, 85°C junction temperatures (T_j). Xilinx recommends analyzing static power consumption at $T_j = 85^\circ\text{C}$ because the majority of designs operate near the high end of the commercial temperature range. Quiescent supply current is specified by speed grade for Virtex-6 devices. Use the XPower™ Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified in Table 4.

Table 4: Typical Quiescent Supply Current

Symbol	Description	Device	Speed and Temperature Grade						Units
			-3 (C)	-2 (C, E, & I)	-1 (C & I)	-1 (I & M) ⁽²⁾	-1L (C)	-1L (I) ⁽¹⁾	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC6VLX75T	927	927	927	N/A	656	741	mA
		XC6VLX130T	1563	1563	1563	N/A	1102	1245	mA
		XC6VLX195T	2059	2059	2059	N/A	1441	1628	mA
		XC6VLX240T	2478	2478	2478	N/A	1733	1957	mA
		XC6VLX365T	3001	3001	3001	N/A	2092	2363	mA
		XC6VLX550T ⁽³⁾	N/A	4515	4515	N/A	3147	3555	mA
		XC6VLX760 ⁽³⁾	N/A	5094	5094	N/A	3471	3921	mA
		XC6VSX315T	3476	3476	3476	N/A	2409	2721	mA
		XC6VSX475T ⁽³⁾	N/A	5227	5227	N/A	3622	4091	mA
		XC6VHX250T	2906	2906	2906	N/A	N/A	N/A	mA
		XC6VHX255T	2746	2746	2746	N/A	N/A	N/A	mA
		XC6VHX380T ⁽⁴⁾	4160	4160	4160	N/A	N/A	N/A	mA
		XC6VHX565T ⁽⁵⁾	N/A	5207	5207	N/A	N/A	N/A	mA
		XQ6VLX130T	N/A	1563	N/A	1563	N/A	1245	mA
		XQ6VLX240T	N/A	2478	N/A	2478	N/A	1957	mA
		XQ6VLX550T ⁽⁷⁾	N/A	N/A	N/A	4515	N/A	3555	mA
		XQ6VSX315T	N/A	3476	N/A	3476	N/A	2721	mA
		XQ6VSX475T ⁽⁷⁾	N/A	N/A	N/A	5227	N/A	4091	mA

Table 4: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed and Temperature Grade						Units
			-3 (C)	-2 (C, E, & I)	-1 (C & I)	-1 (I & M) ⁽²⁾	-1L (C)	-1L (I) ⁽¹⁾	
I _{CCOQ}	Quiescent V _{CCO} supply current	XC6VLX75T	1	1	1	N/A	1	1	mA
		XC6VLX130T	1	1	1	N/A	1	1	mA
		XC6VLX195T	1	1	1	N/A	1	1	mA
		XC6VLX240T	2	2	2	N/A	2	2	mA
		XC6VLX365T	2	2	2	N/A	2	2	mA
		XC6VLX550T ⁽³⁾	N/A	3	3	N/A	3	3	mA
		XC6VLX760 ⁽³⁾	N/A	3	3	N/A	3	3	mA
		XC6VSX315T	2	2	2	N/A	2	2	mA
		XC6VSX475T ⁽³⁾	N/A	2	2	N/A	2	2	mA
		XC6VHX250T	1	1	1	N/A	N/A	N/A	mA
		XC6VHX255T	1	1	1	N/A	N/A	N/A	mA
		XC6VHX380T ⁽⁴⁾	2	2	2	N/A	N/A	N/A	mA
		XC6VHX565T ⁽⁵⁾	N/A	2	2	N/A	N/A	N/A	mA
		XQ6VLX130T	N/A	1	N/A	1	N/A	1	mA
		XQ6VLX240T	N/A	2	N/A	2	N/A	2	mA
		XQ6VLX550T ⁽⁷⁾	N/A	N/A	N/A	3	N/A	3	mA
		XQ6VSX315T	N/A	2	N/A	2	N/A	2	mA
		XQ6VSX475T ⁽⁷⁾	N/A	N/A	N/A	2	N/A	2	mA

Table 4: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed and Temperature Grade						Units
			-3 (C)	-2 (C, E, & I)	-1 (C & I)	-1 (I & M) ⁽²⁾	-1L (C)	-1L (I) ⁽¹⁾	
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current	XC6VLX75T	45	45	45	N/A	45	45	mA
		XC6VLX130T	75	75	75	N/A	75	75	mA
		XC6VLX195T	113	113	113	N/A	113	113	mA
		XC6VLX240T	135	135	135	N/A	135	135	mA
		XC6VLX365T	191	191	191	N/A	191	191	mA
		XC6VLX550T ⁽³⁾	N/A	286	286	N/A	286	286	mA
		XC6VLX760 ⁽³⁾	N/A	387	387	N/A	387	387	mA
		XC6VSX315T	186	186	186	N/A	186	186	mA
		XC6VSX475T ⁽³⁾	N/A	279	279	N/A	279	279	mA
		XC6VHX250T	152	152	152	N/A	N/A	N/A	mA
		XC6VHX255T	152	152	152	N/A	N/A	N/A	mA
		XC6VHX380T ⁽⁴⁾	227	227	227	N/A	N/A	N/A	mA
		XC6VHX565T ⁽⁵⁾	N/A	315	315	N/A	N/A	N/A	mA
		XQ6VLX130T ⁽⁶⁾	N/A	75	N/A	75	N/A	75	mA
		XQ6VLX240T ⁽⁶⁾	N/A	135	N/A	135	N/A	135	mA
		XQ6VLX550T ⁽⁷⁾	N/A	N/A	N/A	286	N/A	286	mA
		XQ6VSX315T ⁽⁶⁾	N/A	186	N/A	186	N/A	186	mA
		XQ6VSX475T ⁽⁷⁾	N/A	N/A	N/A	279	N/A	279	mA

Notes:

- Typical values are specified at nominal voltage, 85°C junction temperatures (T_j). -1 and -2 industrial (I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. -1L industrial temperature range devices have the values specified in this column.
- Use the XPE tool to calculate 125°C values for -1M temperature range devices.
- The -2E extended temperature range (T_j = 0°C to +100°C) is only available in these devices. The -2I temperature range (T_j = -40°C to +100°C) is available for all other devices except the XC6VHX565T.
- The XC6VHX380T is available with both -2E and -2I temperature ranges.
- The XC6VHX565T is only available in the following temperature ranges: -1C, -1I, -2C, and -2E.
- The XQ6VLX130T, XQ6VLX240T, and XQ6VSX315T are available in -2I, -1I, -1M, and -1LI temperature ranges.
- The XQ6VLX550T and the XQ6VSX475T are only available in -1I and -1LI temperature ranges.
- Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
- If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPE or XPower Analyzer (XPA) tools.

GTH Transceiver Specifications

GTH Transceiver DC Characteristics

Table 25: Absolute Maximum Ratings for GTH Transceivers⁽¹⁾

Symbol	Description	Min	Max	Units
MGTHAVCC	Analog supply voltage for the GTH transmitter, receiver, and common analog circuits	−0.5	1.125	V
MGTHAVCCR _X	Analog supply voltage for the GTH receiver circuits and common analog circuits	−0.5	1.125	V
MGTHAVTT	Analog supply voltage for the GTH transmitter termination circuits	−0.5	1.32	V
MGTHAVCCPLL	Analog supply voltage for the GTH receiver and PLL circuits	−0.5	1.935	V
V _{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	−0.5	1.125	V
V _{MGTREFCLK}	Reference clock absolute input voltage	−0.5	1.935	V

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 26: Recommended Operating Conditions for GTH Transceivers ⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
MGTHAVCC	Analog supply voltage for the GTH transmitter, receiver, and common analog circuits	1.075	1.1	1.125	V
MGTHAVCCR _X	Analog supply voltage for the GTH receiver circuits and common analog circuits	1.075	1.1	1.125	V
MGTHAVTT	Analog supply voltage for the GTH transmitter termination circuits	1.140	1.2	1.26	V
MGTHAVCCPLL	Analog supply voltage for the GTH receiver and PLL circuit	1.710	1.8	1.89	V

Notes:

- Each voltage listed requires the filter circuit described in [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#).
- Voltages are specified for the temperature range of T_j = −40°C to +100°C.

Table 27: GTH Transceiver Power Supply Sequencing ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Description	Min	Max	Units
T _{HAVCC2HAVCCR_X}	Maximum time between powering MGTHAVCC to when MGTHAVCCR _X must be powered.	0	5	ms
T _{HAVCCR_X2HAVCCPLL}	Minimum time between powering MGTHAVCCR _X to when MGTHAVCCPLL can be powered.	10	—	μs
T _{HAVCCR_X2HAVTT}	Minimum time between powering MGTHAVCCR _X to when MGTHAVTT can be powered.	10	—	μs

Notes:

- MGTHAVCCR_X must be powered simultaneously or within T_{HAVCC2HAVCCR_X} of MGTHAVCC, but it must not precede MGTHAVCC.
- MGTHAVCC and MGTHAVCCR_X must be powered before MGTHAVCCPLL and MGTHAVTT. This minimum time is defined by T_{HAVCCR_X2HAVCCPLL} and T_{HAVCCR_X2HAVTT}.
- At any time, the condition of MGTHAVCC being present and MGTHAVCCR_X not being present should not occur for more than the maximum T_{HAVCC2HAVCCR_X}.

Figure 4 shows the timing parameters in Table 27.

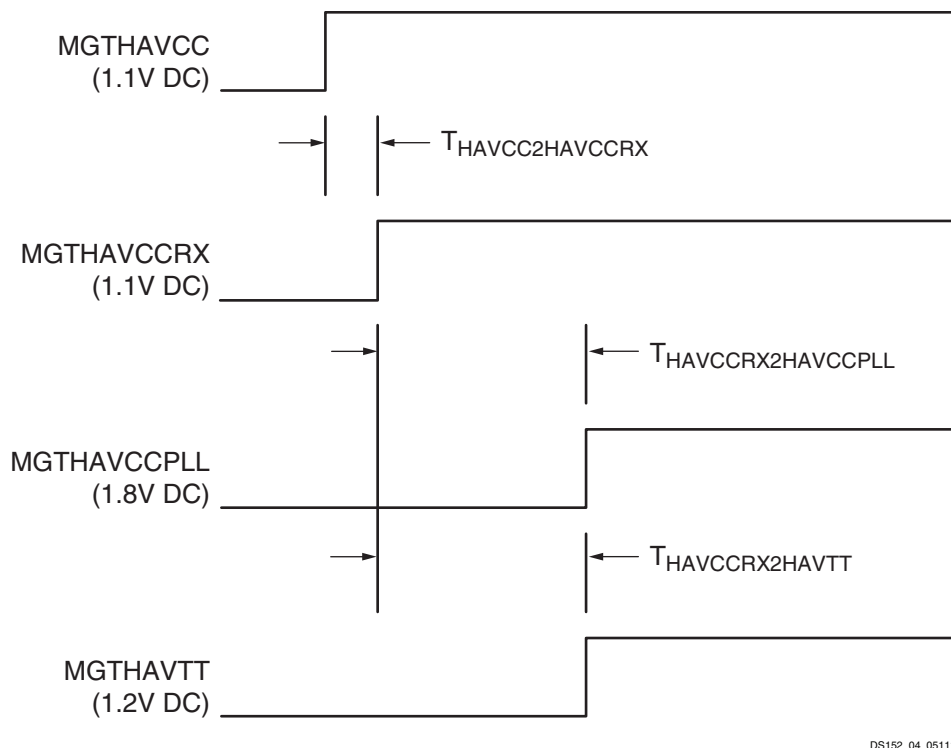


Figure 4: GTH Transceiver Power Supply Power-On Sequencing

Table 28: GTH Transceiver Supply Current

Symbol	Description	Typ ⁽¹⁾	Max	Units
$I_{MGTHAVCC}$	MGTHAVCC supply current for one GTH Quad (4 lanes)	571	Note 2	mA
$I_{MGTHAVCCR}$	MGTHAVCCR supply current for a GTH Quad (4 lanes)	254	Note 2	mA
$I_{MGTHAVTT}$	MGTHAVTT supply current for one GTH Quad (4 lanes)	93	Note 2	mA
$I_{MGTHAVCCPLL}$	MGTHAVCCPLL supply current for one GTH Quad (4 lanes)	219	Note 2	mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	1000.0 ± 1% tolerance		Ω

Notes:

- Typical values are specified at nominal voltage, 25°C, with a 10.3125 Gb/s line rate.
- Values for currents other than the values specified in this table can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

Table 29: GTH Transceiver Quiescent Supply Current⁽¹⁾⁽²⁾

Symbol	Description	Typ ⁽³⁾	Max	Units
$I_{MGTHAVCCQ}$	Quiescent MGTHAVCC Supply Current for one GTH Quad (4 lanes)	65	Note 4	mA
$I_{MGTHAVCCRQ}$	Quiescent MGTHAVCCR Supply Current for one GTH Quad (4 lanes)	17	Note 4	mA
$I_{MGTHAVTTQ}$	Quiescent MGTHAVTT Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA
$I_{MGTHAVCCPLLQ}$	Quiescent MGTHAVCCPLL Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA

Notes:

- Device powered and unconfigured.
- GTH transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTH transceivers.
- Typical values are specified at nominal voltage, 25°C.
- Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.

GTH Transceiver Switching Characteristics

Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further information.

Table 32: GTH Transceiver Maximum Data Rate and PLL Frequency Range

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F_{GTHMAX}	Maximum GTH transceiver data rate	PLL Output Divider = 1	11.182	11.182	10.32	Gb/s
		PLL Output Divider = 4	2.795	2.795	2.58	Gb/s
F_{GTHMIN}	Minimum GTH transceiver data rate ⁽¹⁾	PLL Output Divider = 1	9.92	9.92	9.92	Gb/s
		PLL Output Divider = 4	2.48	2.48	2.48	Gb/s
$F_{GPLLMAX}$	Maximum GTH PLL frequency		5.591	5.591	5.16	GHz
$F_{GPLLMIN}$	Minimum GTH PLL frequency		4.96	4.96	4.96	GHz

Notes:

- Lower data rates can be achieved using FPGA logic based oversampling designs.

Table 33: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{GTHDRPCLK}$	GTHDRPCLK maximum frequency	70	70	60	MHz

Table 34: GTH Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range	-1 speed grade	150	—	645	MHz
		-2 and -3 speed grades	150	—	700	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	—	200	—	ps
T_{FCLK}	Reference clock fall time	80% – 20%	—	200	—	ps
T_{DCREF}	Reference clock duty cycle	CLK	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	—	—	2	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	—	—	20	μs

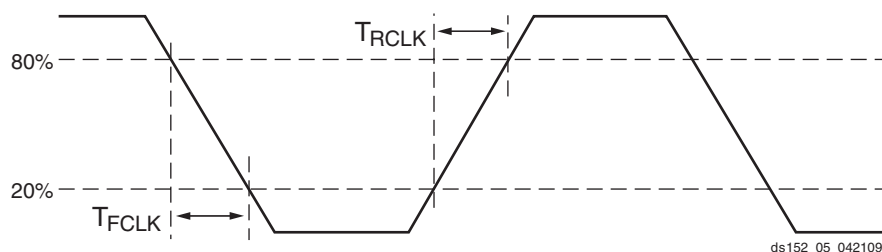


Figure 5: Reference Clock Timing Parameters

Table 35: GTH Transceiver User Clock Switching Characteristics ⁽¹⁾

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F _{TXOUT}	TXUSERCLKOUT maximum frequency		350	350	323	MHz
F _{RXOUT}	RXUSERCLKOUT maximum frequency		350	350	323	MHz
F _{TXIN}	TXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz
F _{RXIN}	RXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz

Notes:

1. Clocking must be implemented as described in [UG371](#): Virtex-6 FPGA GTH Transceivers User Guide.

Table 36: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
T _{RTX}	TX Rise time	20%–80%	–	50 ⁽³⁾	–	ps
T _{FTX}	TX Fall time	80%–20%	–	50 ⁽³⁾	–	ps
T _{LLSKEW}	TX lane-to-lane skew	within one GTH Quad	–	–	300	ps
Transmitter Output Jitter⁽¹⁾⁽²⁾						
TJ _{11.18}	Total Jitter	11.181 Gb/s	–	–	0.280	UI
DJ _{11.18}	Deterministic Jitter		–	–	0.170	UI
TJ _{10.3125}	Total Jitter	10.3125 Gb/s	–	–	0.280	UI
DJ _{10.3125}	Deterministic Jitter		–	–	0.170	UI
TJ _{9.953}	Total Jitter	9.953 Gb/s	–	–	0.280	UI
DJ _{9.953}	Deterministic Jitter		–	–	0.170	UI
TJ _{2.667}	Total Jitter	2.667 Gb/s	–	–	0.110	UI
DJ _{2.667}	Deterministic Jitter		–	–	0.060	UI
TJ _{2.488}	Total Jitter	2.488 Gb/s	–	–	0.110	UI
DJ _{2.488}	Deterministic Jitter		–	–	0.060	UI

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit-error ratio of 1e⁻¹².
3. Rise and fall times are specified at the transmitter package balls.

Table 37: GTH Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
R _{XRL}	Run length (CID)		8000	–	–	UI
R _{XPPMTOL}	Data/REFCLK PPM offset tolerance		–200	–	200	ppm
SJ Jitter Tolerance ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾						
JT_SJ _{11.18}	Sinusoidal Jitter	11.18 Gb/s	0.3	–	–	UI
JT_SJ _{10.32}	Sinusoidal Jitter	10.32 Gb/s	0.3	–	–	UI
JT_SJ _{9.95}	Sinusoidal Jitter	9.95 Gb/s	0.3	–	–	UI
JT_SJ _{2.667}	Sinusoidal Jitter	2.667 Gb/s	0.5	–	–	UI
JT_SJ _{2.48}	Sinusoidal Jitter	2.48 Gb/s	0.5	–	–	UI

Notes:

- These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit error ratio of 1e⁻¹².
- The frequency of the injected sinusoidal jitter is 80 MHz.
- High-frequency jitter tolerance including 6 db of channel loss at a high frequency of the data rate divided by two.

Ethernet MAC Switching Characteristics

Consult [UG368: Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide](#) for further information.

Table 38: Maximum Ethernet MAC Performance

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1	-1L	
F _{TEMACCLIENT}	Client interface maximum frequency	10 Mb/s – 8-bit width	2.5 ⁽¹⁾	2.5 ⁽¹⁾	2.5 ⁽¹⁾	2.5 ⁽¹⁾	MHz
		100 Mb/s – 8-bit width	25 ⁽²⁾	25 ⁽²⁾	25 ⁽²⁾	25 ⁽²⁾	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		1000 Mb/s – 16-bit width	62.5	62.5	62.5	62.5	MHz
		2000 Mb/s – 16-bit width	125	125	125	N/A	MHz
		2500 Mb/s – 16-bit width	156.25	156.25	156.25	N/A	MHz
F _{TEMACPHY}	Physical interface maximum frequency	10 Mb/s – 4-bit width	2.5	2.5	2.5	2.5	MHz
		100 Mb/s – 4-bit width	25	25	25	25	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		2000 Mb/s – 8-bit width	250	250	250	N/A	MHz
		2500 Mb/s – 8-bit width	312.5	312.5	312.5	N/A	MHz

Notes:

- When not using clock enable, the F_{MAX} is lowered to 1.25 MHz.
- When not using clock enable, the F_{MAX} is lowered to 12.5 MHz.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 39: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F _{PIPECLK}	Pipe clock maximum frequency	250	250	250	250	MHz
F _{USERCLK}	User clock maximum frequency	500	500	250	250	MHz
F _{DRPCLK}	DRP clock maximum frequency	250	250	250	250	MHz

System Monitor Analog-to-Digital Converter Specification

Table 40: Analog-to-Digital Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
AV _{DD} = 2.5V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 5.2 MHz, T _j = -55°C to 125°C M-Grade, Typical values at T _j = +35°C						
DC Accuracy: All external input channels. Both unipolar and bipolar modes.						
Resolution			10	—	—	Bits
Integral Nonlinearity	INL		—	—	±1	LSBs
Differential Nonlinearity	DNL	No missing codes (T _{MIN} to T _{MAX}) Guaranteed Monotonic	—	—	±0.9	LSBs
Unipolar Offset Error ⁽¹⁾		Uncalibrated	—	±2	±30	LSBs
Bipolar Offset Error ⁽¹⁾		Uncalibrated measured in bipolar mode	—	±2	±30	LSBs
Gain Error		Uncalibrated - External Reference	—	±0.2	±2	%
		Uncalibrated - Internal Reference	—	±2	—	%
Bipolar Gain Error ⁽¹⁾		Uncalibrated - External Reference	—	±0.2	±2	%
		Uncalibrated - Internal Reference	—	±2	—	%
Total Unadjusted Error (Uncalibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	—	±10	—	LSBs
		Deviation from ideal transfer function. Internal reference	—	±20	—	LSBs
Total Unadjusted Error (Calibrated)	TUE	Deviation from ideal transfer function. External 1.25V reference	—	±1	±2	LSBs
Calibrated Gain Temperature Coefficient		Variation of FS code with temperature	—	±0.01	—	LSB/°C
DC Common-Mode Reject	CMRR _{DC}	V _N = V _{CM} = 0.5V ± 0.5V, V _P - V _N = 100mV	—	70	—	dB
Conversion Rate ⁽²⁾						
Conversion Time - Continuous	t _{CONV}	Number of CLK cycles	26	—	32	
Conversion Time - Event	t _{CONV}	Number of CLK cycles	—	—	21	
T/H Acquisition Time	t _{ACQ}	Number of CLK cycles	4	—	—	
DRP Clock Frequency	DCLK	DRP clock frequency	8	—	80	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	—	5.2	MHz
CLK Duty cycle			40	—	60	%

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label ([Advance](#), [Preliminary](#), [Production](#)). Any labeling discrepancies are corrected in subsequent speed specification releases.

[Table 43](#) lists the production released Virtex-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE® software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 43: Virtex-6 Device Production Software and Speed Specification Release

Device	Speed Grade Designations			
	-3	-2	-1	-1L
XC6VLX75T	ISE 12.2 v1.08			ISE 12.3 v1.07 Patch
XC6VLX130T	ISE 12.1 v1.06	ISE 11.5 v1.05 ⁽²⁾	ISE 11.5 v1.05 ⁽²⁾	ISE 12.2 v1.05
XC6VLX195T	ISE 12.1 v1.06	ISE 12.1 v1.06	ISE 12.1 v1.06	ISE 12.2 v1.04
XC6VLX240T	ISE 12.1 v1.06	ISE 11.4.1 v1.04 ⁽²⁾	ISE 11.4.1 v1.04 ⁽²⁾	ISE 12.2 v1.04
XC6VLX365T	ISE 12.2 v1.08			ISE 12.2 v1.04
XC6VLX550T	N/A	ISE 12.2 v1.07		ISE 12.2 v1.04
XC6VLX760	N/A	ISE 12.2 v1.08		ISE 12.3 v1.07 Patch
XC6VSX315T	ISE 12.2 v1.08	ISE 12.1 v1.06		ISE 12.3 v1.07 Patch
XC6VSX475T	N/A	ISE 12.2 v1.08		ISE 12.3 v1.07 Patch
XC6VHX250T	ISE 12.4 v1.10			N/A
XC6VHX255T	ISE 13.1 v1.14 using the ISE 13.1 software update			N/A
XC6VHX380T	ISE 12.4 v1.10			N/A
XC6VHX565T	N/A	ISE 13.1 v1.14 using the ISE 13.1 software update		N/A
XQ6VLX130T	N/A	ISE 13.3 v1.17 Patch		ISE 13.3 v1.10
XQ6VLX240T	N/A	ISE 13.3 v1.17 Patch		ISE 13.3 v1.10
XQ6VLX550T	N/A	N/A	ISE 13.3 v1.17 Patch	ISE 13.3 v1.10
XQ6VSX315T	N/A	ISE 13.3 v1.17 Patch		ISE 13.3 v1.10
XQ6VSX475T	N/A	N/A	ISE 13.3 v1.17 Patch	ISE 13.3 v1.10

Notes:

- Blank entries indicate a device and/or speed grade in advance or preliminary status.
- Designs utilizing the GTX transceivers must use the software version ISE 12.1 v1.06 or later.

IOB Pad Input/Output/3-State Switching Characteristics

Table 44 (for commercial (XC) Virtex-6 devices) and **Table 45** (for the Defense-grade (XQ) Virtex-6 devices) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 46 summarizes the value of T_{IOTPHZ} . T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDS_25	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
LVDSEXT_25	0.85	0.94	1.09	1.08	1.53	1.65	1.84	1.73	1.53	1.65	1.84	1.73	ns
HT_25	0.85	0.94	1.09	1.08	1.51	1.62	1.78	1.69	1.51	1.62	1.78	1.69	ns
BLVDS_25	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.65	1.39	1.50	1.67	1.65	ns
RSDS_25 (point to point)	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
HSTL_I	0.81	0.91	1.06	1.06	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns
HSTL_II	0.81	0.91	1.06	1.06	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
HSTL_III	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
HSTL_I_18	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
HSTL_II_18	0.81	0.91	1.06	1.06	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
HSTL_III_18	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
SSTL2_I	0.81	0.91	1.06	1.06	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
SSTL2_II	0.81	0.91	1.06	1.06	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
LVC MOS25, Slow, 2 mA	0.51	0.57	0.66	0.70	5.09	5.46	6.01	5.63	5.09	5.46	6.01	5.63	ns
LVC MOS25, Slow, 4 mA	0.51	0.57	0.66	0.70	3.30	3.49	3.79	3.65	3.30	3.49	3.79	3.65	ns
LVC MOS25, Slow, 6 mA	0.51	0.57	0.66	0.70	2.62	2.81	3.08	2.95	2.62	2.81	3.08	2.95	ns
LVC MOS25, Slow, 8 mA	0.51	0.57	0.66	0.70	2.21	2.41	2.72	2.59	2.21	2.41	2.72	2.59	ns
LVC MOS25, Slow, 12 mA	0.51	0.57	0.66	0.70	1.80	1.95	2.17	2.10	1.80	1.95	2.17	2.10	ns
LVC MOS25, Slow, 16 mA	0.51	0.57	0.66	0.70	1.89	2.05	2.29	2.21	1.89	2.05	2.29	2.21	ns
LVC MOS25, Slow, 24 mA	0.51	0.57	0.66	0.70	1.68	1.82	2.02	1.98	1.68	1.82	2.02	1.98	ns
LVC MOS25, Fast, 2 mA	0.51	0.57	0.66	0.70	5.12	5.49	6.04	5.62	5.12	5.49	6.04	5.62	ns
LVC MOS25, Fast, 4 mA	0.51	0.57	0.66	0.70	3.28	3.50	3.82	3.65	3.28	3.50	3.82	3.65	ns
LVC MOS25, Fast, 6 mA	0.51	0.57	0.66	0.70	2.56	2.73	2.99	2.88	2.56	2.73	2.99	2.88	ns
LVC MOS25, Fast, 8 mA	0.51	0.57	0.66	0.70	2.11	2.33	2.65	2.53	2.11	2.33	2.65	2.53	ns
LVC MOS25, Fast, 12 mA	0.51	0.57	0.66	0.70	1.74	1.88	2.08	2.03	1.74	1.88	2.08	2.03	ns
LVC MOS25, Fast, 16 mA	0.51	0.57	0.66	0.70	1.77	1.92	2.13	2.08	1.77	1.92	2.13	2.08	ns

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDCI_DV2_25	0.51	0.57	0.66	0.70	1.71	1.83	2.01	2.00	1.71	1.83	2.01	2.00	ns
LVDCI_DV2_18	0.55	0.61	0.71	0.73	1.69	1.81	2.00	1.98	1.69	1.81	2.00	1.98	ns
LVDCI_DV2_15	0.64	0.73	0.85	0.85	1.68	1.77	1.91	1.98	1.68	1.77	1.91	1.98	ns
LVPECL_25	0.85	0.94	1.09	1.08	1.38	1.49	1.65	1.64	1.38	1.49	1.65	1.64	ns
HSTL_I_12	0.81	0.91	1.06	1.06	1.48	1.60	1.78	1.74	1.48	1.60	1.78	1.74	ns
HSTL_I_DCI	0.81	0.91	1.06	1.06	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
HSTL_II_DCI	0.81	0.91	1.06	1.06	1.37	1.49	1.68	1.66	1.37	1.49	1.68	1.66	ns
HSTL_II_T_DCI	0.81	0.91	1.06	1.06	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
HSTL_III_DCI	0.81	0.91	1.06	1.06	1.34	1.45	1.62	1.61	1.34	1.45	1.62	1.61	ns
HSTL_I_DCI_18	0.81	0.91	1.06	1.06	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
HSTL_II_DCI_18	0.81	0.91	1.06	1.06	1.36	1.46	1.62	1.59	1.36	1.46	1.62	1.59	ns
HSTL_II_T_DCI_18	0.81	0.91	1.06	1.06	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
HSTL_III_DCI_18	0.81	0.91	1.06	1.06	1.43	1.54	1.69	1.67	1.43	1.54	1.69	1.67	ns
DIFF_HSTL_I_18	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
DIFF_HSTL_I_DCI_18	0.85	0.94	1.09	1.08	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
DIFF_HSTL_I	0.85	0.94	1.09	1.08	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns
DIFF_HSTL_I_DCI	0.85	0.94	1.09	1.08	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
DIFF_HSTL_II_18	0.85	0.94	1.09	1.08	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
DIFF_HSTL_II_DCI_18	0.85	0.94	1.09	1.08	1.36	1.46	1.62	1.59	1.36	1.46	1.62	1.59	ns
DIFF_HSTL_II_T_DCI_18	0.85	0.94	1.09	1.08	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
DIFF_HSTL_II	0.85	0.94	1.09	1.08	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
DIFF_HSTL_II_DCI	0.85	0.94	1.09	1.08	1.37	1.49	1.68	1.66	1.37	1.49	1.68	1.66	ns
SSTL2_I_DCI	0.81	0.91	1.06	1.06	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
SSTL2_II_DCI	0.81	0.91	1.06	1.06	1.39	1.50	1.67	1.69	1.39	1.50	1.67	1.69	ns
SSTL2_II_T_DCI	0.81	0.91	1.06	1.06	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
SSTL18_I	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
SSTL18_II	0.81	0.91	1.06	1.06	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
SSTL18_I_DCI	0.81	0.91	1.06	1.06	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
SSTL18_II_DCI	0.81	0.91	1.06	1.06	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
SSTL18_II_T_DCI	0.81	0.91	1.06	1.06	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL2_I	0.85	0.94	1.09	1.08	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
DIFF_SSTL2_I_DCI	0.85	0.94	1.09	1.08	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
DIFF_SSTL2_II	0.85	0.94	1.09	1.08	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
DIFF_SSTL2_II_DCI	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.69	1.39	1.50	1.67	1.69	ns
DIFF_SSTL2_II_T_DCI	0.85	0.94	1.09	1.08	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns

Table 48: Output Delay Measurement Methodology (Cont'd)

Description	I/O Standard Attribute	R _{REF} (Ω)	C _{REF} ⁽¹⁾ (pF)	V _{MEAS} (V)	V _{REF} (V)
HT (HyperTransport), 2.5V	LDT_25	100	0	0 ⁽²⁾	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	100	0	0 ⁽²⁾	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V _{REF}	0.75
HSTL, Class III, with DCI	HSTL_III_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V _{REF}	0.9
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termination Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V _{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V _{REF}	1.25

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 49: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Setup/Hold						
T _{ICE1CK} /T _{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.21/ 0.03	0.25/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T _{ISRCK} /T _{ICKSR}	SR pin Setup/Hold with respect to CLK	0.66/ −0.08	0.78/ −0.08	0.96/ −0.08	1.09/ −0.11	ns
T _{IDOCK} /T _{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.07/ 0.41	0.08/ 0.46	0.10/ 0.54	0.11/ 0.64	ns
T _{IDOCKD} /T _{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.10/ 0.32	0.12/ 0.36	0.14/ 0.42	0.16/ 0.50	ns
Combinatorial						
T _{IDI}	D pin to O pin propagation delay, no Delay	0.15	0.17	0.20	0.23	ns
T _{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.19	0.22	0.25	0.28	ns
Sequential Delays						
T _{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.48	0.54	0.64	0.73	ns
T _{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.52	0.58	0.68	0.78	ns
T _{ICKQ}	CLK to Q outputs	0.54	0.61	0.70	0.93	ns
T _{RQ_ILOGIC}	SR pin to OQ/TQ out	0.85	0.97	1.15	1.32	ns
T _{GSRQ_ILOGIC}	Global Set/Reset to Q outputs	7.60	7.60	10.51	10.51	ns
Set/Reset						
T _{RPW_ILOGIC}	Minimum Pulse Width, SR inputs	0.78	0.95	1.20	1.30	ns, Min

Table 58: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Maximum Frequency							
F _{MAX}	With all registers used	600	540	450	450	410	MHz
F _{MAX_PATDET}	With pattern detector	551	483	408	408	356	MHz
F _{MAX_MULT_NOMREG}	Two register multiply without MREG	356	311	262	262	224	MHz
F _{MAX_MULT_NOMREG_PATDET}	Two register multiply without MREG with pattern detect	327	286	241	241	211	MHz
F _{MAX_PREADD_MULT_NOADREG}	Without ADREG	398	347	292	292	254	MHz
F _{MAX_PREADD_MULT_NOADREG_PATDET}	Without ADREG with pattern detect	398	347	292	292	254	MHz
F _{MAX_NOPIPELINEREG}	Without pipeline registers (MREG, ADREG)	266	233	196	196	171	MHz
F _{MAX_NOPIPELINEREG_PATDET}	Without pipeline registers (MREG, ADREG) with pattern detect	250	219	184	184	160	MHz

Configuration Switching Characteristics

Table 59: Configuration Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Power-up Timing Characteristics						
T _{PL} ⁽¹⁾	Program Latency	5	5	5	5	ms, Max
T _{POR} ⁽¹⁾	Power-on-Reset	15/55	15/55	15/55	15/60	ms, Min/Max
T _{ICCK}	CCLK (output) delay	400	400	400	400	ns, Min
T _{PROGRAM}	Program Pulse Width	250	250	250	250	ns, Min
Master/Slave Serial Mode Programming Switching						
T _{DCCK} /T _{CCKD}	DIN Setup/Hold, slave mode	4.0/0.0	4.0/0.0	4.0/0.0	4.5/0.0	ns, Min
T _{DSCCK} /T _{SCCKD}	DIN Setup/Hold, master mode	4.0/0.0	4.0/0.0	4.0/0.0	5.0/0.0	ns, Min
T _{CCO}	DOUT at 2.5V	6	6	6	7	ns, Max
	DOUT at 1.8V	6	6	6	7	ns, Max
F _{MCCK}	Maximum CCLK frequency, serial modes	105	105	105	70	MHz, Max
F _{MCCKTOL}	Frequency Tolerance, master mode with respect to nominal CCLK.	55	55	55	60	%
F _{MSCCK}	Slave mode external CCLK	100	100	100	100	MHz
SelectMAP Mode Programming Switching						
T _{SMDCK} /T _{SMCKD}	SelectMAP Data Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	5.5/0.0	ns, Min
T _{SMCSCCK} /T _{SMCKCS}	CSI_B Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	5.5/0.0	ns, Min
T _{SMCCKW} /T _{SMWCK}	RDWR_B Setup/Hold	10.0/0.0	10.0/0.0	10.0/0.0	16.0/0.0	ns, Min
T _{SMCKCSO}	CSO_B clock to out (330 Ω pull-up resistor required)	6	6	6	7	ns, Max
T _{SMCO}	CCLK to DATA out in readback at 2.5V	6	6	6	7	ns, Max
	CCLK to DATA out in readback at 1.8V	6	6	6	7	ns, Max

Table 59: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T _{SMCKBY}	CCLK to BUSY out in readback at 2.5V	6	6	6	7	ns, Max
	CCLK to BUSY out in readback at 1.8V	6	6	6	7	ns, Max
F _{SMCK}	Maximum Frequency with respect to nominal CCLK	100	100	100	70	MHz, Max
F _{RBCK}	Maximum Readback Frequency with respect to nominal CCLK	100	100	100	60	MHz, Max
F _{MCCKTOL}	Frequency tolerance, master mode with respect to nominal CCLK	55	55	55	60	%
Boundary-Scan Port Timing Specifications						
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI Setup time before TCK/ Hold time after TCK	3.0/2.0	3.0/2.0	3.0/2.0	4.0/2.0	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output valid at 2.5V	6	6	6	7	ns, Max
	TCK falling edge to TDO output valid at 1.8V	6	6	6	7	ns, Max
F _{TCK}	Maximum configuration TCK clock frequency	66	66	66	33	MHz, Max
F _{TCKB_MIN}	Minimum boundary-scan TCK clock frequency when using IEEE Std 1149.6 (AC-JTAG). Minimum operating temperature for IEEE Std 1149.6 is 0°C.	15	15	15	15	MHz, Min
F _{TCKB}	Maximum boundary-scan TCK clock frequency	66	66	66	33	MHz, Max
BPI Master Flash Mode Programming Switching						
T _{BPICCO} ⁽²⁾	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 2.5V	6	6	6	7	ns
	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 1.8V	6	6	6	7	ns
T _{BPIDCC} /T _{BPICCD}	Setup/Hold on D[15:0] data input pins	4.0/0.0	4.0/0.0	4.0/0.0	5.0/0.0	ns
T _{INITADDR}	Minimum period of initial ADDR[25:0] address cycles	3	3	3	3	CCLK cycles
SPI Master Flash Mode Programming Switching						
T _{SPIDCC} /T _{SPIDCCD}	DIN Setup/Hold before/after the rising CCLK edge	3.0/0.0	3.0/0.0	3.0/0.0	3.5/0.0	ns
T _{SPICCM}	MOSI clock to out at 2.5V	6	6	6	7	ns
	MOSI clock to out at 1.8V	6	6	6	7	ns
T _{SPICFC}	FCS_B clock to out at 2.5V	6	6	6	7	ns
	FCS_B clock to out at 1.8V	6	6	6	7	ns
T _{FSINIT} /T _{FSINITH}	FS[2:0] to INIT_B rising edge Setup and Hold	2	2	2	2	µs
CCLK Output (Master Modes)						
T _{MCCKL}	Master CCLK clock Low time duty cycle	45/55	45/55	45/55	40/60	%, Min/Max
T _{MCCKH}	Master CCLK clock High time duty cycle	45/55	45/55	45/55	40/60	%, Min/Max
CCLK Input (Slave Modes)						
T _{SCCKL}	Slave CCLK clock minimum Low time	2.5	2.5	2.5	2.5	ns, Min
T _{SCCKH}	Slave CCLK clock minimum High time	2.5	2.5	2.5	2.5	ns, Min
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
F _{DCK}	Maximum frequency for DCLK	200	200	200	200	MHz
T _{MMCMCKD_DADDR} / T _{MMCMCKD_DADDR}	DADDR Setup/Hold	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns

Table 69: Global Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T _{PSMMCMGC} / T _{PHMMCMGC}	No Delay Global Clock Input and IFF(2) with MMCM	XC6VLX75T	1.45/ −0.18	1.57/ −0.18	1.72/ −0.18	1.78/ −0.08	ns
		XC6VLX130T	1.53/ −0.18	1.65/ −0.18	1.81/ −0.18	1.87/ −0.07	ns
		XC6VLX195T	1.54/ −0.17	1.66/ −0.17	1.82/ −0.17	1.87/ −0.08	ns
		XC6VLX240T	1.54/ −0.17	1.66/ −0.17	1.82/ −0.17	1.87/ −0.08	ns
		XC6VLX365T	1.55/ −0.18	1.67/ −0.18	1.83/ −0.18	1.87/ −0.07	ns
		XC6VLX550T	N/A	1.84/ −0.17	2.02/ −0.17	2.06/ −0.06	ns
		XC6VLX760	N/A	2.26/ −0.13	2.49/ −0.13	2.06/ −0.03	ns
		XC6VSX315T	1.56/ −0.18	1.68/ −0.18	1.84/ −0.18	1.89/ −0.08	ns
		XC6VSX475T	N/A	1.85/ −0.23	2.03/ −0.23	2.07/ −0.13	ns
		XC6VHX250T	1.52/ −0.17	1.64/ −0.17	1.80/ −0.17	N/A	ns
		XC6VHX255T	1.52/ −0.12	1.64/ −0.12	1.85/ −0.12	N/A	ns
		XC6VHX380T	1.68/ −0.16	1.81/ −0.16	1.99/ −0.16	N/A	ns
		XC6VHX565T	N/A	1.81/ −0.01	1.99/ −0.01	N/A	ns
		XQ6VLX130T	N/A	1.65/ −0.18	1.81/ −0.18	1.87/ −0.07	ns
		XQ6VLX240T	N/A	1.66/ −0.17	1.82/ −0.17	1.87/ −0.08	ns
		XQ6VLX550T	N/A	N/A	2.02/ −0.17	2.06/ −0.06	ns
		XQ6VSX315T	N/A	1.68/ −0.18	1.84/ −0.18	1.89/ −0.08	ns
		XQ6VSX475T	N/A	N/A	2.03/ −0.23	2.07/ −0.13	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 70: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard. ⁽¹⁾							
T _{PSMMCMCC} / T _{PHMMCMCC}	No Delay Clock-capable Clock Input and IFF ⁽²⁾ with MMCM	XC6VLX75T	1.56/ −0.25	1.69/ −0.25	1.86/ −0.25	1.91/ −0.15	ns
		XC6VLX130T	1.64/ −0.25	1.78/ −0.25	1.95/ −0.25	2.00/ −0.14	ns
		XC6VLX195T	1.65/ −0.24	1.79/ −0.24	1.96/ −0.24	2.01/ −0.15	ns
		XC6VLX240T	1.65/ −0.24	1.79/ −0.24	1.96/ −0.24	2.01/ −0.15	ns
		XC6VLX365T	1.66/ −0.25	1.79/ −0.25	1.97/ −0.25	2.02/ −0.15	ns
		XC6VLX550T	N/A	1.97/ −0.24	2.16/ −0.24	2.19/ −0.14	ns
		XC6VLX760	N/A	2.39/ −0.20	2.63/ −0.20	2.21/ −0.10	ns
		XC6VSX315T	1.67/ −0.25	1.80/ −0.25	1.98/ −0.25	2.03/ −0.16	ns
		XC6VSX475T	N/A	1.98/ −0.29	2.17/ −0.29	2.21/ −0.20	ns
		XC6VHX250T	1.63/ −0.24	1.76/ −0.24	1.94/ −0.24	N/A	ns
		XC6VHX255T	1.63/ −0.19	1.76/ −0.19	1.99/ −0.19	N/A	ns
		XC6VHX380T	1.80/ −0.23	1.94/ −0.23	2.13/ −0.23	N/A	ns
		XC6VHX565T	N/A	1.94/ −0.08	2.13/ −0.08	N/A	ns
		XQ6VLX130T	N/A	1.78/ −0.25	1.95/ −0.25	2.00/ −0.14	ns
		XQ6VLX240T	N/A	1.79/ −0.24	1.96/ −0.24	2.01/ −0.15	ns
		XQ6VLX550T	N/A	N/A	2.16/ −0.24	2.19/ −0.14	ns
		XQ6VSX315T	N/A	1.80/ −0.25	1.98/ −0.25	2.03/ −0.16	ns
		XQ6VSX475T	N/A	N/A	2.17/ −0.29	2.21/ −0.20	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 72: Package Skew

Symbol	Description	Device	Package	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	XC6VLX75T	FF484	95	ps
			FF784	146	ps
		XC6VLX130T	FF484	95	ps
			FF784	146	ps
			FF1156	165	ps
		XC6VLX195T	FF784	145	ps
			FF1156	182	ps
		XC6VLX240T	FF784	146	ps
			FF1156	182	ps
			FF1759	187	ps
		XC6VLX365T	FF1156	189	ps
			FF1759	184	ps
		XC6VLX550T	FF1759	196	ps
			FF1760	249	ps
		XC6VLX760	FF1760	236	ps
		XC6VSX315T	FF1156	168	ps
			FF1759	190	ps
		XC6VSX475T	FF1156	168	ps
			FF1759	204	ps
		XC6VHX250T	FF1154	166	ps
		XC6VHX255T	FF1155	168	ps
			FF1923	228	ps
		XC6VHX380T	FF1154	159	ps
			FF1155	172	ps
			FF1923	227	ps
			FF1924	220	ps
		XC6VHX565T	FF1923	232	ps
			FF1924	197	ps
		XQ6VLX130T	RF784	146	ps
			RF1156	165	ps
			FFG1156	165	ps
		XQ6VLX240T	RF784	146	ps
			RF1156	182	ps
			FFG1156	182	ps
			RF1759	187	ps
		XQ6VLX550T	RF1759	196	ps
		XQ6VSX315T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	190	ps
		XQ6VSX475T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	204	ps

Notes:

- These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
- Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Date	Version	Description of Revisions
01/18/10	2.1	Changed absolute maximum ratings for both V_{IN} and V_{TS} in Table 1 . Added data to Table 3 . Added data to Table 5 . Updated SSTL15 in Table 7 . Updated V_{OCM} and V_{OD} values in Table 8 . Added eFUSE endurance Table 12 . Added values to $V_{MGTREFCLK}$ and V_{IN} in Table 13 , page 11 . Added values and updated tables in the GTX Transceiver Specifications and GTH Transceiver Specifications sections. Added Table 27 and Figure 4 . Revised parameters and values in Table 39 . Updated Table 40 , page 23 . Added data to Table 41 . Updated speed specification to v1.04 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX240T for -1 and -2 speed grades. Speed specification changes and numerous updates also made to Table 44 , and Table 49 through Table 71 . Added data to Table 73 and Table 74 .
02/09/10	2.2	Revised description of C_{IN} in Table 3 . Clarified values in Table 5 . Fixed SDR LVDS unit error in Table 41 .
04/12/10	2.3	Added note 3 and update value of n in Table 3 . Clarified simultaneous power-down in Power-On Power Supply Requirements . Updated external reference junction temperatures in Table 40 , Analog-to-Digital Specifications . Updated speed specification to v1.05 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX130T for -1 and -2 speed grades. Fixed note 4 in Table 48 . Increased the -2 specification for $F_{IDELAYCTRL_REF}$ and clarified units for $T_{IDELAYPAT_JIT}$ in Table 53 . Added note 1 to Table 62 .
05/11/10	2.4	Updated F_{RXREC} in Table 22 . Revised $F_{IDELAYCTRL_REF}$ in Table 53 . Removed $T_{RCKO_PARITY_ECC}$: Clock CLK to ECCPARITY in standard ECC mode row in Table 57 . Added XC6VLX130T values to Table 72 .
05/26/10	2.5	Added XC6VLX195T data to Table 5 . Updated values in Table 22 including adding note 2 and note 3. Updated speed specification to v1.06 with appropriate changes to Table 42 and Table 43 including production release of the XC6VLX195T for -1 and -2 speed grades. Added XC6VLX195T values to Table 72 .
07/16/10	2.6	Changed Table 42 and Table 43 to production status on the -3 speed grade XC6VLX130T, XC6VLX195T, and XC6VLX240T devices. Added XC6VHX250T data to Table 4 and Table 72 . Added Note 6 to Table 64 .
07/23/10	2.7	Changed Table 42 and Table 43 to production status on the XC6VLX75T, XC6VLX365T, XC6VLX550T, XC6VLX760, XC6VSX315T, and XC6VSX475T devices using ISE 12.2 software with speed specification v1.08. Updated $V_{CMOUTDC}$ equation to $MGTAVTT - D_{VPPOUT}/4$ in Table 17 . Updated some -3, -2, -1 specifications in Table 65 through Table 72 . Added and updated -1L specifications to Table 41 and for most switching characteristics tables.
07/30/10	2.8	Changed Table 42 and Table 43 to production status on the -1L speed grade for the XC6VLX130T, XC6VLX195T, XC6VLX240T, XC6VLX365T, and XC6VLX550T devices using ISE 12.2 software with current speed specifications. Also updated the speed specifications for XC6VLX75T, XC6VLX550T, and XC6VSX315T. Updated V_{CCINT} specifications for -1L speed grade industrial temperature range devices in Table 2 .
09/20/10	2.9	In Table 32 , changed $F_{GPLLMAX}$ specification in -3 column from 5.951 to 5.591. In Table 40 , changed F_{MAX} for the DCLK from 250 MHz to 80 MHz.
10/18/10	2.10	The specification change in version 2.9, Table 40 is described in XCN10032 , <i>Virtex-6 FPGA: GTX Transceiver User Guide, Family Data Sheet (SYSMON DCLK), and JTAG ID Changes</i> . In this version (2.10), -1L(I) data is added to Table 4 and clarified in Note 2. Changed Table 42 and Table 43 to production status on the -1L speed grade XC6VLX75T, XC6VLX760, XC6VSX315T, and XC6VSX475T devices using ISE 12.3 software with current speed specifications. Revised the XC6VLX760 -1L speed specification for $T_{PHMMCMGC}$ in Table 69 and $T_{PHMMCMCC}$ in Table 70 .
01/17/11	2.11	Changed in Table 42 and Table 43 to production status on the XC6VHX250T devices using ISE 12.4 software with current speed specifications. Added industrial temperature range (T_I) recommended specifications to Table 2 ; including specific ranges for the -2I XC6VSX475T, XC6VLX550T, XC6VLX760, and XC6VHX565T devices. Added note 3 to Table 36 and maximum total jitter values. Added note 4 to Table 37 and maximum sinusoidal jitter values. Added note 2 to Table 43 . Revised F_{MAX} descriptions in Table 57 and added note 12. Added note 8 to F_{PFDMIN} in Table 64 . The following revisions are due to specification changes as described in XCN11009 , <i>Virtex-6 FPGA: Data Sheet, User Guides, and JTAG ID Updates</i> . In Table 59: Configuration Switching Characteristics , page 49 , revised -1L specifications for T_{POR} , F_{MCKK} , $F_{MCKKTOL}$, T_{SMCCKK} , T_{SMCKKW} , F_{RBCKK} , F_{TCK} , F_{TCKB} , T_{MCKKL} , and T_{MCKKH} . In Table 64: MMCM Specification , added bandwidth settings to F_{PFDMIN} and added note 1.