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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	24600
Number of Logic Elements/Cells	314880
Total RAM Bits	25952256
Number of I/O	720
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1759-BBGA, FCBGA
Supplier Device Package	1759-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vsx315t-1ff1759c

Table 3: DC Characteristics Over Recommended Operating Conditions (1)(2)

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	10	μA
I_L	Input or output leakage current per pin (sample-tested)	–	–	10	μA
$C_{IN}^{(3)}$	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 2.5V$	20	–	80	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.8V$	8	–	40	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.5V$	5	–	30	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.2V$	1	–	20	μA
I_{RPD}	Pad pull-down (when selected) @ $V_{IN} = 2.5V$	3	–	80	μA
I_{BATT}	Battery supply current	–	–	150	nA
n	Temperature diode ideality factor	–	1.0002	–	n
r	Series resistance	–	5	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst case process at 25°C.
3. This measurement represents the die capacitance at the pad, not including the package.

Table 6: Power Supply Ramp Time

Symbol	Description	Ramp Time	Units
V_{CCINT}	Internal supply voltage relative to GND	0.20 to 50.0	ms
V_{CCO}	Output drivers supply voltage relative to GND	0.20 to 50.0	ms
V_{CCAUX}	Auxiliary supply voltage relative to GND	0.20 to 50.0	ms

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 7: SelectIO DC Input and Output Levels

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVC MOS25, LVDCI25	-0.3	0.7	1.7	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	Note(3)	Note(3)
LVC MOS18, LVDCI18	-0.3	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.3$	0.45	$V_{CCO} - 0.45$	Note(4)	Note(4)
LVC MOS15, LVDCI15	-0.3	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.3$	25% V_{CCO}	75% V_{CCO}	Note(4)	Note(4)
LVC MOS12	-0.3	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.3$	25% V_{CCO}	75% V_{CCO}	Note(5)	Note(5)
HSTL I ₁₂	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	25% V_{CCO}	75% V_{CCO}	6.3	6.3
HSTL I ⁽²⁾	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	8	-8
HSTL II ⁽²⁾	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	16	-16
HSTL III ⁽²⁾	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	24	-8
DIFF HSTL I ⁽²⁾	-0.3	50% $V_{CCO} - 0.1$	50% $V_{CCO} + 0.1$	$V_{CCO} + 0.3$	—	—	—	—
DIFF HSTL II ⁽²⁾	-0.3	50% $V_{CCO} - 0.1$	50% $V_{CCO} + 0.1$	$V_{CCO} + 0.3$	—	—	—	—
SSTL2 I	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCO} + 0.3$	$V_{TT} - 0.61$	$V_{TT} + 0.61$	8.1	-8.1
SSTL2 II	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCO} + 0.3$	$V_{TT} - 0.81$	$V_{TT} + 0.81$	16.2	-16.2
DIFF SSTL2 I	-0.3	50% $V_{CCO} - 0.15$	50% $V_{CCO} + 0.15$	$V_{CCO} + 0.3$	—	—	—	—
DIFF SSTL2 II	-0.3	50% $V_{CCO} - 0.15$	50% $V_{CCO} + 0.15$	$V_{CCO} + 0.3$	—	—	—	—
SSTL18 I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.3$	$V_{TT} - 0.47$	$V_{TT} + 0.47$	6.7	-6.7
SSTL18 II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.3$	$V_{TT} - 0.60$	$V_{TT} + 0.60$	13.4	-13.4
DIFF SSTL18 I	-0.3	50% $V_{CCO} - 0.125$	50% $V_{CCO} + 0.125$	$V_{CCO} + 0.3$	—	—	—	—
DIFF SSTL18 II	-0.3	50% $V_{CCO} - 0.125$	50% $V_{CCO} + 0.125$	$V_{CCO} + 0.3$	—	—	—	—
SSTL15	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	$V_{TT} - 0.175$	$V_{TT} + 0.175$	14.3	14.3

Notes:

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. Supported drive strengths of 2, 4, 6, or 8 mA.
6. For detailed interface specific DC voltage levels, see [UG361](#): Virtex-6 FPGA SelectIO Resources User Guide.

Table 24: GTX Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
F _{GTXRX}	Serial data rate	RX oversampler not enabled	0.600	–	F _{GTXMAX}	Gb/s
		RX oversampler enabled	0.480	–	0.600	Gb/s
T _{RXELECIDLE}	Time for RXELECIdle to respond to loss or restoration of data		–	75	–	ns
RX _{OOBVDPP}	OOB detect threshold peak-to-peak		60	–	150	mV
RX _{SST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated @ 33 KHz	–5000	–	0	ppm
RX _{RL}	Run length (CID)	Internal AC capacitor bypassed	–	–	512	UI
RX _{PPMTOL}	Data/REFCLK PPM offset tolerance	CDR 2 nd -order loop disabled	–200	–	200	ppm
		CDR 2 nd -order loop enabled	–2000	–	2000	ppm
SJ Jitter Tolerance ⁽²⁾						
JT_SJ _{6.5}	Sinusoidal Jitter ⁽³⁾	6.5 Gb/s	0.44	–	–	UI
JT_SJ _{5.0}	Sinusoidal Jitter ⁽³⁾	5.0 Gb/s	0.44	–	–	UI
JT_SJ _{4.25}	Sinusoidal Jitter ⁽³⁾	4.25 Gb/s	0.44	–	–	UI
JT_SJ _{3.75}	Sinusoidal Jitter ⁽³⁾	3.75 Gb/s	0.44	–	–	UI
JT_SJ _{3.125}	Sinusoidal Jitter ⁽³⁾	3.125 Gb/s	0.45	–	–	UI
JT_SJ _{3.125L}	Sinusoidal Jitter ⁽³⁾	3.125 Gb/s ⁽⁴⁾	0.45	–	–	UI
JT_SJ _{2.5}	Sinusoidal Jitter ⁽³⁾	2.5 Gb/s ⁽⁵⁾	0.5	–	–	UI
JT_SJ _{1.25}	Sinusoidal Jitter ⁽³⁾	1.25 Gb/s ⁽⁶⁾	0.5	–	–	UI
JT_SJ ₆₀₀	Sinusoidal Jitter ⁽³⁾	600 Mb/s	0.4	–	–	UI
JT_SJ ₄₈₀	Sinusoidal Jitter ⁽³⁾	480 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye ⁽²⁾						
JT_TJSE _{3.125}	Total Jitter with Stressed Eye ⁽⁷⁾	3.125 Gb/s	0.70	–	–	UI
		5.0 Gb/s	0.70	–	–	UI
JT_SJSE _{3.125}	Sinusoidal Jitter with Stressed Eye ⁽⁷⁾	3.125 Gb/s	0.1	–	–	UI
		5.0 Gb/s	0.1	–	–	UI

Notes:

- Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 1e^{–12}.
- The frequency of the injected sinusoidal jitter is 80 MHz.
- PLL frequency at 1.5625 GHz and OUTDIV = 1.
- PLL frequency at 2.5 GHz and OUTDIV = 2.
- PLL frequency at 2.5 GHz and OUTDIV = 4.
- Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Specifications

GTH Transceiver DC Characteristics

Table 25: Absolute Maximum Ratings for GTH Transceivers⁽¹⁾

Symbol	Description	Min	Max	Units
MGTHAVCC	Analog supply voltage for the GTH transmitter, receiver, and common analog circuits	−0.5	1.125	V
MGTHAVCCR _X	Analog supply voltage for the GTH receiver circuits and common analog circuits	−0.5	1.125	V
MGTHAVTT	Analog supply voltage for the GTH transmitter termination circuits	−0.5	1.32	V
MGTHAVCCPLL	Analog supply voltage for the GTH receiver and PLL circuits	−0.5	1.935	V
V _{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	−0.5	1.125	V
V _{MGTREFCLK}	Reference clock absolute input voltage	−0.5	1.935	V

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 26: Recommended Operating Conditions for GTH Transceivers ⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
MGTHAVCC	Analog supply voltage for the GTH transmitter, receiver, and common analog circuits	1.075	1.1	1.125	V
MGTHAVCCR _X	Analog supply voltage for the GTH receiver circuits and common analog circuits	1.075	1.1	1.125	V
MGTHAVTT	Analog supply voltage for the GTH transmitter termination circuits	1.140	1.2	1.26	V
MGTHAVCCPLL	Analog supply voltage for the GTH receiver and PLL circuit	1.710	1.8	1.89	V

Notes:

- Each voltage listed requires the filter circuit described in [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#).
- Voltages are specified for the temperature range of T_j = −40°C to +100°C.

Table 27: GTH Transceiver Power Supply Sequencing ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Description	Min	Max	Units
T _{HAVCC2HAVCCR_X}	Maximum time between powering MGTHAVCC to when MGTHAVCCR _X must be powered.	0	5	ms
T _{HAVCCR_X2HAVCCPLL}	Minimum time between powering MGTHAVCCR _X to when MGTHAVCCPLL can be powered.	10	—	μs
T _{HAVCCR_X2HAVTT}	Minimum time between powering MGTHAVCCR _X to when MGTHAVTT can be powered.	10	—	μs

Notes:

- MGTHAVCCR_X must be powered simultaneously or within T_{HAVCC2HAVCCR_X} of MGTHAVCC, but it must not precede MGTHAVCC.
- MGTHAVCC and MGTHAVCCR_X must be powered before MGTHAVCCPLL and MGTHAVTT. This minimum time is defined by T_{HAVCCR_X2HAVCCPLL} and T_{HAVCCR_X2HAVTT}.
- At any time, the condition of MGTHAVCC being present and MGTHAVCCR_X not being present should not occur for more than the maximum T_{HAVCC2HAVCCR_X}.

Figure 4 shows the timing parameters in Table 27.

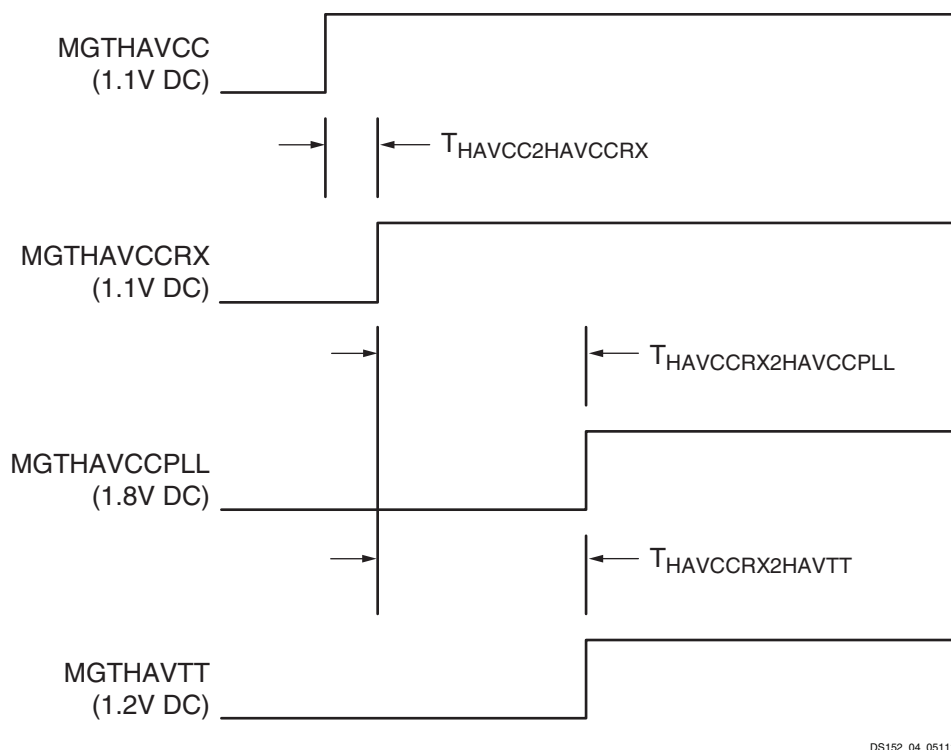


Figure 4: GTH Transceiver Power Supply Power-On Sequencing

Table 28: GTH Transceiver Supply Current

Symbol	Description	Typ ⁽¹⁾	Max	Units
$I_{MGTHAVCC}$	MGTHAVCC supply current for one GTH Quad (4 lanes)	571	Note 2	mA
$I_{MGTHAVCCR}$	MGTHAVCCR supply current for a GTH Quad (4 lanes)	254	Note 2	mA
$I_{MGTHAVTT}$	MGTHAVTT supply current for one GTH Quad (4 lanes)	93	Note 2	mA
$I_{MGTHAVCCPLL}$	MGTHAVCCPLL supply current for one GTH Quad (4 lanes)	219	Note 2	mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	1000.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 10.3125 Gb/s line rate.
2. Values for currents other than the values specified in this table can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

Table 29: GTH Transceiver Quiescent Supply Current⁽¹⁾⁽²⁾

Symbol	Description	Typ ⁽³⁾	Max	Units
$I_{MGTHAVCCQ}$	Quiescent MGTHAVCC Supply Current for one GTH Quad (4 lanes)	65	Note 4	mA
$I_{MGTHAVCCRQ}$	Quiescent MGTHAVCCR Supply Current for one GTH Quad (4 lanes)	17	Note 4	mA
$I_{MGTHAVTTQ}$	Quiescent MGTHAVTT Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA
$I_{MGTHAVCCPLLQ}$	Quiescent MGTHAVCCPLL Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA

Notes:

1. Device powered and unconfigured.
2. GTH transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTH transceivers.
3. Typical values are specified at nominal voltage, 25°C.
4. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.

GTH Transceiver DC Input and Output Levels

Table 30 summarizes the DC output specifications of the GTH transceivers in Virtex-6 FPGAs. Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further details.

Table 30: GTH Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
D_{VPPIN}	Differential peak-to-peak input voltage	External AC coupled	175	–	1200	mV
D_{VPPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	800	–	1200	mV
R_{IN}	Differential input resistance		80	100	120	Ω
R_{OUT}	Differential output resistance		80	100	120	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	–	ps
C_{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 31 summarizes the DC specifications of the clock input of the GTH transceiver. Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further details.

Table 31: GTH Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	≤ 600 MHz	500	–	1600	mV
		> 600 MHz	600	–	1600	mV
R_{IN}	Differential input resistance		80	100	120	Ω
C_{EXT}	Required external AC coupling capacitor		–	100	–	nF

Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.17 for -3, -2, and -1; and v1.10 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 42 correlates the current status of each Virtex-6 device on a per speed grade basis.

Table 42: Virtex-6 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6VLX75T			-3, -2, -1, -1L
XC6VLX130T			-3, -2, -1, -1L
XC6VLX195T			-3, -2, -1, -1L
XC6VLX240T			-3, -2, -1, -1L
XC6VLX365T			-3, -2, -1, -1L
XC6VLX550T			-2, -1, -1L
XC6VLX760			-2, -1, -1L
XC6VSX315T			-3, -2, -1, -1L
XC6VSX475T			-2, -1, -1L
XC6VHX250T			-3, -2, -1
XC6VHX255T			-3, -2, -1
XC6VHX380T			-3, -2, -1
XC6VHX565T			-2, -1
XQ6VLX130T			-2, -1, -1L
XQ6VLX240T			-2, -1, -1L
XQ6VLX550T			-1, -1L
XQ6VSX315T			-2, -1, -1L
XQ6VSX475T			-1, -1L

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 devices.

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
DIFF_SSTL18_I	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
DIFF_SSTL18_I_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL18_II	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
DIFF_SSTL18_II_DCI	0.85	0.94	1.09	1.08	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
DIFF_SSTL18_II_T_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
DIFF_SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVDS_25	0.94	1.09	1.08	1.54	2.16	1.62	1.54	2.16	1.62	ns
LVDSEXT_25	0.94	1.09	1.08	1.65	2.20	1.73	1.65	2.20	1.73	ns
HT_25	0.94	1.09	1.08	1.62	2.20	1.69	1.62	2.20	1.69	ns
BLVDS_25	0.94	1.09	1.08	1.50	3.18	1.65	1.50	3.18	1.65	ns
RSDS_25 (point to point)	0.94	1.09	1.08	1.54	2.22	1.62	1.54	2.22	1.62	ns
HSTL_I	0.91	1.06	1.06	1.56	2.44	1.71	1.56	2.44	1.71	ns
HSTL_II	0.91	1.06	1.06	1.56	2.21	1.72	1.56	2.21	1.72	ns
HSTL_III	0.91	1.06	1.06	1.54	2.50	1.69	1.54	2.50	1.69	ns
HSTL_I_18	0.91	1.06	1.06	1.58	2.43	1.72	1.58	2.43	1.72	ns
HSTL_II_18	0.91	1.06	1.06	1.62	2.30	1.78	1.62	2.30	1.78	ns
HSTL_III_18	0.91	1.06	1.06	1.54	2.49	1.69	1.54	2.49	1.69	ns
SSTL2_I	0.91	1.06	1.06	1.60	2.50	1.74	1.60	2.50	1.74	ns
SSTL2_II	0.91	1.06	1.06	1.54	2.49	1.71	1.54	2.49	1.71	ns
SSTL15	0.91	1.06	1.06	1.54	2.07	1.69	1.54	2.07	1.69	ns
LVC MOS25, Slow, 2 mA	0.57	0.66	0.70	5.46	6.01	5.63	5.46	6.01	5.63	ns
LVC MOS25, Slow, 4 mA	0.57	0.66	0.70	3.49	3.79	3.65	3.49	3.79	3.65	ns
LVC MOS25, Slow, 6 mA	0.57	0.66	0.70	2.81	3.08	2.95	2.81	3.08	2.95	ns
LVC MOS25, Slow, 8 mA	0.57	0.66	0.70	2.41	2.72	2.59	2.41	2.72	2.59	ns
LVC MOS25, Slow, 12 mA	0.57	0.66	0.70	1.95	2.23	2.10	1.95	2.23	2.10	ns
LVC MOS25, Slow, 16 mA	0.57	0.66	0.70	2.05	2.29	2.21	2.05	2.29	2.21	ns
LVC MOS25, Slow, 24 mA	0.57	0.66	0.70	1.82	2.24	1.98	1.82	2.24	1.98	ns
LVC MOS25, Fast, 2 mA	0.57	0.66	0.70	5.49	6.04	5.62	5.49	6.04	5.62	ns
LVC MOS25, Fast, 4 mA	0.57	0.66	0.70	3.50	3.82	3.65	3.50	3.82	3.65	ns
LVC MOS25, Fast, 6 mA	0.57	0.66	0.70	2.73	2.99	2.88	2.73	2.99	2.88	ns
LVC MOS25, Fast, 8 mA	0.57	0.66	0.70	2.33	2.65	2.53	2.33	2.65	2.53	ns
LVC MOS25, Fast, 12 mA	0.57	0.66	0.70	1.88	2.08	2.03	1.88	2.08	2.03	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVDCI_DV2_18	0.61	0.72	0.73	1.81	2.36	1.98	1.81	2.36	1.98	ns
LVDCI_DV2_15	0.73	0.85	0.85	1.77	2.30	1.98	1.77	2.30	1.98	ns
LVPECL_25	0.94	1.09	1.08	1.49	2.68	1.64	1.49	2.68	1.64	ns
HSTL_I_12	0.91	1.06	1.06	1.60	2.48	1.74	1.60	2.48	1.74	ns
HSTL_I_DCI	0.91	1.06	1.06	1.50	2.43	1.64	1.50	2.43	1.64	ns
HSTL_II_DCI	0.91	1.06	1.06	1.49	2.39	1.66	1.49	2.39	1.66	ns
HSTL_II_T_DCI	0.91	1.06	1.06	1.50	2.43	1.64	1.50	2.43	1.64	ns
HSTL_III_DCI	0.91	1.06	1.06	1.45	2.48	1.61	1.45	2.48	1.61	ns
HSTL_I_DCI_18	0.91	1.06	1.06	1.53	2.44	1.66	1.53	2.44	1.66	ns
HSTL_II_DCI_18	0.91	1.06	1.06	1.46	2.41	1.59	1.46	2.41	1.59	ns
HSTL_II_T_DCI_18	0.91	1.06	1.06	1.53	2.43	1.66	1.53	2.43	1.66	ns
HSTL_III_DCI_18	0.91	1.06	1.06	1.54	2.50	1.67	1.54	2.50	1.67	ns
DIFF_HSTL_I_18	0.94	1.09	1.08	1.58	2.30	1.72	1.58	2.30	1.72	ns
DIFF_HSTL_I_DCI_18	0.94	1.09	1.08	1.53	2.21	1.66	1.53	2.21	1.66	ns
DIFF_HSTL_I	0.94	1.09	1.08	1.56	2.28	1.71	1.56	2.28	1.71	ns
DIFF_HSTL_I_DCI	0.94	1.09	1.08	1.50	2.28	1.64	1.50	2.28	1.64	ns
DIFF_HSTL_II_18	0.94	1.09	1.08	1.62	2.33	1.78	1.62	2.33	1.78	ns
DIFF_HSTL_II_DCI_18	0.94	1.09	1.08	1.46	2.18	1.59	1.46	2.18	1.59	ns
DIFF_HSTL_II_T_DCI_18	0.94	1.09	1.08	1.53	2.22	1.66	1.53	2.22	1.66	ns
DIFF_HSTL_II	0.94	1.09	1.08	1.56	2.29	1.72	1.56	2.29	1.72	ns
DIFF_HSTL_II_DCI	0.94	1.09	1.08	1.49	2.26	1.66	1.49	2.26	1.66	ns
SSTL2_I_DCI	0.91	1.06	1.06	1.53	2.51	1.68	1.53	2.51	1.68	ns
SSTL2_II_DCI	0.91	1.06	1.06	1.50	2.50	1.69	1.50	2.50	1.69	ns
SSTL2_II_T_DCI	0.91	1.06	1.06	1.53	2.52	1.68	1.53	2.52	1.68	ns
SSTL18_I	0.91	1.06	1.06	1.58	2.48	1.73	1.58	2.48	1.73	ns
SSTL18_II	0.91	1.06	1.06	1.50	2.46	1.66	1.50	2.46	1.66	ns
SSTL18_I_DCI	0.91	1.06	1.06	1.51	2.49	1.65	1.51	2.49	1.65	ns
SSTL18_II_DCI	0.91	1.06	1.06	1.47	2.41	1.62	1.47	2.41	1.62	ns
SSTL18_II_T_DCI	0.91	1.06	1.06	1.51	2.49	1.65	1.51	2.49	1.65	ns
SSTL15_T_DCI	0.91	1.06	1.06	1.52	2.48	1.66	1.52	2.48	1.66	ns
SSTL15_DCI	0.91	1.06	1.06	1.52	2.48	1.66	1.52	2.48	1.66	ns
DIFF_SSTL2_I	0.94	1.09	1.08	1.60	2.34	1.74	1.60	2.34	1.74	ns
DIFF_SSTL2_I_DCI	0.94	1.09	1.08	1.53	2.25	1.68	1.53	2.25	1.68	ns
DIFF_SSTL2_II	0.94	1.09	1.08	1.54	2.29	1.71	1.54	2.29	1.71	ns
DIFF_SSTL2_II_DCI	0.94	1.09	1.08	1.50	2.23	1.69	1.50	2.23	1.69	ns
DIFF_SSTL2_II_T_DCI	0.94	1.09	1.08	1.53	2.26	1.68	1.53	2.26	1.68	ns
DIFF_SSTL18_I	0.94	1.09	1.08	1.58	2.22	1.73	1.58	2.22	1.73	ns
DIFF_SSTL18_I_DCI	0.94	1.09	1.08	1.51	2.30	1.65	1.51	2.30	1.65	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 47 shows the test setup parameters used for measuring input delay.

Table 47: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)(2)}$	$V_H^{(1)(2)}$	$V_{MEAS}^{(1)(4)(5)}$	$V_{REF}^{(1)(3)(5)}$
LVC MOS, 2.5V	LVC MOS25	0	2.5	1.25	—
LVC MOS, 1.8V	LVC MOS18	0	1.8	0.9	—
LVC MOS, 1.5V	LVC MOS15	0	1.5	0.75	—
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL, Class III	HSTL_III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	$V_{REF} - 1.00$	$V_{REF} + 1.00$	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	$1.2 - 0.125$	$1.2 + 0.125$	$0^{(6)}$	—
LVDS EXT (LVDS Extended Mode), 2.5V	LVDS EXT_25	$1.2 - 0.125$	$1.2 + 0.125$	$0^{(6)}$	—
HT (HyperTransport), 2.5V	LDT_25	$0.6 - 0.125$	$0.6 + 0.125$	$0^{(6)}$	—

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVC MOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H .
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 6.
6. The value given is the differential input voltage.

Input Serializer/Deserializer Switching Characteristics

Table 51: ISERDES Switching Characteristics

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup/Hold for Control Lines							
T _{ISCKK_BITSIP} / T _{ISCKC_BITSIP}	BITSLIP pin Setup/Hold with respect to CLKDIV	0.07/ 0.15	0.08/ 0.16	0.09/ 0.17	0.09/ 0.17	0.14/ 0.17	ns
T _{ISCKK_CE} / T _{ISCKC_CE} ⁽²⁾	CE pin Setup/Hold with respect to CLK (for CE1)	0.20/ 0.03	0.25/ 0.04	0.27/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T _{ISCKK_CE2} / T _{ISCKC_CE2} ⁽²⁾	CE pin Setup/Hold with respect to CLKDIV (for CE2)	0.01/ 0.27	0.01 0.29	0.01/ 0.31	0.01/ 0.31	−0.05/ 0.35	ns
Setup/Hold for Data Lines							
T _{ISDCK_D} / T _{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.07/ 0.08	0.08/ 0.09	0.09/ 0.11	0.09/ 0.11	0.11/ 0.19	ns
T _{ISDCK_DDLY} / T _{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY) ⁽¹⁾	0.10/ 0.05	0.12/ 0.06	0.14/ 0.07	0.14/ 0.07	0.16/ 0.15	ns
T _{ISDCK_D_DDR} / T _{ISCKD_D_DDR}	D pin Setup/Hold with respect to CLK at DDR mode	0.07/ 0.08	0.08/ 0.09	0.09/ 0.11	0.09/ 0.11	0.11/ 0.19	ns
T _{ISDCK_DDLY_DDR} / T _{ISCKD_DDLY_DDR}	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY) ⁽¹⁾	0.10/ 0.05	0.12/ 0.06	0.14/ 0.07	0.14/ 0.07	0.16/ 0.15	ns
Sequential Delays							
T _{ISCKO_Q}	CLKDIV to out at Q pin	0.57	0.66	0.75	0.80	0.88	ns
Propagation Delays							
T _{ISDO_DO}	D input to DO output pin	0.19	0.22	0.25	0.25	0.28	ns

Notes:

- Recorded at 0 tap value.
- T_{ISCK_CE2} and T_{ISCK_CE2} are reported as $T_{ISCK_CE} / T_{ISCK_CE}$ in TRACE report.

Block RAM and FIFO Switching Characteristics

Table 57: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Block RAM and FIFO Clock-to-Out Delays						
T _{RCKO_DO} and T _{RCKO_DO_REG} ⁽¹⁾	Clock CLK to DOUT output (without output register) ⁽²⁾⁽³⁾	1.60	1.79	2.08	2.36	ns, Max
	Clock CLK to DOUT output (with output register) ⁽⁴⁾⁽⁵⁾	0.60	0.66	0.75	0.83	ns, Max
T _{RCKO_DO_ECC} and T _{RCKO_DO_ECC_REG}	Clock CLK to DOUT output with ECC (without output register) ⁽²⁾⁽³⁾	2.62	2.89	3.30	3.73	ns, Max
	Clock CLK to DOUT output with ECC (with output register) ⁽⁴⁾⁽⁵⁾	0.71	0.77	0.86	0.94	ns, Max
T _{RCKO_CASC} and T _{RCKO_CASC_REG}	Clock CLK to DOUT output with Cascade (without output register) ⁽²⁾	2.49	2.77	3.18	3.61	ns, Max
	Clock CLK to DOUT output with Cascade (with output register) ⁽⁴⁾	1.29	1.41	1.58	1.79	ns, Max
T _{RCKO_FLAGS}	Clock CLK to FIFO flags outputs ⁽⁶⁾	0.74	0.81	0.91	0.98	ns, Max
T _{RCKO_POINTERS}	Clock CLK to FIFO pointers outputs ⁽⁷⁾	0.90	0.98	1.09	1.21	ns, Max
T _{RCKO_SDBIT_ECC} and T _{RCKO_SDBIT_ECC_REG}	Clock CLK to BITERR (with output register)	0.62	0.68	0.76	0.82	ns, Max
	Clock CLK to BITERR (without output register)	2.21	2.46	2.84	3.23	ns, Max
T _{RCKO_PARITY_ECC}	Clock CLK to ECCPARITY in ECC encode only mode	0.86	0.94	1.06	1.18	ns, Max
T _{RCKO_RDADDR_ECC} and T _{RCKO_RDADDR_ECC_REG}	Clock CLK to RDADDR output with ECC (without output register)	0.73	0.79	0.90	1.00	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.76	0.82	0.92	1.02	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{RCKC_ADDR} /T _{RCKC_ADDR}	ADDR inputs ⁽⁸⁾	0.47/ 0.27	0.53/ 0.29	0.62/ 0.32	0.66/ 0.34	ns, Min
T _{RDCK_DI} /T _{RCKD_DI}	DIN inputs ⁽⁹⁾	0.84/ 0.30	0.95/ 0.32	1.11/ 0.34	1.26/ 0.36	ns, Min
T _{RDCK_DI_ECC} /T _{RCKD_DI_ECC}	DIN inputs with block RAM ECC in standard mode ⁽⁹⁾	0.47/ 0.30	0.52/ 0.32	0.59/ 0.34	0.68/ 0.36	ns, Min
	DIN inputs with block RAM ECC encode only ⁽⁹⁾	0.68/ 0.30	0.75/ 0.32	0.85/ 0.34	0.97/ 0.36	ns, Min
	DIN inputs with FIFO ECC in standard mode ⁽⁹⁾	0.77/ 0.30	0.87/ 0.32	1.02/ 0.34	1.16/ 0.36	ns, Min
T _{RCKC_CLK} /T _{RCKC_CLK}	Inject single/double bit error in ECC mode	0.90/ 0.27	1.02/ 0.28	1.20/ 0.29	1.56/ 0.29	ns, Min
T _{RCKC_RDEN} /T _{RCKC_RDEN}	Block RAM Enable (EN) input	0.31/ 0.26	0.35/ 0.27	0.41/ 0.30	0.44/ 0.31	ns, Min
T _{RCKC_REGCE} /T _{RCKC_REGCE}	CE input of output register	0.18/ 0.25	0.19/ 0.27	0.22/ 0.31	0.24/ 0.33	ns, Min
T _{RCKC_RSTREG} /T _{RCKC_RSTREG}	Synchronous RSTREG input	0.22/ 0.23	0.24/ 0.24	0.28/ 0.26	0.31/ 0.27	ns, Min
T _{RCKC_RSTRAM} /T _{RCKC_RSTRAM}	Synchronous RSTRAM input	0.32/ 0.23	0.36/ 0.24	0.41/ 0.27	0.46/ 0.29	ns, Min

Table 58: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
$T_{\text{DSPDCK_RSTP_PREG}} / T_{\text{DSPCKD_RSTP_PREG}}$	RSTP input to P register CLK	0.26/ 0.04	0.30/ 0.04	0.35/ 0.05	0.35/ 0.05	0.43/ 0.06	ns
Combinatorial Delays from Input Pins to Output Pins							
$T_{\text{DSPDO_}\{A, B\}_ \{P, \text{CARRYOUT}\}_ \text{MULT}}$	{A, B} input to {P, CARRYOUT} output using multiplier	3.76	4.29	5.08	5.08	5.87	ns
$T_{\text{DSPDO_D_}\{P, \text{CARRYOUT}\}_ \text{MULT}}$	D input to {P, CARRYOUT} output using multiplier	3.57	4.07	4.82	4.82	5.57	ns
$T_{\text{DSPDO_}\{A, B\}_ \{P, \text{CARRYOUT}\}}$	{A, B} input to {P, CARRYOUT} output not using multiplier	1.55	1.76	2.07	2.07	2.41	ns
$T_{\text{DSPDO_}\{C, \text{CARRYIN}\}_ \{P, \text{CARRYOUT}\}}$	{C, CARRYIN} input to {P, CARRYOUT} output	1.38	1.56	1.83	1.83	2.13	ns
Combinatorial Delays from Input Pins to Cascading Output Pins							
$T_{\text{DSPDO_}\{A, B\}_ \{ACOUT, BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.49	0.56	0.65	0.65	0.73	ns
$T_{\text{DSPDO_}\{A, B\}_ \{PCOUT, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}_ \text{MULT}}$	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.87	4.42	5.24	5.24	6.09	ns
$T_{\text{DSPDO_D_}\{PCOUT, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}_ \text{MULT}}$	D input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.66	4.17	4.94	4.94	5.76	ns
$T_{\text{DSPDO_}\{A, B\}_ \{PCOUT, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}$	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.64	1.86	2.19	2.19	2.60	ns
$T_{\text{DSPDO_}\{C, \text{CARRYIN}\}_ \{PCOUT, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}$	{C, CARRYIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.46	1.66	1.95	1.95	2.32	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins							
$T_{\text{DSPDO_}\{ACIN, BCIN\}_ \{P, \text{CARRYOUT}\}_ \text{MULT}}$	{ACIN, BCIN} input to {P, CARRYOUT} output using multiplier	3.67	4.19	4.97	4.97	5.75	ns
$T_{\text{DSPDO_}\{ACIN, BCIN\}_ \{P, \text{CARRYOUT}\}}$	{ACIN, BCIN} input to {P, CARRYOUT} output not using multiplier	1.43	1.63	1.92	1.92	2.25	ns
$T_{\text{DSPDO_}\{ACIN, BCIN\}_ \{ACOUT, BCOUT\}}$	{ACIN, BCIN} input to {ACOUT, BCOUT} output	0.36	0.42	0.49	0.49	0.56	ns
$T_{\text{DSPDO_}\{ACIN, BCIN\}_ \{PCOUT, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}_ \text{MULT}}$	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.76	4.29	5.10	5.10	5.94	ns
$T_{\text{DSPDO_}\{ACIN, BCIN\}_ \{PCOUT, \text{CARRYCASCOUT}, \text{MULTSIGNOUT}\}}$	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.52	1.73	2.05	2.05	2.44	ns
$T_{\text{DSPDO_}\{PCIN, \text{CARRYCASCIN}, \text{MULTSIGNIN}\}_ \{P, \text{CARRYOUT}\}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {P, CARRYOUT} output	1.19	1.35	1.60	1.60	1.87	ns

Table 59: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T _{SMCKBY}	CCLK to BUSY out in readback at 2.5V	6	6	6	7	ns, Max
	CCLK to BUSY out in readback at 1.8V	6	6	6	7	ns, Max
F _{SMCK}	Maximum Frequency with respect to nominal CCLK	100	100	100	70	MHz, Max
F _{RBCK}	Maximum Readback Frequency with respect to nominal CCLK	100	100	100	60	MHz, Max
F _{MCCKTOL}	Frequency tolerance, master mode with respect to nominal CCLK	55	55	55	60	%
Boundary-Scan Port Timing Specifications						
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI Setup time before TCK/ Hold time after TCK	3.0/2.0	3.0/2.0	3.0/2.0	4.0/2.0	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output valid at 2.5V	6	6	6	7	ns, Max
	TCK falling edge to TDO output valid at 1.8V	6	6	6	7	ns, Max
F _{TCK}	Maximum configuration TCK clock frequency	66	66	66	33	MHz, Max
F _{TCKB_MIN}	Minimum boundary-scan TCK clock frequency when using IEEE Std 1149.6 (AC-JTAG). Minimum operating temperature for IEEE Std 1149.6 is 0°C.	15	15	15	15	MHz, Min
F _{TCKB}	Maximum boundary-scan TCK clock frequency	66	66	66	33	MHz, Max
BPI Master Flash Mode Programming Switching						
T _{BPICCO} ⁽²⁾	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 2.5V	6	6	6	7	ns
	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 1.8V	6	6	6	7	ns
T _{BPIDCC} /T _{BPICCD}	Setup/Hold on D[15:0] data input pins	4.0/0.0	4.0/0.0	4.0/0.0	5.0/0.0	ns
T _{INITADDR}	Minimum period of initial ADDR[25:0] address cycles	3	3	3	3	CCLK cycles
SPI Master Flash Mode Programming Switching						
T _{SPIDCC} /T _{SPIDCCD}	DIN Setup/Hold before/after the rising CCLK edge	3.0/0.0	3.0/0.0	3.0/0.0	3.5/0.0	ns
T _{SPICCM}	MOSI clock to out at 2.5V	6	6	6	7	ns
	MOSI clock to out at 1.8V	6	6	6	7	ns
T _{SPICFC}	FCS_B clock to out at 2.5V	6	6	6	7	ns
	FCS_B clock to out at 1.8V	6	6	6	7	ns
T _{FSINIT} /T _{FSINITH}	FS[2:0] to INIT_B rising edge Setup and Hold	2	2	2	2	µs
CCLK Output (Master Modes)						
T _{MCCKL}	Master CCLK clock Low time duty cycle	45/55	45/55	45/55	40/60	%, Min/Max
T _{MCCKH}	Master CCLK clock High time duty cycle	45/55	45/55	45/55	40/60	%, Min/Max
CCLK Input (Slave Modes)						
T _{SCCKL}	Slave CCLK clock minimum Low time	2.5	2.5	2.5	2.5	ns, Min
T _{SCCKH}	Slave CCLK clock minimum High time	2.5	2.5	2.5	2.5	ns, Min
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
F _{DCK}	Maximum frequency for DCLK	200	200	200	200	MHz
T _{MMCMCKD_DADDR} / T _{MMCMCKD_DADDR}	DADDR Setup/Hold	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns

Table 59: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{\text{MMCMDCK_DI}}/$ $T_{\text{MMCCKD_DI}}$	DI Setup/Hold	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{\text{MMCMDCK_DEN}}/$ $T_{\text{MMCCKD_DEN}}$	DEN Setup/Hold time	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{\text{MMCMDCK_DWE}}/$ $T_{\text{MMCCKD_DWE}}$	DWE Setup/Hold time	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{\text{MMCCKO_DO}}$	CLK to out of DO ⁽³⁾	2.60	3.02	3.64	3.68	ns
$T_{\text{MMCCKO_DRDY}}$	CLK to out of DRDY	0.32	0.34	0.38	0.38	ns

Notes:

1. To support longer delays in configuration, use the design solutions described in [UG360: Virtex-6 FPGA Configuration User Guide](#).
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
3. DO will hold until next DRP operation.

Clock Buffers and Networks

Table 60: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	Devices	Speed Grade				Units
			-3	-2	-1	-1L	
$T_{\text{BCCCK_CE}}/T_{\text{BCCCK_CE}}^{(1)}$	CE pins Setup/Hold	All	0.11/ 0.00	0.13/ 0.00	0.16/ 0.00	0.13/ 0.00	ns
$T_{\text{BCCCK_S}}/T_{\text{BCCCK_S}}^{(1)}$	S pins Setup/Hold	All	0.11/ 0.00	0.13/ 0.00	0.16/ 0.00	0.13/ 0.00	ns
$T_{\text{BCKO_O}}^{(2)}$	BUFGCTRL delay from I0/I1 to O	All	0.07	0.08	0.10	0.10	ns
Maximum Frequency							
F_{MAX}	Global clock tree (BUFG)	All except LX760	800	750	700	667	MHz
		LX760	N/A	700	700	667	MHz

Notes:

1. $T_{\text{BCCCK_CE}}$ and $T_{\text{BCCCK_S}}$ must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. $T_{\text{BCKO_O}}$ (BUFG delay from I0 to O) values are the same as $T_{\text{BCKO_O}}$ values.

Table 61: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{\text{BIOCKO_O}}$	Clock to out delay from I to O	0.14	0.16	0.18	0.21	ns
Maximum Frequency						
F_{MAX}	I/O clock tree (BUFIO)	800	800	710	710	MHz

Table 62: Regional Clock Switching Characteristics (BUFR)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{\text{BRCKO_O}}$	Clock to out delay from I to O	0.56	0.62	0.73	0.82	ns
$T_{\text{BRCKO_O_BYP}}$	Clock to out delay from I to O with Divide Bypass attribute set	0.28	0.31	0.36	0.41	ns

Table 64: MMCM Specification (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
RST _{MINPULSE}	Minimum Reset Pulse Width	1.5	1.5	1.5	1.5	ns
F _{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized ⁽⁹⁾	550	500	450	450	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300	300	300	300	MHz
F _{PFDMIN}	Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	135	135	135	135	MHz
	Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	10	10	10	10	MHz
T _{FBDELAY}	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				
T _{MMCMCK_PSEN} / T _{MMCMCKD_PSEN}	Setup and Hold of Phase Shift Enable	1.04 0.00	1.04 0.00	1.04 0.00	1.04 0.00	ns
T _{MMCMCK_PINCDEC} / T _{MMCMCKD_PINCDEC}	Setup and Hold of Phase Shift Increment/Decrement	1.04 0.00	1.04 0.00	1.04 0.00	1.04 0.00	ns
T _{MMCMCKO_PSDONE}	Phase Shift Clock-to-Out of PSDONE	0.32	0.34	0.38	0.38	ns

Notes:

1. When DIVCLK_DIVIDE = 3 or 4, F_{INMAX} is 315 MHz.
2. This duty cycle specification does not apply to the GTH_QUAD (GTH) to MMCM connection. The GTH transceivers drive the MMCMs at the following maximum frequencies: 323 MHz for -1 speed grade devices, 350 MHz for -2 speed grade devices, or 350 MHz for -3 speed grade devices.
3. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. The static offset is measured between any MMCM outputs with identical phase.
5. Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
6. Includes global clock buffer.
7. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
8. When CASCADE4_OUT = TRUE, F_{OUTMIN} is 0.036 MHz.
9. In ISE software 12.3 (or earlier versions supporting the Virtex-6 family), the phase frequency detector Optimized bandwidth setting is equivalent to the High bandwidth setting. Starting with ISE software 12.4, the Optimized bandwidth setting is automatically adjusted to Low when the software can determine that the phase frequency detector input is less than 135 MHz.

Virtex-6 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 65. Values are expressed in nanoseconds unless otherwise noted.

Table 65: Global Clock Input to Output Delay Without MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>without</i> MMCM.							
T _{ICKOF}	Global Clock input and OUTFF <i>without</i> MMCM	XC6VLX75T	4.91	5.32	5.88	6.02	ns
		XC6VLX130T	4.89	5.33	6.00	6.13	ns
		XC6VLX195T	5.02	5.46	6.13	6.27	ns
		XC6VLX240T	5.02	5.46	6.13	6.27	ns
		XC6VLX365T	5.30	5.75	6.43	6.37	ns
		XC6VLX550T	N/A	6.02	6.72	6.60	ns
		XC6VLX760	N/A	6.26	6.97	6.87	ns
		XC6VSX315T	5.40	5.85	6.54	6.49	ns
		XC6VSX475T	N/A	6.01	6.71	6.61	ns
		XC6VHX250T	5.18	5.63	6.30	N/A	ns
		XC6VHX255T	5.20	5.66	6.34	N/A	ns
		XC6VHX380T	5.38	5.84	6.53	N/A	ns
		XC6VHX565T	N/A	6.03	6.71	N/A	ns
		XQ6VLX130T	N/A	5.33	6.00	6.13	ns
		XQ6VLX240T	N/A	5.46	6.13	6.27	ns
		XQ6VLX550T	N/A	N/A	6.72	6.60	ns
		XQ6VSX315T	N/A	5.85	6.54	6.49	ns
		XQ6VSX475T	N/A	N/A	6.71	6.61	ns

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Virtex-6 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 68. Values are expressed in nanoseconds unless otherwise noted.

Table 68: Global Clock Input Setup and Hold Without MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. ⁽¹⁾							
T _{PSFD} / T _{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF ⁽²⁾ without MMCM	XC6VLX75T	1.33/ 0.03	1.44/ 0.03	1.75/ 0.03	2.18/ −0.22	ns
		XC6VLX130T	1.31/ −0.08	1.54/ −0.08	1.88/ −0.08	2.31/ −0.12	ns
		XC6VLX195T	1.36/ −0.11	1.60/ −0.11	1.97/ −0.11	2.40/ −0.25	ns
		XC6VLX240T	1.36/ −0.11	1.60/ −0.11	1.97/ −0.11	2.40/ −0.25	ns
		XC6VLX365T	1.79/ −0.28	1.87/ −0.28	2.17/ −0.28	2.48/ −0.24	ns
		XC6VLX550T	N/A	2.22/ −0.12	2.36/ −0.12	2.77/ −0.26	ns
		XC6VLX760	N/A	2.19/ −0.24	2.35/ −0.24	2.71/ −0.21	ns
		XC6VSX315T	1.75/ −0.09	1.85/ −0.09	2.06/ −0.09	2.47/ −0.24	ns
		XC6VSX475T	N/A	2.14/ −0.14	2.31/ −0.14	2.71/ −0.30	ns
		XC6VHX250T	1.93/ −0.22	2.04/ −0.22	2.25/ −0.22	N/A	ns
		XC6VHX255T	1.81/ −0.33	2.11/ −0.33	2.56/ −0.33	N/A	ns
		XC6VHX380T	1.93/ −0.11	2.04/ −0.11	2.25/ −0.11	N/A	ns
		XC6VHX565T	N/A	2.20/ −0.12	2.39/ −0.12	N/A	ns
		XQ6VLX130T	N/A	1.54/ −0.08	1.88/ −0.08	2.31/ −0.12	ns
		XQ6VLX240T	N/A	1.60/ −0.11	1.97/ −0.11	2.40/ −0.25	ns
		XQ6VLX550T	N/A	N/A	2.36/ −0.12	2.77/ −0.26	ns
		XQ6VSX315T	N/A	1.85/ −0.09	2.06/ −0.09	2.47/ −0.24	ns
		XQ6VSX475T	N/A	N/A	2.31/ −0.14	2.71/ −0.30	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch
- A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 70: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard. ⁽¹⁾							
T _{PSMMCMCC} / T _{PHMMCMCC}	No Delay Clock-capable Clock Input and IFF ⁽²⁾ with MMCM	XC6VLX75T	1.56/ −0.25	1.69/ −0.25	1.86/ −0.25	1.91/ −0.15	ns
		XC6VLX130T	1.64/ −0.25	1.78/ −0.25	1.95/ −0.25	2.00/ −0.14	ns
		XC6VLX195T	1.65/ −0.24	1.79/ −0.24	1.96/ −0.24	2.01/ −0.15	ns
		XC6VLX240T	1.65/ −0.24	1.79/ −0.24	1.96/ −0.24	2.01/ −0.15	ns
		XC6VLX365T	1.66/ −0.25	1.79/ −0.25	1.97/ −0.25	2.02/ −0.15	ns
		XC6VLX550T	N/A	1.97/ −0.24	2.16/ −0.24	2.19/ −0.14	ns
		XC6VLX760	N/A	2.39/ −0.20	2.63/ −0.20	2.21/ −0.10	ns
		XC6VSX315T	1.67/ −0.25	1.80/ −0.25	1.98/ −0.25	2.03/ −0.16	ns
		XC6VSX475T	N/A	1.98/ −0.29	2.17/ −0.29	2.21/ −0.20	ns
		XC6VHX250T	1.63/ −0.24	1.76/ −0.24	1.94/ −0.24	N/A	ns
		XC6VHX255T	1.63/ −0.19	1.76/ −0.19	1.99/ −0.19	N/A	ns
		XC6VHX380T	1.80/ −0.23	1.94/ −0.23	2.13/ −0.23	N/A	ns
		XC6VHX565T	N/A	1.94/ −0.08	2.13/ −0.08	N/A	ns
		XQ6VLX130T	N/A	1.78/ −0.25	1.95/ −0.25	2.00/ −0.14	ns
		XQ6VLX240T	N/A	1.79/ −0.24	1.96/ −0.24	2.01/ −0.15	ns
		XQ6VLX550T	N/A	N/A	2.16/ −0.24	2.19/ −0.14	ns
		XQ6VSX315T	N/A	1.80/ −0.25	1.98/ −0.25	2.03/ −0.16	ns
		XQ6VSX475T	N/A	N/A	2.17/ −0.29	2.21/ −0.20	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 72: Package Skew

Symbol	Description	Device	Package	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	XC6VLX75T	FF484	95	ps
			FF784	146	ps
		XC6VLX130T	FF484	95	ps
			FF784	146	ps
			FF1156	165	ps
		XC6VLX195T	FF784	145	ps
			FF1156	182	ps
		XC6VLX240T	FF784	146	ps
			FF1156	182	ps
			FF1759	187	ps
		XC6VLX365T	FF1156	189	ps
			FF1759	184	ps
		XC6VLX550T	FF1759	196	ps
			FF1760	249	ps
		XC6VLX760	FF1760	236	ps
		XC6VSX315T	FF1156	168	ps
			FF1759	190	ps
		XC6VSX475T	FF1156	168	ps
			FF1759	204	ps
		XC6VHX250T	FF1154	166	ps
		XC6VHX255T	FF1155	168	ps
			FF1923	228	ps
		XC6VHX380T	FF1154	159	ps
			FF1155	172	ps
			FF1923	227	ps
			FF1924	220	ps
		XC6VHX565T	FF1923	232	ps
			FF1924	197	ps
		XQ6VLX130T	RF784	146	ps
			RF1156	165	ps
			FFG1156	165	ps
		XQ6VLX240T	RF784	146	ps
			RF1156	182	ps
			FFG1156	182	ps
			RF1759	187	ps
		XQ6VLX550T	RF1759	196	ps
		XQ6VSX315T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	190	ps
		XQ6VSX475T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	204	ps

Notes:

- These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
- Package trace length information is available for these device/package combinations. This information can be used to deskew the package.