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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	24600
Number of Logic Elements/Cells	314880
Total RAM Bits	25952256
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1156-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vsx315t-3ffg1156c

Table 3: DC Characteristics Over Recommended Operating Conditions (1)(2)

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	10	μA
I_L	Input or output leakage current per pin (sample-tested)	–	–	10	μA
$C_{IN}^{(3)}$	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 2.5V$	20	–	80	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.8V$	8	–	40	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.5V$	5	–	30	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.2V$	1	–	20	μA
I_{RPD}	Pad pull-down (when selected) @ $V_{IN} = 2.5V$	3	–	80	μA
I_{BATT}	Battery supply current	–	–	150	nA
n	Temperature diode ideality factor	–	1.0002	–	n
r	Series resistance	–	5	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst case process at 25°C.
3. This measurement represents the die capacitance at the pad, not including the package.

Table 4: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed and Temperature Grade						Units
			-3 (C)	-2 (C, E, & I)	-1 (C & I)	-1 (I & M) ⁽²⁾	-1L (C)	-1L (I) ⁽¹⁾	
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current	XC6VLX75T	45	45	45	N/A	45	45	mA
		XC6VLX130T	75	75	75	N/A	75	75	mA
		XC6VLX195T	113	113	113	N/A	113	113	mA
		XC6VLX240T	135	135	135	N/A	135	135	mA
		XC6VLX365T	191	191	191	N/A	191	191	mA
		XC6VLX550T ⁽³⁾	N/A	286	286	N/A	286	286	mA
		XC6VLX760 ⁽³⁾	N/A	387	387	N/A	387	387	mA
		XC6VSX315T	186	186	186	N/A	186	186	mA
		XC6VSX475T ⁽³⁾	N/A	279	279	N/A	279	279	mA
		XC6VHX250T	152	152	152	N/A	N/A	N/A	mA
		XC6VHX255T	152	152	152	N/A	N/A	N/A	mA
		XC6VHX380T ⁽⁴⁾	227	227	227	N/A	N/A	N/A	mA
		XC6VHX565T ⁽⁵⁾	N/A	315	315	N/A	N/A	N/A	mA
		XQ6VLX130T ⁽⁶⁾	N/A	75	N/A	75	N/A	75	mA
		XQ6VLX240T ⁽⁶⁾	N/A	135	N/A	135	N/A	135	mA
		XQ6VLX550T ⁽⁷⁾	N/A	N/A	N/A	286	N/A	286	mA
		XQ6VSX315T ⁽⁶⁾	N/A	186	N/A	186	N/A	186	mA
		XQ6VSX475T ⁽⁷⁾	N/A	N/A	N/A	279	N/A	279	mA

Notes:

- Typical values are specified at nominal voltage, 85°C junction temperatures (T_j). -1 and -2 industrial (I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. -1L industrial temperature range devices have the values specified in this column.
- Use the XPE tool to calculate 125°C values for -1M temperature range devices.
- The -2E extended temperature range (T_j = 0°C to +100°C) is only available in these devices. The -2I temperature range (T_j = -40°C to +100°C) is available for all other devices except the XC6VHX565T.
- The XC6VHX380T is available with both -2E and -2I temperature ranges.
- The XC6VHX565T is only available in the following temperature ranges: -1C, -1I, -2C, and -2E.
- The XQ6VLX130T, XQ6VLX240T, and XQ6VSX315T are available in -2I, -1I, -1M, and -1LI temperature ranges.
- The XQ6VLX550T and the XQ6VSX475T are only available in -1I and -1LI temperature ranges.
- Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
- If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPE or XPower Analyzer (XPA) tools.

Table 6: Power Supply Ramp Time

Symbol	Description	Ramp Time	Units
V_{CCINT}	Internal supply voltage relative to GND	0.20 to 50.0	ms
V_{CCO}	Output drivers supply voltage relative to GND	0.20 to 50.0	ms
V_{CCAUX}	Auxiliary supply voltage relative to GND	0.20 to 50.0	ms

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 7: SelectIO DC Input and Output Levels

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVC MOS25, LVDCI25	-0.3	0.7	1.7	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	Note(3)	Note(3)
LVC MOS18, LVDCI18	-0.3	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.3$	0.45	$V_{CCO} - 0.45$	Note(4)	Note(4)
LVC MOS15, LVDCI15	-0.3	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.3$	25% V_{CCO}	75% V_{CCO}	Note(4)	Note(4)
LVC MOS12	-0.3	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.3$	25% V_{CCO}	75% V_{CCO}	Note(5)	Note(5)
HSTL I ₁₂	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	25% V_{CCO}	75% V_{CCO}	6.3	6.3
HSTL I ⁽²⁾	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	8	-8
HSTL II ⁽²⁾	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	16	-16
HSTL III ⁽²⁾	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	24	-8
DIFF HSTL I ⁽²⁾	-0.3	50% $V_{CCO} - 0.1$	50% $V_{CCO} + 0.1$	$V_{CCO} + 0.3$	—	—	—	—
DIFF HSTL II ⁽²⁾	-0.3	50% $V_{CCO} - 0.1$	50% $V_{CCO} + 0.1$	$V_{CCO} + 0.3$	—	—	—	—
SSTL2 I	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCO} + 0.3$	$V_{TT} - 0.61$	$V_{TT} + 0.61$	8.1	-8.1
SSTL2 II	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCO} + 0.3$	$V_{TT} - 0.81$	$V_{TT} + 0.81$	16.2	-16.2
DIFF SSTL2 I	-0.3	50% $V_{CCO} - 0.15$	50% $V_{CCO} + 0.15$	$V_{CCO} + 0.3$	—	—	—	—
DIFF SSTL2 II	-0.3	50% $V_{CCO} - 0.15$	50% $V_{CCO} + 0.15$	$V_{CCO} + 0.3$	—	—	—	—
SSTL18 I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.3$	$V_{TT} - 0.47$	$V_{TT} + 0.47$	6.7	-6.7
SSTL18 II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.3$	$V_{TT} - 0.60$	$V_{TT} + 0.60$	13.4	-13.4
DIFF SSTL18 I	-0.3	50% $V_{CCO} - 0.125$	50% $V_{CCO} + 0.125$	$V_{CCO} + 0.3$	—	—	—	—
DIFF SSTL18 II	-0.3	50% $V_{CCO} - 0.125$	50% $V_{CCO} + 0.125$	$V_{CCO} + 0.3$	—	—	—	—
SSTL15	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	$V_{TT} - 0.175$	$V_{TT} + 0.175$	14.3	14.3

Notes:

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. Supported drive strengths of 2, 4, 6, or 8 mA.
6. For detailed interface specific DC voltage levels, see [UG361](#): Virtex-6 FPGA SelectIO Resources User Guide.

HT DC Specifications (HT_25)

Table 8: HT DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage for XC devices	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	480	600	885	mV
	Differential Output Voltage for XQ devices		480	600	930	mV
ΔV_{OD}	Change in V_{OD} Magnitude		-15	—	15	mV
V_{OCM}	Output Common Mode Voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	440	600	760	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		-15	—	15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		-15	—	15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		-15	—	15	mV

LVDS DC Specifications (LVDS_25)

Table 9: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	—	—	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.825	—	—	V
V_{ODIFF}	Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage for XC devices	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
	Output Common-Mode Voltage for XQ devices		1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 10: Extended LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	—	—	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.715	—	—	V
V_{ODIFF}	Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High for XC devices	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	350	—	840	mV
	Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High for XQ devices		350	—	850	mV
V_{OCM}	Output Common-Mode Voltage for XC devices	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
	Output Common-Mode Voltage for XQ devices		1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	—	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ± 350 mV	0.3	1.2	2.2	V

Table 16: GTX Transceiver Quiescent Supply Current (per Lane) ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Description	Typ ⁽⁴⁾	Max	Units
I_{MGTAVTTQ}	Quiescent MGTAVTT supply current for one GTX transceiver	0.9	Note 2	mA
I_{MGTAVCCQ}	Quiescent MGTAVCC supply current for one GTX transceiver	3.5		mA

Notes:

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.
3. GTX transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX transceivers.
4. Typical values are specified at nominal voltage, 25°C.

GTX Transceiver DC Input and Output Levels

Table 17 summarizes the DC output specifications of the GTX transceivers in Virtex-6 FPGAs. Consult [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#) for further details.

Table 17: GTX Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled ≤ 4.25 Gb/s	125	–	2000	mV
		External AC coupled > 4.25 Gb/s	175	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled MGTAVTT = 1.2V	–400	–	MGTAVTT	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTT = 1.2V	–	2/3 MGTAVTT	–	mV
DV_{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	–	–	1000	mV
V_{CMOUTDC}	DC common mode output voltage.	Equation based	$\text{MGTAVTT} - DV_{\text{PPOUT}}/4$			mV
R_{IN}	Differential input resistance		80	100	130	Ω
R_{OUT}	Differential output resistance		80	100	120	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	8	ps
C_{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#) and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

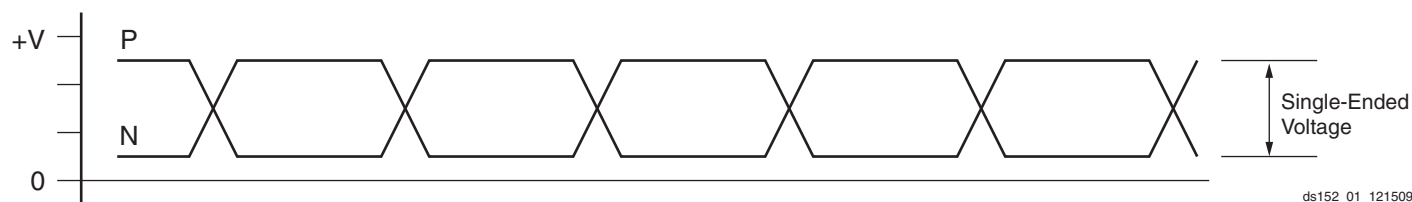


Figure 1: Single-Ended Peak-to-Ppeak Voltage

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Table 23: GTX Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTXTX}	Serial data rate range		0.480	–	F _{GTXMAX}	Gb/s
T _{RTX}	TX Rise time	20%–80%	–	120	–	ps
T _{FTX}	TX Fall time	80%–20%	–	120	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	350	ps
V _{TXOOBVDPP}	Electrical idle amplitude		–	–	15	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		–	–	75	ns
TJ _{6.5}	Total Jitter ⁽²⁾⁽³⁾	6.5 Gb/s	–	–	0.33	UI
DJ _{6.5}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.17	UI
TJ _{5.0}	Total Jitter ⁽²⁾⁽³⁾	5.0 Gb/s	–	–	0.33	UI
DJ _{5.0}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.15	UI
TJ _{4.25}	Total Jitter ⁽²⁾⁽³⁾	4.25 Gb/s	–	–	0.33	UI
DJ _{4.25}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.14	UI
TJ _{3.75}	Total Jitter ⁽²⁾⁽³⁾	3.75 Gb/s	–	–	0.34	UI
DJ _{3.75}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.16	UI
TJ _{3.125}	Total Jitter ⁽²⁾⁽³⁾	3.125 Gb/s	–	–	0.2	UI
DJ _{3.125}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.1	UI
TJ _{3.125L}	Total Jitter ⁽²⁾⁽³⁾	3.125 Gb/s ⁽⁴⁾	–	–	0.35	UI
DJ _{3.125L}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.16	UI
TJ _{2.5}	Total Jitter ⁽²⁾⁽³⁾	2.5 Gb/s ⁽⁵⁾	–	–	0.20	UI
DJ _{2.5}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.08	UI
TJ _{1.25}	Total Jitter ⁽²⁾⁽³⁾	1.25 Gb/s ⁽⁶⁾	–	–	0.15	UI
DJ _{1.25}	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.06	UI
TJ ₆₀₀	Total Jitter ⁽²⁾⁽³⁾	600 Mb/s	–	–	0.1	UI
DJ ₆₀₀	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.03	UI
TJ ₄₈₀	Total Jitter ⁽²⁾⁽³⁾	480 Mb/s	–	–	0.1	UI
DJ ₄₈₀	Deterministic Jitter ⁽²⁾⁽³⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
- Using PLL_DIVSEL_FB = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 1e⁻¹².
- PLL frequency at 1.5625 GHz and OUTDIV = 1.
- PLL frequency at 2.5 GHz and OUTDIV = 2.
- PLL frequency at 2.5 GHz and OUTDIV = 4.

Table 24: GTX Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
F _{GTXRX}	Serial data rate	RX oversampler not enabled	0.600	–	F _{GTXMAX}	Gb/s
		RX oversampler enabled	0.480	–	0.600	Gb/s
T _{RXELECIDLE}	Time for RXELECIdle to respond to loss or restoration of data		–	75	–	ns
RX _{OOBVDPP}	OOB detect threshold peak-to-peak		60	–	150	mV
RX _{SST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated @ 33 KHz	–5000	–	0	ppm
RX _{RL}	Run length (CID)	Internal AC capacitor bypassed	–	–	512	UI
RX _{PPMTOL}	Data/REFCLK PPM offset tolerance	CDR 2 nd -order loop disabled	–200	–	200	ppm
		CDR 2 nd -order loop enabled	–2000	–	2000	ppm
SJ Jitter Tolerance ⁽²⁾						
JT_SJ _{6.5}	Sinusoidal Jitter ⁽³⁾	6.5 Gb/s	0.44	–	–	UI
JT_SJ _{5.0}	Sinusoidal Jitter ⁽³⁾	5.0 Gb/s	0.44	–	–	UI
JT_SJ _{4.25}	Sinusoidal Jitter ⁽³⁾	4.25 Gb/s	0.44	–	–	UI
JT_SJ _{3.75}	Sinusoidal Jitter ⁽³⁾	3.75 Gb/s	0.44	–	–	UI
JT_SJ _{3.125}	Sinusoidal Jitter ⁽³⁾	3.125 Gb/s	0.45	–	–	UI
JT_SJ _{3.125L}	Sinusoidal Jitter ⁽³⁾	3.125 Gb/s ⁽⁴⁾	0.45	–	–	UI
JT_SJ _{2.5}	Sinusoidal Jitter ⁽³⁾	2.5 Gb/s ⁽⁵⁾	0.5	–	–	UI
JT_SJ _{1.25}	Sinusoidal Jitter ⁽³⁾	1.25 Gb/s ⁽⁶⁾	0.5	–	–	UI
JT_SJ ₆₀₀	Sinusoidal Jitter ⁽³⁾	600 Mb/s	0.4	–	–	UI
JT_SJ ₄₈₀	Sinusoidal Jitter ⁽³⁾	480 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye ⁽²⁾						
JT_TJSE _{3.125}	Total Jitter with Stressed Eye ⁽⁷⁾	3.125 Gb/s	0.70	–	–	UI
		5.0 Gb/s	0.70	–	–	UI
JT_SJSE _{3.125}	Sinusoidal Jitter with Stressed Eye ⁽⁷⁾	3.125 Gb/s	0.1	–	–	UI
		5.0 Gb/s	0.1	–	–	UI

Notes:

- Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 1e^{–12}.
- The frequency of the injected sinusoidal jitter is 80 MHz.
- PLL frequency at 1.5625 GHz and OUTDIV = 1.
- PLL frequency at 2.5 GHz and OUTDIV = 2.
- PLL frequency at 2.5 GHz and OUTDIV = 4.
- Composite jitter with RX equalizer enabled. DFE disabled.

Figure 4 shows the timing parameters in Table 27.

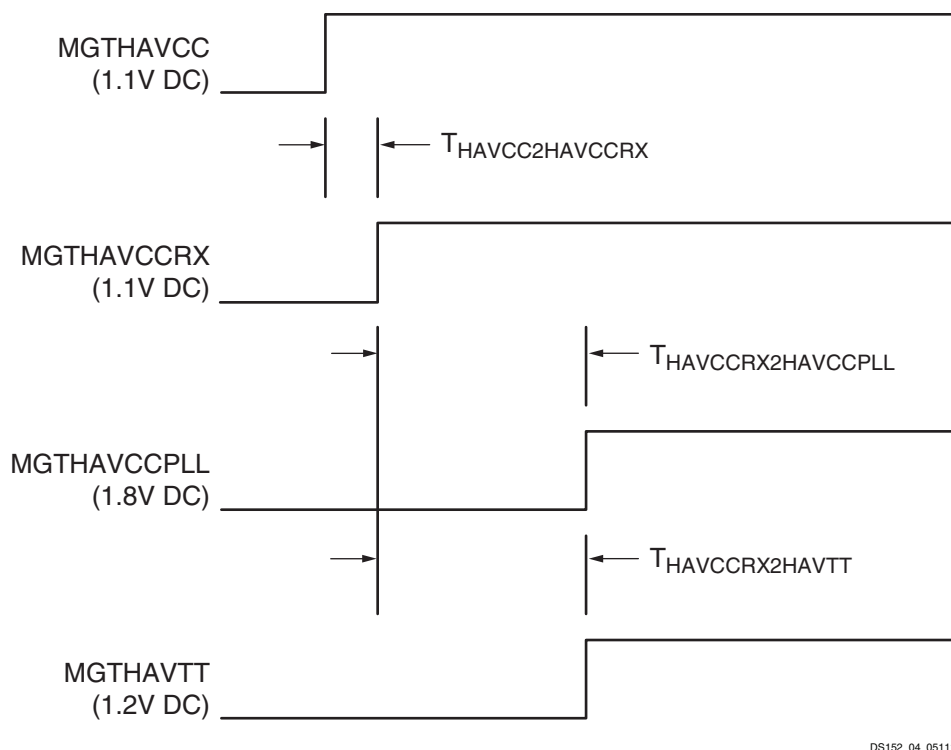


Figure 4: GTH Transceiver Power Supply Power-On Sequencing

Table 28: GTH Transceiver Supply Current

Symbol	Description	Typ ⁽¹⁾	Max	Units
$I_{MGTHAVCC}$	MGTHAVCC supply current for one GTH Quad (4 lanes)	571	Note 2	mA
$I_{MGTHAVCCR}$	MGTHAVCCR supply current for a GTH Quad (4 lanes)	254	Note 2	mA
$I_{MGTHAVTT}$	MGTHAVTT supply current for one GTH Quad (4 lanes)	93	Note 2	mA
$I_{MGTHAVCCPLL}$	MGTHAVCCPLL supply current for one GTH Quad (4 lanes)	219	Note 2	mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	1000.0 ± 1% tolerance		Ω

Notes:

- Typical values are specified at nominal voltage, 25°C, with a 10.3125 Gb/s line rate.
- Values for currents other than the values specified in this table can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

Table 29: GTH Transceiver Quiescent Supply Current⁽¹⁾⁽²⁾

Symbol	Description	Typ ⁽³⁾	Max	Units
$I_{MGTHAVCCQ}$	Quiescent MGTHAVCC Supply Current for one GTH Quad (4 lanes)	65	Note 4	mA
$I_{MGTHAVCCRQ}$	Quiescent MGTHAVCCR Supply Current for one GTH Quad (4 lanes)	17	Note 4	mA
$I_{MGTHAVTTQ}$	Quiescent MGTHAVTT Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA
$I_{MGTHAVCCPLLQ}$	Quiescent MGTHAVCCPLL Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA

Notes:

- Device powered and unconfigured.
- GTH transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTH transceivers.
- Typical values are specified at nominal voltage, 25°C.
- Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.

Table 35: GTH Transceiver User Clock Switching Characteristics ⁽¹⁾

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F _{TXOUT}	TXUSERCLKOUT maximum frequency		350	350	323	MHz
F _{RXOUT}	RXUSERCLKOUT maximum frequency		350	350	323	MHz
F _{TXIN}	TXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz
F _{RXIN}	RXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz

Notes:

1. Clocking must be implemented as described in [UG371](#): Virtex-6 FPGA GTH Transceivers User Guide.

Table 36: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
T _{RTX}	TX Rise time	20%–80%	–	50 ⁽³⁾	–	ps
T _{FTX}	TX Fall time	80%–20%	–	50 ⁽³⁾	–	ps
T _{LLSKEW}	TX lane-to-lane skew	within one GTH Quad	–	–	300	ps
Transmitter Output Jitter⁽¹⁾⁽²⁾						
TJ _{11.18}	Total Jitter	11.181 Gb/s	–	–	0.280	UI
DJ _{11.18}	Deterministic Jitter		–	–	0.170	UI
TJ _{10.3125}	Total Jitter	10.3125 Gb/s	–	–	0.280	UI
DJ _{10.3125}	Deterministic Jitter		–	–	0.170	UI
TJ _{9.953}	Total Jitter	9.953 Gb/s	–	–	0.280	UI
DJ _{9.953}	Deterministic Jitter		–	–	0.170	UI
TJ _{2.667}	Total Jitter	2.667 Gb/s	–	–	0.110	UI
DJ _{2.667}	Deterministic Jitter		–	–	0.060	UI
TJ _{2.488}	Total Jitter	2.488 Gb/s	–	–	0.110	UI
DJ _{2.488}	Deterministic Jitter		–	–	0.060	UI

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit-error ratio of 1e⁻¹².
3. Rise and fall times are specified at the transmitter package balls.

Table 37: GTH Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
R _{XRL}	Run length (CID)		8000	–	–	UI
R _{XPPMTOL}	Data/REFCLK PPM offset tolerance		–200	–	200	ppm
SJ Jitter Tolerance ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾						
JT_SJ _{11.18}	Sinusoidal Jitter	11.18 Gb/s	0.3	–	–	UI
JT_SJ _{10.32}	Sinusoidal Jitter	10.32 Gb/s	0.3	–	–	UI
JT_SJ _{9.95}	Sinusoidal Jitter	9.95 Gb/s	0.3	–	–	UI
JT_SJ _{2.667}	Sinusoidal Jitter	2.667 Gb/s	0.5	–	–	UI
JT_SJ _{2.48}	Sinusoidal Jitter	2.48 Gb/s	0.5	–	–	UI

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. High-frequency jitter tolerance including 6 db of channel loss at a high frequency of the data rate divided by two.

Ethernet MAC Switching Characteristics

Consult [UG368: Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide](#) for further information.

Table 38: Maximum Ethernet MAC Performance

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1	-1L	
F _{TEMACCLIENT}	Client interface maximum frequency	10 Mb/s – 8-bit width	2.5 ⁽¹⁾	2.5 ⁽¹⁾	2.5 ⁽¹⁾	2.5 ⁽¹⁾	MHz
		100 Mb/s – 8-bit width	25 ⁽²⁾	25 ⁽²⁾	25 ⁽²⁾	25 ⁽²⁾	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		1000 Mb/s – 16-bit width	62.5	62.5	62.5	62.5	MHz
		2000 Mb/s – 16-bit width	125	125	125	N/A	MHz
		2500 Mb/s – 16-bit width	156.25	156.25	156.25	N/A	MHz
F _{TEMACPHY}	Physical interface maximum frequency	10 Mb/s – 4-bit width	2.5	2.5	2.5	2.5	MHz
		100 Mb/s – 4-bit width	25	25	25	25	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		2000 Mb/s – 8-bit width	250	250	250	N/A	MHz
		2500 Mb/s – 8-bit width	312.5	312.5	312.5	N/A	MHz

Notes:

1. When not using clock enable, the F_{MAX} is lowered to 1.25 MHz.
2. When not using clock enable, the F_{MAX} is lowered to 12.5 MHz.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [Switching Characteristics, page 26](#).

Table 41: Interface Performances

Description	Speed Grade			
	-3	-2	-1	-1L
Networking Applications				
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	710 Mb/s	710 Mb/s	650 Mb/s	585 Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 10)	1.4 Gb/s	1.3 Gb/s	1.25 Gb/s	1.1 Gb/s
SDR LVDS receiver (SFI-4.1) ⁽¹⁾	710 Mb/s	710 Mb/s	650 Mb/s	585 Mb/s
DDR LVDS receiver (SPI-4.2) ⁽¹⁾	1.4 Gb/s	1.3 Gb/s	1.1 Gb/s	0.9 Gb/s
Maximum Physical Interface (PHY) Rate for Memory Interfaces⁽²⁾⁽³⁾⁽⁴⁾				
DDR2	800 Mb/s	800 Mb/s	800 Mb/s	606 Mb/s
DDR3	1066 Mb/s	1066 Mb/s	800 Mb/s	800 Mb/s
QDR II + SRAM	400 MHz	350 MHz	300 MHz	—
RLDRAM II	500 MHz	400 MHz	350 MHz	—

Notes:

1. LVDS receivers are typically bounded with certain applications where specific DPA algorithms dominate deterministic performance.
2. Verified on Xilinx memory characterization platforms designed according to the guidelines in UG: *Virtex-6 FPGA Memory Interface Solutions User Guide*.
3. Consult [DS186](#); *Virtex-6 FPGA Memory Interface Solutions Data Sheet* for performance and feature information on memory interface cores (controller plus PHY).
4. Memory Interface data rates have not been tested over the junction temperature operating range for military (M) temperature devices. Customers are responsible for specifying and testing their specific M temperature grade memory implementation.

IOB Pad Input/Output/3-State Switching Characteristics

Table 44 (for commercial (XC) Virtex-6 devices) and **Table 45** (for the Defense-grade (XQ) Virtex-6 devices) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 46 summarizes the value of T_{IOTPHZ} . T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDS_25	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
LVDSEXT_25	0.85	0.94	1.09	1.08	1.53	1.65	1.84	1.73	1.53	1.65	1.84	1.73	ns
HT_25	0.85	0.94	1.09	1.08	1.51	1.62	1.78	1.69	1.51	1.62	1.78	1.69	ns
BLVDS_25	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.65	1.39	1.50	1.67	1.65	ns
RSDS_25 (point to point)	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
HSTL_I	0.81	0.91	1.06	1.06	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns
HSTL_II	0.81	0.91	1.06	1.06	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
HSTL_III	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
HSTL_I_18	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
HSTL_II_18	0.81	0.91	1.06	1.06	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
HSTL_III_18	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
SSTL2_I	0.81	0.91	1.06	1.06	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
SSTL2_II	0.81	0.91	1.06	1.06	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
LVC MOS25, Slow, 2 mA	0.51	0.57	0.66	0.70	5.09	5.46	6.01	5.63	5.09	5.46	6.01	5.63	ns
LVC MOS25, Slow, 4 mA	0.51	0.57	0.66	0.70	3.30	3.49	3.79	3.65	3.30	3.49	3.79	3.65	ns
LVC MOS25, Slow, 6 mA	0.51	0.57	0.66	0.70	2.62	2.81	3.08	2.95	2.62	2.81	3.08	2.95	ns
LVC MOS25, Slow, 8 mA	0.51	0.57	0.66	0.70	2.21	2.41	2.72	2.59	2.21	2.41	2.72	2.59	ns
LVC MOS25, Slow, 12 mA	0.51	0.57	0.66	0.70	1.80	1.95	2.17	2.10	1.80	1.95	2.17	2.10	ns
LVC MOS25, Slow, 16 mA	0.51	0.57	0.66	0.70	1.89	2.05	2.29	2.21	1.89	2.05	2.29	2.21	ns
LVC MOS25, Slow, 24 mA	0.51	0.57	0.66	0.70	1.68	1.82	2.02	1.98	1.68	1.82	2.02	1.98	ns
LVC MOS25, Fast, 2 mA	0.51	0.57	0.66	0.70	5.12	5.49	6.04	5.62	5.12	5.49	6.04	5.62	ns
LVC MOS25, Fast, 4 mA	0.51	0.57	0.66	0.70	3.28	3.50	3.82	3.65	3.28	3.50	3.82	3.65	ns
LVC MOS25, Fast, 6 mA	0.51	0.57	0.66	0.70	2.56	2.73	2.99	2.88	2.56	2.73	2.99	2.88	ns
LVC MOS25, Fast, 8 mA	0.51	0.57	0.66	0.70	2.11	2.33	2.65	2.53	2.11	2.33	2.65	2.53	ns
LVC MOS25, Fast, 12 mA	0.51	0.57	0.66	0.70	1.74	1.88	2.08	2.03	1.74	1.88	2.08	2.03	ns
LVC MOS25, Fast, 16 mA	0.51	0.57	0.66	0.70	1.77	1.92	2.13	2.08	1.77	1.92	2.13	2.08	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVC MOS25, Fast, 16 mA	0.57	0.66	0.70	1.92	2.15	2.08	1.92	2.15	2.08	ns
LVC MOS25, Fast, 24 mA	0.57	0.66	0.70	1.79	2.15	1.96	1.79	2.15	1.96	ns
LVC MOS18, Slow, 2 mA	0.61	0.71	0.73	4.47	4.87	4.30	4.47	4.87	4.30	ns
LVC MOS18, Slow, 4 mA	0.61	0.71	0.73	2.96	3.21	2.94	2.96	3.21	2.94	ns
LVC MOS18, Slow, 6 mA	0.61	0.71	0.73	2.43	2.64	2.47	2.43	2.64	2.47	ns
LVC MOS18, Slow, 8 mA	0.61	0.71	0.73	2.11	2.41	2.24	2.11	2.41	2.24	ns
LVC MOS18, Slow, 12 mA	0.61	0.71	0.73	1.99	2.30	2.10	1.99	2.30	2.10	ns
LVC MOS18, Slow, 16 mA	0.61	0.71	0.73	1.95	2.30	2.04	1.95	2.30	2.04	ns
LVC MOS18, Fast, 2 mA	0.61	0.71	0.73	4.23	4.57	4.08	4.23	4.57	4.08	ns
LVC MOS18, Fast, 4 mA	0.61	0.71	0.73	2.76	2.97	2.74	2.76	2.97	2.74	ns
LVC MOS18, Fast, 6 mA	0.61	0.71	0.73	2.28	2.46	2.32	2.28	2.46	2.32	ns
LVC MOS18, Fast, 8 mA	0.61	0.71	0.73	1.99	2.34	2.14	1.99	2.34	2.14	ns
LVC MOS18, Fast, 12 mA	0.61	0.71	0.73	1.80	2.19	1.88	1.80	2.19	1.88	ns
LVC MOS18, Fast, 16 mA	0.61	0.71	0.73	1.74	2.18	1.88	1.74	2.18	1.88	ns
LVC MOS15, Slow, 2 mA	0.73	0.85	0.85	3.77	4.29	3.91	3.77	4.29	3.91	ns
LVC MOS15, Slow, 4 mA	0.73	0.85	0.85	2.79	3.10	2.93	2.79	3.10	2.93	ns
LVC MOS15, Slow, 6 mA	0.73	0.85	0.85	2.32	2.68	2.50	2.32	2.68	2.50	ns
LVC MOS15, Slow, 8 mA	0.73	0.85	0.85	1.98	2.29	2.24	1.98	2.29	2.24	ns
LVC MOS15, Slow, 12 mA	0.73	0.85	0.85	1.91	2.23	2.07	1.91	2.23	2.07	ns
LVC MOS15, Slow, 16 mA	0.73	0.85	0.85	1.83	2.23	1.98	1.83	2.23	1.98	ns
LVC MOS15, Fast, 2 mA	0.73	0.85	0.85	3.77	4.28	3.91	3.77	4.28	3.91	ns
LVC MOS15, Fast, 4 mA	0.73	0.85	0.85	2.53	2.78	2.66	2.53	2.78	2.66	ns
LVC MOS15, Fast, 6 mA	0.73	0.85	0.85	2.05	2.42	2.16	2.05	2.42	2.16	ns
LVC MOS15, Fast, 8 mA	0.73	0.85	0.85	1.90	2.20	2.04	1.90	2.20	2.04	ns
LVC MOS15, Fast, 12 mA	0.73	0.85	0.85	1.77	2.11	1.90	1.77	2.11	1.90	ns
LVC MOS15, Fast, 16 mA	0.73	0.85	0.85	1.76	2.11	1.92	1.76	2.11	1.92	ns
LVC MOS12, Slow, 2 mA	0.81	0.93	0.95	3.39	3.75	3.54	3.39	3.75	3.54	ns
LVC MOS12, Slow, 4 mA	0.81	0.93	0.95	2.63	2.93	2.79	2.63	2.93	2.79	ns
LVC MOS12, Slow, 6 mA	0.81	0.93	0.95	2.11	2.67	2.26	2.11	2.67	2.26	ns
LVC MOS12, Slow, 8 mA	0.81	0.93	0.95	2.02	2.25	2.17	2.02	2.25	2.17	ns
LVC MOS12, Fast, 2 mA	0.81	0.93	0.95	2.98	3.39	3.11	2.98	3.39	3.11	ns
LVC MOS12, Fast, 4 mA	0.81	0.93	0.95	2.16	2.70	2.31	2.16	2.70	2.31	ns
LVC MOS12, Fast, 6 mA	0.81	0.93	0.95	1.89	2.34	2.05	1.89	2.34	2.05	ns
LVC MOS12, Fast, 8 mA	0.81	0.93	0.95	1.82	2.10	1.98	1.82	2.10	1.98	ns
LVDCI_25	0.57	0.70	0.70	2.14	2.82	2.26	2.14	2.82	2.26	ns
LVDCI_18	0.61	0.71	0.73	2.23	2.78	2.38	2.23	2.78	2.38	ns
LVDCI_15	0.73	0.85	0.85	2.01	2.75	2.18	2.01	2.75	2.18	ns
LVDCI_DV2_25	0.57	0.70	0.70	1.83	2.37	2.00	1.83	2.37	2.00	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVDCI_DV2_18	0.61	0.72	0.73	1.81	2.36	1.98	1.81	2.36	1.98	ns
LVDCI_DV2_15	0.73	0.85	0.85	1.77	2.30	1.98	1.77	2.30	1.98	ns
LVPECL_25	0.94	1.09	1.08	1.49	2.68	1.64	1.49	2.68	1.64	ns
HSTL_I_12	0.91	1.06	1.06	1.60	2.48	1.74	1.60	2.48	1.74	ns
HSTL_I_DCI	0.91	1.06	1.06	1.50	2.43	1.64	1.50	2.43	1.64	ns
HSTL_II_DCI	0.91	1.06	1.06	1.49	2.39	1.66	1.49	2.39	1.66	ns
HSTL_II_T_DCI	0.91	1.06	1.06	1.50	2.43	1.64	1.50	2.43	1.64	ns
HSTL_III_DCI	0.91	1.06	1.06	1.45	2.48	1.61	1.45	2.48	1.61	ns
HSTL_I_DCI_18	0.91	1.06	1.06	1.53	2.44	1.66	1.53	2.44	1.66	ns
HSTL_II_DCI_18	0.91	1.06	1.06	1.46	2.41	1.59	1.46	2.41	1.59	ns
HSTL_II_T_DCI_18	0.91	1.06	1.06	1.53	2.43	1.66	1.53	2.43	1.66	ns
HSTL_III_DCI_18	0.91	1.06	1.06	1.54	2.50	1.67	1.54	2.50	1.67	ns
DIFF_HSTL_I_18	0.94	1.09	1.08	1.58	2.30	1.72	1.58	2.30	1.72	ns
DIFF_HSTL_I_DCI_18	0.94	1.09	1.08	1.53	2.21	1.66	1.53	2.21	1.66	ns
DIFF_HSTL_I	0.94	1.09	1.08	1.56	2.28	1.71	1.56	2.28	1.71	ns
DIFF_HSTL_I_DCI	0.94	1.09	1.08	1.50	2.28	1.64	1.50	2.28	1.64	ns
DIFF_HSTL_II_18	0.94	1.09	1.08	1.62	2.33	1.78	1.62	2.33	1.78	ns
DIFF_HSTL_II_DCI_18	0.94	1.09	1.08	1.46	2.18	1.59	1.46	2.18	1.59	ns
DIFF_HSTL_II_T_DCI_18	0.94	1.09	1.08	1.53	2.22	1.66	1.53	2.22	1.66	ns
DIFF_HSTL_II	0.94	1.09	1.08	1.56	2.29	1.72	1.56	2.29	1.72	ns
DIFF_HSTL_II_DCI	0.94	1.09	1.08	1.49	2.26	1.66	1.49	2.26	1.66	ns
SSTL2_I_DCI	0.91	1.06	1.06	1.53	2.51	1.68	1.53	2.51	1.68	ns
SSTL2_II_DCI	0.91	1.06	1.06	1.50	2.50	1.69	1.50	2.50	1.69	ns
SSTL2_II_T_DCI	0.91	1.06	1.06	1.53	2.52	1.68	1.53	2.52	1.68	ns
SSTL18_I	0.91	1.06	1.06	1.58	2.48	1.73	1.58	2.48	1.73	ns
SSTL18_II	0.91	1.06	1.06	1.50	2.46	1.66	1.50	2.46	1.66	ns
SSTL18_I_DCI	0.91	1.06	1.06	1.51	2.49	1.65	1.51	2.49	1.65	ns
SSTL18_II_DCI	0.91	1.06	1.06	1.47	2.41	1.62	1.47	2.41	1.62	ns
SSTL18_II_T_DCI	0.91	1.06	1.06	1.51	2.49	1.65	1.51	2.49	1.65	ns
SSTL15_T_DCI	0.91	1.06	1.06	1.52	2.48	1.66	1.52	2.48	1.66	ns
SSTL15_DCI	0.91	1.06	1.06	1.52	2.48	1.66	1.52	2.48	1.66	ns
DIFF_SSTL2_I	0.94	1.09	1.08	1.60	2.34	1.74	1.60	2.34	1.74	ns
DIFF_SSTL2_I_DCI	0.94	1.09	1.08	1.53	2.25	1.68	1.53	2.25	1.68	ns
DIFF_SSTL2_II	0.94	1.09	1.08	1.54	2.29	1.71	1.54	2.29	1.71	ns
DIFF_SSTL2_II_DCI	0.94	1.09	1.08	1.50	2.23	1.69	1.50	2.23	1.69	ns
DIFF_SSTL2_II_T_DCI	0.94	1.09	1.08	1.53	2.26	1.68	1.53	2.26	1.68	ns
DIFF_SSTL18_I	0.94	1.09	1.08	1.58	2.22	1.73	1.58	2.22	1.73	ns
DIFF_SSTL18_I_DCI	0.94	1.09	1.08	1.51	2.30	1.65	1.51	2.30	1.65	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 47 shows the test setup parameters used for measuring input delay.

Table 47: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)(2)}$	$V_H^{(1)(2)}$	$V_{MEAS}^{(1)(4)(5)}$	$V_{REF}^{(1)(3)(5)}$
LVC MOS, 2.5V	LVC MOS25	0	2.5	1.25	—
LVC MOS, 1.8V	LVC MOS18	0	1.8	0.9	—
LVC MOS, 1.5V	LVC MOS15	0	1.5	0.75	—
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL, Class III	HSTL_III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	$V_{REF} - 1.00$	$V_{REF} + 1.00$	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	$1.2 - 0.125$	$1.2 + 0.125$	$0^{(6)}$	—
LVDS EXT (LVDS Extended Mode), 2.5V	LVDS EXT_25	$1.2 - 0.125$	$1.2 + 0.125$	$0^{(6)}$	—
HT (HyperTransport), 2.5V	LDT_25	$0.6 - 0.125$	$0.6 + 0.125$	$0^{(6)}$	—

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVC MOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H .
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 6.
6. The value given is the differential input voltage.

Block RAM and FIFO Switching Characteristics

Table 57: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Block RAM and FIFO Clock-to-Out Delays						
T _{RCKO_DO} and T _{RCKO_DO_REG} ⁽¹⁾	Clock CLK to DOUT output (without output register) ⁽²⁾⁽³⁾	1.60	1.79	2.08	2.36	ns, Max
	Clock CLK to DOUT output (with output register) ⁽⁴⁾⁽⁵⁾	0.60	0.66	0.75	0.83	ns, Max
T _{RCKO_DO_ECC} and T _{RCKO_DO_ECC_REG}	Clock CLK to DOUT output with ECC (without output register) ⁽²⁾⁽³⁾	2.62	2.89	3.30	3.73	ns, Max
	Clock CLK to DOUT output with ECC (with output register) ⁽⁴⁾⁽⁵⁾	0.71	0.77	0.86	0.94	ns, Max
T _{RCKO_CASC} and T _{RCKO_CASC_REG}	Clock CLK to DOUT output with Cascade (without output register) ⁽²⁾	2.49	2.77	3.18	3.61	ns, Max
	Clock CLK to DOUT output with Cascade (with output register) ⁽⁴⁾	1.29	1.41	1.58	1.79	ns, Max
T _{RCKO_FLAGS}	Clock CLK to FIFO flags outputs ⁽⁶⁾	0.74	0.81	0.91	0.98	ns, Max
T _{RCKO_POINTERS}	Clock CLK to FIFO pointers outputs ⁽⁷⁾	0.90	0.98	1.09	1.21	ns, Max
T _{RCKO_SDBIT_ECC} and T _{RCKO_SDBIT_ECC_REG}	Clock CLK to BITERR (with output register)	0.62	0.68	0.76	0.82	ns, Max
	Clock CLK to BITERR (without output register)	2.21	2.46	2.84	3.23	ns, Max
T _{RCKO_PARITY_ECC}	Clock CLK to ECCPARITY in ECC encode only mode	0.86	0.94	1.06	1.18	ns, Max
T _{RCKO_RDADDR_ECC} and T _{RCKO_RDADDR_ECC_REG}	Clock CLK to RDADDR output with ECC (without output register)	0.73	0.79	0.90	1.00	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.76	0.82	0.92	1.02	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{RCKC_ADDR} /T _{RCKC_ADDR}	ADDR inputs ⁽⁸⁾	0.47/ 0.27	0.53/ 0.29	0.62/ 0.32	0.66/ 0.34	ns, Min
T _{RDCK_DI} /T _{RCKD_DI}	DIN inputs ⁽⁹⁾	0.84/ 0.30	0.95/ 0.32	1.11/ 0.34	1.26/ 0.36	ns, Min
T _{RDCK_DI_ECC} /T _{RCKD_DI_ECC}	DIN inputs with block RAM ECC in standard mode ⁽⁹⁾	0.47/ 0.30	0.52/ 0.32	0.59/ 0.34	0.68/ 0.36	ns, Min
	DIN inputs with block RAM ECC encode only ⁽⁹⁾	0.68/ 0.30	0.75/ 0.32	0.85/ 0.34	0.97/ 0.36	ns, Min
	DIN inputs with FIFO ECC in standard mode ⁽⁹⁾	0.77/ 0.30	0.87/ 0.32	1.02/ 0.34	1.16/ 0.36	ns, Min
T _{RCKC_CLK} /T _{RCKC_CLK}	Inject single/double bit error in ECC mode	0.90/ 0.27	1.02/ 0.28	1.20/ 0.29	1.56/ 0.29	ns, Min
T _{RCKC_RDEN} /T _{RCKC_RDEN}	Block RAM Enable (EN) input	0.31/ 0.26	0.35/ 0.27	0.41/ 0.30	0.44/ 0.31	ns, Min
T _{RCKC_REGCE} /T _{RCKC_REGCE}	CE input of output register	0.18/ 0.25	0.19/ 0.27	0.22/ 0.31	0.24/ 0.33	ns, Min
T _{RCKC_RSTREG} /T _{RCKC_RSTREG}	Synchronous RSTREG input	0.22/ 0.23	0.24/ 0.24	0.28/ 0.26	0.31/ 0.27	ns, Min
T _{RCKC_RSTRAM} /T _{RCKC_RSTRAM}	Synchronous RSTRAM input	0.32/ 0.23	0.36/ 0.24	0.41/ 0.27	0.46/ 0.29	ns, Min

DSP48E1 Switching Characteristics

Table 58: DSP48E1 Switching Characteristics

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock							
$T_{\text{DSPDCK}_{\{A, \text{ACIN}; B, \text{BCIN}\}}_{\{\text{AREG}; \text{BREG}\}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}; B, \text{BCIN}\}}_{\{\text{AREG}; \text{BREG}\}}}$	{A, ACIN, B, BCIN} input to {A, B} register CLK	0.25/ 0.27	0.29/ 0.30	0.35/ 0.34	0.36/ 0.34	0.46/ 0.39	ns
$T_{\text{DSPDCK}_{\text{C_CREG}}/T_{\text{DSPCKD}_{\text{C_CREG}}}}$	C input to C register CLK	0.16/ 0.20	0.19/ 0.22	0.22/ 0.24	0.25/ 0.24	0.33/ 0.30	ns
$T_{\text{DSPDCK}_{\text{D_DREG}}/T_{\text{DSPCKD}_{\text{D_DREG}}}}$	D input to D register CLK	0.07/ 0.31	0.10/ 0.34	0.15/ 0.39	0.16/ 0.39	0.24/ 0.45	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock							
$T_{\text{DSPDCK}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{MREG_MULT}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{MREG_MULT}}}$	{A, ACIN, B, BCIN} input to M register CLK	2.36/ 0.04	2.70/ 0.04	3.21/ 0.04	3.21/ 0.04	3.66/ 0.02	ns
$T_{\text{DSPDCK}_{\{A, D\}}_{\text{ADREG}}/T_{\text{DSPCKD}_{\{A, D\}}_{\text{ADREG}}}$	{A, D} input to AD register CLK	1.24/ 0.10	1.42/ 0.12	1.69/ 0.13	1.69/ 0.13	1.91/ 0.16	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock							
$T_{\text{DSPDCK}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG_MULT}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG_MULT}}}$	{A, ACIN, B, BCIN} input to P register CLK using multiplier	3.83/ −0.13	4.37/ −0.13	5.20/ −0.13	5.20/ −0.13	5.94/ −0.24	ns
$T_{\text{DSPDCK}_{\text{D_PREG_MULT}}/T_{\text{DSPCKD}_{\text{D_PREG_MULT}}}}$	D input to P register CLK	3.62/ −0.47	4.13/ −0.47	4.90/ −0.47	4.90/ −0.47	5.61/ −0.77	ns
$T_{\text{DSPDCK}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG}}}$	{A, ACIN, B, BCIN} input to P register CLK not using multiplier	1.59/ −0.13	1.81/ −0.13	2.15/ −0.13	2.15/ −0.13	2.44/ −0.24	ns
$T_{\text{DSPDCK}_{\text{C_PREG}}/T_{\text{DSPCKD}_{\text{C_PREG}}}}$	C input to P register CLK	1.42/ −0.10	1.61/ −0.10	1.91/ −0.10	1.91/ −0.10	2.16/ −0.19	ns
$T_{\text{DSPDCK}_{\{\text{PCIN}, \text{CARRYCASCIN}, \text{MULTSIGNIN}\}}_{\text{PREG}}/T_{\text{DSPCKD}_{\{\text{PCIN}, \text{CARRYCASCIN}, \text{MULTSIGNIN}\}}_{\text{PREG}}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK	1.23/ −0.02	1.41/ −0.02	1.67/ −0.02	1.67/ −0.02	1.91/ −0.07	ns
Setup and Hold Times of the CE Pins							
$T_{\text{DSPDCK}_{\{\text{CEA}; \text{CEB}\}}_{\{\text{AREG}; \text{BREG}\}}/T_{\text{DSPCKD}_{\{\text{CEA}; \text{CEB}\}}_{\{\text{AREG}; \text{BREG}\}}}$	{CEA; CEB} input to {A; B} register CLK	0.14/ 0.19	0.17/ 0.22	0.22/ 0.25	0.22/ 0.25	0.30/ 0.28	ns
$T_{\text{DSPDCK}_{\text{CEC_CREG}}/T_{\text{DSPCKD}_{\text{CEC_CREG}}}}$	CEC input to C register CLK	0.15/ 0.18	0.18/ 0.20	0.24/ 0.23	0.24/ 0.23	0.31/ 0.26	ns
$T_{\text{DSPDCK}_{\text{CED_DREG}}/T_{\text{DSPCKD}_{\text{CED_DREG}}}}$	CED input to D register CLK	0.20/ 0.12	0.24/ 0.13	0.31/ 0.14	0.31/ 0.14	0.43/ 0.16	ns
$T_{\text{DSPDCK}_{\text{CEM_MREG}}/T_{\text{DSPCKD}_{\text{CEM_MREG}}}}$	CEM input to M register CLK	0.16/ 0.19	0.20/ 0.21	0.26/ 0.25	0.26/ 0.25	0.32/ 0.28	ns
$T_{\text{DSPDCK}_{\text{CEP_PREG}}/T_{\text{DSPCKD}_{\text{CEP_PREG}}}}$	CEP input to P register CLK	0.32/ 0.02	0.38/ 0.02	0.46/ 0.03	0.46/ 0.03	0.54/ 0.04	ns
Setup and Hold Times of the RST Pins							
$T_{\text{DSPDCK}_{\{\text{RSTA}; \text{RSTB}\}}_{\{\text{AREG}; \text{BREG}\}}/T_{\text{DSPCKD}_{\{\text{RSTA}; \text{RSTB}\}}_{\{\text{AREG}; \text{BREG}\}}}$	{RSTA, RSTB} input to {A, B} register CLK	0.27/ 0.17	0.31/ 0.19	0.38/ 0.22	0.38/ 0.22	0.41/ 0.25	ns
$T_{\text{DSPDCK}_{\text{RSTC_CREG}}/T_{\text{DSPCKD}_{\text{RSTC_CREG}}}}$	RSTC input to C register CLK	0.18/ 0.08	0.20/ 0.08	0.23/ 0.09	0.23/ 0.09	0.27/ 0.11	ns
$T_{\text{DSPDCK}_{\text{RSTD_DREG}}/T_{\text{DSPCKD}_{\text{RSTD_DREG}}}}$	RSTD input to D register CLK	0.28/ 0.15	0.32/ 0.16	0.38/ 0.19	0.38/ 0.19	0.45/ 0.21	ns
$T_{\text{DSPDCK}_{\text{RSTM_MREG}}/T_{\text{DSPCKD}_{\text{RSTM_MREG}}}}$	RSTM input to M register CLK	0.20/ 0.24	0.23/ 0.26	0.26/ 0.30	0.26/ 0.30	0.29/ 0.34	ns

Table 59: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{\text{MMCMDCK_DI}}/$ $T_{\text{MMCCKD_DI}}$	DI Setup/Hold	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{\text{MMCMDCK_DEN}}/$ $T_{\text{MMCCKD_DEN}}$	DEN Setup/Hold time	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{\text{MMCMDCK_DWE}}/$ $T_{\text{MMCCKD_DWE}}$	DWE Setup/Hold time	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{\text{MMCCKO_DO}}$	CLK to out of DO ⁽³⁾	2.60	3.02	3.64	3.68	ns
$T_{\text{MMCCKO_DRDY}}$	CLK to out of DRDY	0.32	0.34	0.38	0.38	ns

Notes:

1. To support longer delays in configuration, use the design solutions described in [UG360: Virtex-6 FPGA Configuration User Guide](#).
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
3. DO will hold until next DRP operation.

Clock Buffers and Networks

Table 60: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	Devices	Speed Grade				Units
			-3	-2	-1	-1L	
$T_{\text{BCCCK_CE}}/T_{\text{BCCCK_CE}}^{(1)}$	CE pins Setup/Hold	All	0.11/ 0.00	0.13/ 0.00	0.16/ 0.00	0.13/ 0.00	ns
$T_{\text{BCCCK_S}}/T_{\text{BCCCK_S}}^{(1)}$	S pins Setup/Hold	All	0.11/ 0.00	0.13/ 0.00	0.16/ 0.00	0.13/ 0.00	ns
$T_{\text{BCKO_O}}^{(2)}$	BUFGCTRL delay from I0/I1 to O	All	0.07	0.08	0.10	0.10	ns
Maximum Frequency							
F_{MAX}	Global clock tree (BUFG)	All except LX760	800	750	700	667	MHz
		LX760	N/A	700	700	667	MHz

Notes:

1. $T_{\text{BCCCK_CE}}$ and $T_{\text{BCCCK_S}}$ must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. $T_{\text{BCKO_O}}$ (BUFG delay from I0 to O) values are the same as $T_{\text{BCKO_O}}$ values.

Table 61: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{\text{BIOCKO_O}}$	Clock to out delay from I to O	0.14	0.16	0.18	0.21	ns
Maximum Frequency						
F_{MAX}	I/O clock tree (BUFIO)	800	800	710	710	MHz

Table 62: Regional Clock Switching Characteristics (BUFR)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{\text{BRCKO_O}}$	Clock to out delay from I to O	0.56	0.62	0.73	0.82	ns
$T_{\text{BRCKO_O_BYP}}$	Clock to out delay from I to O with Divide Bypass attribute set	0.28	0.31	0.36	0.41	ns

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 FPGA clock transmitter and receiver data-valid windows.

Table 71: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion ⁽¹⁾	All	0.12	0.12	0.12	0.12	ns
T_{CKSKEW}	Global Clock Tree Skew ⁽²⁾	XC6VLX75T	0.15	0.16	0.18	0.17	ns
		XC6VLX130T	0.25	0.26	0.29	0.28	ns
		XC6VLX195T	0.26	0.27	0.31	0.30	ns
		XC6VLX240T	0.26	0.27	0.31	0.30	ns
		XC6VLX365T	0.28	0.29	0.31	0.31	ns
		XC6VLX550T	N/A	0.50	0.54	0.54	ns
		XC6VLX760	N/A	0.51	0.56	0.56	ns
		XC6VSX315T	0.27	0.28	0.32	0.30	ns
		XC6VSX475T	N/A	0.39	0.44	0.42	ns
		XC6VHX250T	0.25	0.26	0.29	N/A	ns
		XC6VHX255T	0.35	0.37	0.41	N/A	ns
		XC6VHX380T	0.45	0.47	0.52	N/A	ns
		XC6VHX565T	N/A	0.46	0.51	N/A	ns
		XQ6VLX130T	N/A	0.26	0.29	0.28	ns
		XQ6VLX240T	N/A	0.27	0.31	0.30	ns
		XQ6VLX550T	N/A	N/A	0.54	0.54	ns
		XQ6VSX315T	N/A	0.28	0.32	0.30	ns
		XQ6VSX475T	N/A	N/A	0.44	0.42	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.08	0.08	0.08	0.08	ns
T_{BUFIO_SKEW}	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	0.02	ns
T_{BUFIO_SKEW2}	I/O clock tree skew across three clock regions	All	0.10	0.12	0.23	0.12	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	ns

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Date	Version	Description of Revisions
02/08/11	2.12	Removed note 1 from Table 4 as the larger devices (XC6VLX550T, XC6VLX760, XC6VSX475T, and XC6VHX565T) are now offered in -2I. Updated Table 4 and Table 5 with data for the XC6VHX380T in the FF(G)1154 package. In Table 41 , updated -1L specification for DDR3. Added Note 1 to Table 42 . Moved the XC6VHX380T devices in the FF(G)1154 package to production release in Table 43 using ISE 12.4 software with current speed specifications. Updated description for F_{INDUTY} in Table 64 .
02/25/11	3.0	Designated the data sheet as Preliminary for all devices not already labeled production in Table 42 . Changed the XC6VHX380T devices in all packages to production status in Table 42 and Table 43 . Removed note 1 from Table 42 . Added maximum specifications to Table 25 . Updated $T_{HAVCC2HAVCCRX}$ in Table 27 . Updated the typical values and notes in Table 28 and Table 29 . Added values to Table 30 and Table 31 . In Table 34 , added values for T_{LOCK} and T_{PHASE} . Updated the values in Table 36 and added note 3. Updated Table 37 and added note 4.
03/21/11	3.1	Updated Table 2 including Note 7 . In Table 4 , added Note 3 and -2E, extended temperature range to the XC6VLX550T, XC6VLX760, XC6VSX475T, and XC6VHX380T devices, and added Note 5 for the XC6VHX565T. Updated Table 28 typical values. Updated the description for $F_{IDELAYCTRL_REF}$ in Table 53 . Updated F_{MCCK} in Table 59 .
04/01/11	3.2	Added T_j values for C, E, and I temperature ranges to Table 2 . Updated the I_{CCQ} values in Table 4 . Updated F_{GCLK} in Table 34 . Designated the data sheet as Production for all devices not already labeled production in Table 42 . Changed the XC6VHX255T and XC6VHX565T devices in all packages to production status in Table 42 and Table 43 . This included updates to the Virtex-6 Device Pin-to-Pin Output Parameter Guidelines and Virtex-6 Device Pin-to-Pin Input Parameter Guidelines for these devices. Production speed specifications for these devices are available using the speed specification v1.14 in the ISE 13.1 software update. Updated and added package skew values to Table 72 ; these values are correct with regards to previous production released speed specifications in software. Updated copyright page 1 and Notice of Disclaimer .
12/08/11	3.3	Production release of the Defense-grade XQ devices in Table 42 and Table 43 using ISE v13.3 v1.17 Patch for -2 and -1 speed specifications; and v1.10 for -1L speed specifications. Added the XQ6VLX130T, XQ6VLX240T, XQ6VLX550T, XQ6VSX315T, and XQ6VSX475T to the data sheet which included adding Table 45 . Updated T_j in Table 2 . In Table 40 , updated T_j for most specifications and added Note 4 . Added Note 4 to Table 41 . Added -1(XQ) speed specification columns only to Table 50 , Table 51 , Table 52 , and Table 58 . Updated V_{OD} in Table 8 , V_{OCM} in Table 9 , and V_{OCM} and V_{DIFF} in Table 10 . Updated the Power-On Power Supply Requirements section. In Table 27 , updated maximum specification for $T_{HAVCC2HAVCCRX}$ and added Note 3 . Updated T_j in Table 40 . In Table 41 , increased the DDR LVDS receiver (SPI-4.2) -1 speed grade performance value from 1.0 Gb/s to 1.1 Gb/s. In Table 60 , updated the F_{MAX} to add a separate row for the LX760 device values. The speed specifications in the software tools have always matched these values for the LX760, the data sheet is now correct. Updated the notes for $T_{OUTJITTER}$ in Table 64 .
01/12/12	3.4	Added the temperature range -2E to Note 5 in Table 4 .